THE SEMICONDUCTOR DATA BOOK
SUPPLEMENT 2

This is the second supplement to the 2nd Edition of the Semiconductor Data Book originally published in August 1966. It is produced to keep an up-to-date listing of the most advanced semiconductor products.

Devices characterized in this supplement include only the type numbers introduced after the publication of the first supplement to the Semiconductor Data Book. For a complete compilation of all devices, use this Supplement in conjunction with the Data Book and Supplement I.

The information in this handbook has been carefully checked and is believed to be reliable; however, no responsibility is assumed for inaccuracies.

CONTENTS

Indicated section numbers coincide with the section numbers in the Semiconductor Data Book in which other devices of the same type are characterized.

IV

The following standard devices are now available as JAN units:

Device Type Number	Description		Data Book Page Number
JAN2N559-1	PNP Germanium Switching Transistor	(Supplement 2)	8- 2
JAN2N559-2	PNP Germanium Switching Transistor	(Supplement 2)	8- 2
JAN2N559-3	PNP Germanium Switching Transistor	(Supplement 2)	8- 2
JAN2N703	NPN Silicon Switching Transistor		8- 8
JAN2N708	NPN Silicon Switching Transistor		8- 17
JAN2N718A	NPN Silicon Switching and Amplifier Transistor		8- 22
JAN2N916	NPN Silicon Switching and Amplifier Transistor		8- 45
JAN2N1613	NPN Silicon Switching and Amplifier Transistor		8- 22
JAN2N1711	NPN Silicon Switching and Amplifier Transistor		8- 22
JAN2N1893	NPN Silicon Switching and Amplifier Transistor		8- 70
JAN2N2369A	NPN Silicon Switching Transistor		8- 92
JAN2N2708	NPN Silicon Amplifier Transistor	(Supplement 2)	8- 29
JAN2N2919	NPN Silicon Multiple Device		11- 7
JAN2N2920	NPN Silicon Multiple Device		11- 7
JAN2N3127	PNP Germanium Amplifier Transistor	(Supplement 2)	9- 4
JAN2N3253	NPN Silicon Switching Transistor		8-147
JAN2N3444	NPN Silicon Switching Transistor		8-147
JAN2N3498	NPN Silicon Switching and Amplifier Transistor		8-161
JAN2N3499	NPN Silicon Switching and Amplifier Transistor		8-161
JAN2N3500	NPN Silicon Switching and Amplifier Transistor		8-161
JAN2N3501	NPN Silicon Switching and Amplifier Transistor		8-161
JAN2N3506	NPN Silicon Switching Transistor		8-167
JAN2N3507	NPN Silicon Switching Transistor		8-167
JAN2N3634	PNP Silicon Switching and Amplifier Transistor		8-178
JAN2N3635	PNP Silicon Switching and Amplifier Transistor		8-178
JAN2N3636	PNP Silicon Switching and Amplifier Transistor		8-178
JAN2N3637	PNP Silicon Switching and Amplifier Transistor		8-178
JAN2N3810	PNP Silicon Multiple Device	(Supplement 2)	11- 20
JAN2N3811	PNP Silicon Multiple Device	(Supplement 2)	11- 20

DEVICE INDEX

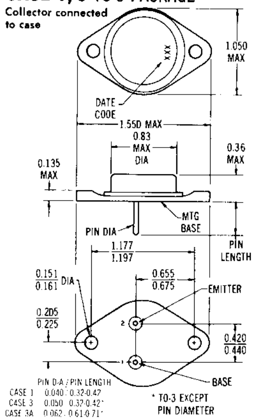
The following is an alpha-numerical list of the devices contained in this supplement.

DEVICE DIMENSION DRAWINGS

All dimensions are in inches

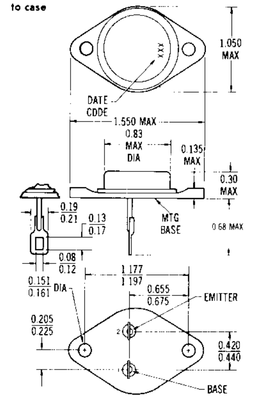
CASE 1, 3 TO-3 PACKAGE

Collector connected to case



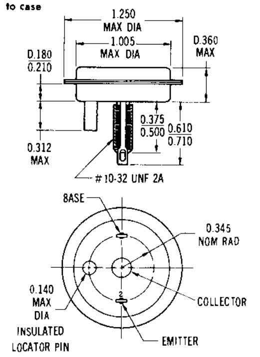
CASE 4 TO-41 PACKAGE

Collector connected to case



CASE 5, 6, 7 TO-36 PACKAGE

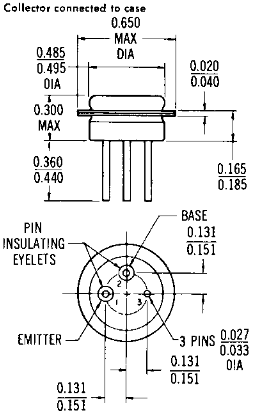
Collector connected to case



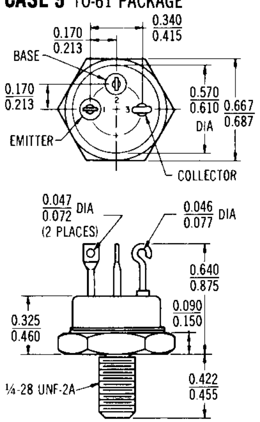
CASE 5 (WITH LUGS)
CASE 6 (WITH FLEXIBLE LEADS)
CASE 7 (WITH STRAIGHT LEADS)

CASE 8

Collector connected to case

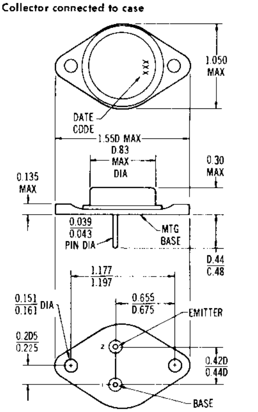


CASE 9 TO-61 PACKAGE



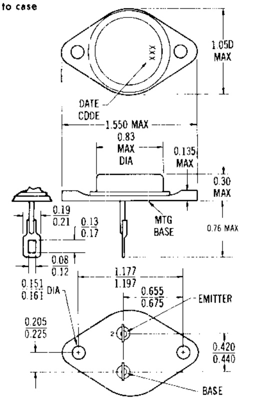
CASE 11 TO-3 PACKAGE

Collector connected to case

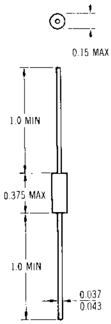


CASE 16 (TO-41 Except Lug Length)

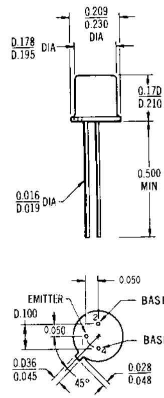
Collector connected to case



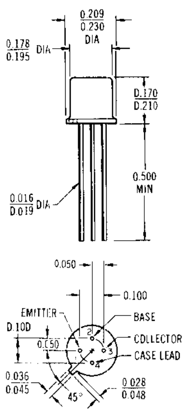
CASE 17



CASE 19 TO-72 PACKAGE

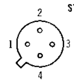


CASE 20 TO-72 PACKAGE



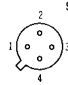
CASE 20 STYLES

STYLE 1



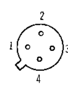
Pin 1. Source
2. Drain
3. Gate
4. Case

STYLE 2



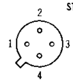
Pin 1. Source
2. Gate
3. Drain
4. Substrate and Case

STYLE 3



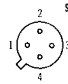
Pin 1. Drain
2. Source
3. Gate
4. Case

STYLE 4



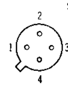
Pin 1. Source
2. Gate 1
3. Drain
4. Gate 2 – Substrate and Case

STYLE 5



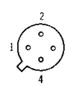
Pin 1. Source
2. Gate
3. Drain
4. Case

STYLE 6



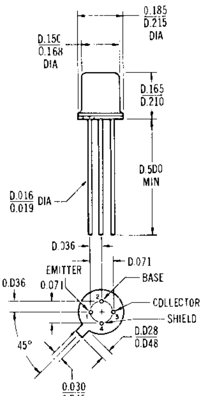
Pin 1. Drain
2. Source and Substrate
3. Gate
4. Source and Substrate

STYLE 7

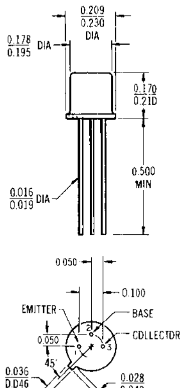


Pin 1. Drain
2. Source
3. Gate
4. Case and Substrate

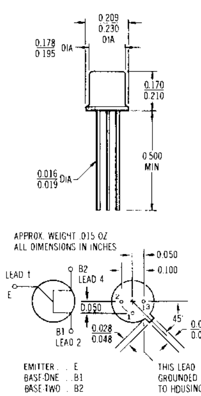
CASE 21 TO-17 PACKAGE



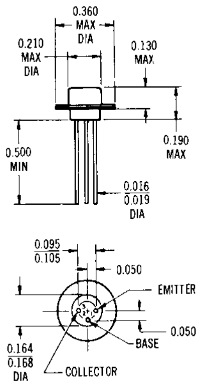
CASE 22 TO-18 PACKAGE



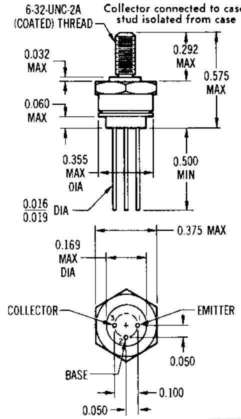
CASE 22A TO-18 PACKAGE



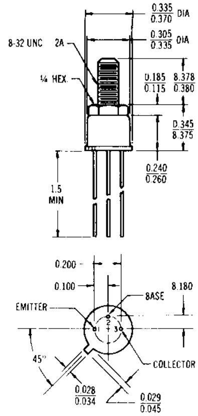
CASE 23 TO-107 PACKAGE



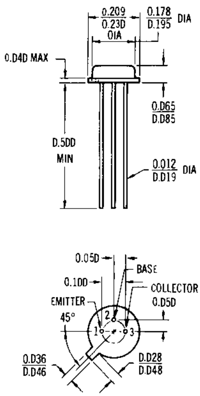
CASE 24 TO-102 PACKAGE



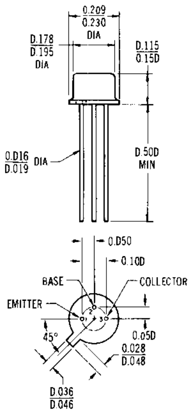
CASE 25



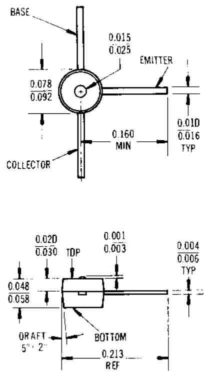
CASE 26 TO-46 PACKAGE



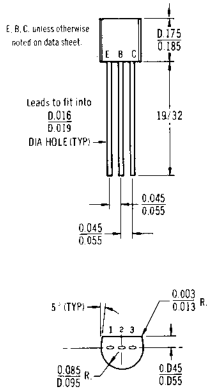
CASE 27 TO-52 PACKAGE



CASE 28



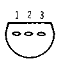
CASE 29 TO-92 PACKAGE
PLASTIC TRANSISTOR



CASE 29 STYLES

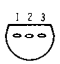
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 1



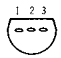
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2



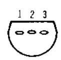
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 3



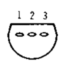
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 4



PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 5

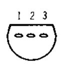


PIN 1. GATE
2. SOURCE AND SUBSTRATE
3. DRAIN

STYLE 6

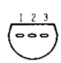
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 7



PIN 1. DRAIN
2. GATE
3. SOURCE AND SUBSTRATE

STYLE 8



PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 9

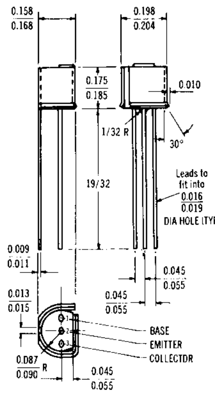
(UNIJUNCTIONS)

PIN 1. CATHODE
2. GATE
3. ANODE

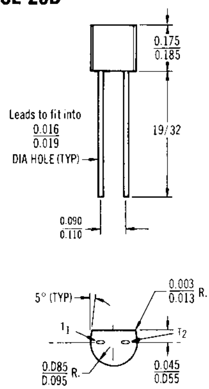
STYLE 18

All dimensions are in inches

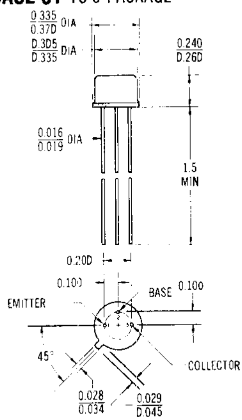
CASE 29A PLASTIC TRANSISTOR WITH SHIELD



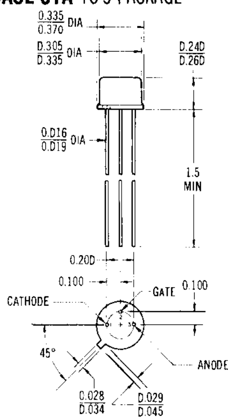
CASE 29B



CASE 31 TO-5 PACKAGE

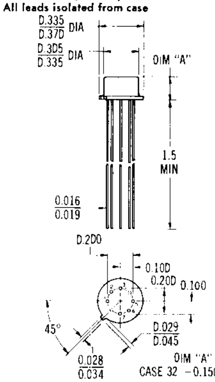


CASE 31A TO-5 PACKAGE



CASE 32, 32A, 32B

All leads isolated from case



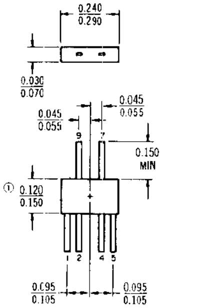
PINS 4 AND 8 OMITTED

DIM "A"
CASE 32 – 0.150/0.180
CASE 32A – 0.140/0.260
CASE 32B, TO-77 – 0.240/0.260

CASE 33, 33A TO-89 PACKAGE

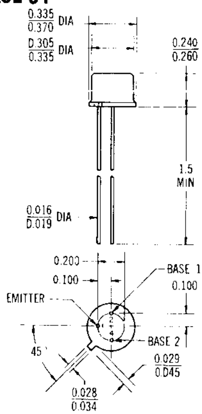
All leads isolated from case

Lead 1 identified by square impression on underside of case.



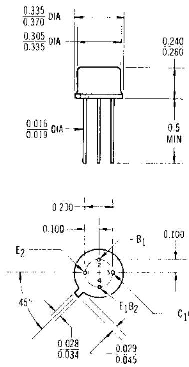
① CASE 33A 0.115/0.135

CASE 34



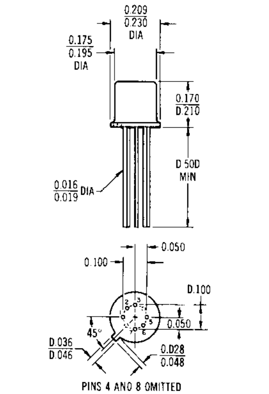
CASE 34A TO-12 PACKAGE

Collectors Connected to Case

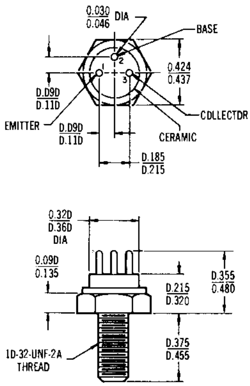


CASE 35 TO-71 PACKAGE

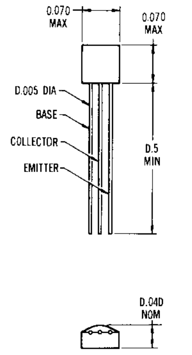
All leads isolated from case



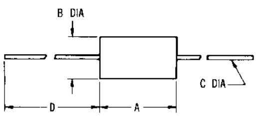
CASE 36 TO-60 PACKAGE



CASE 37 CERAMIC PACKAGE

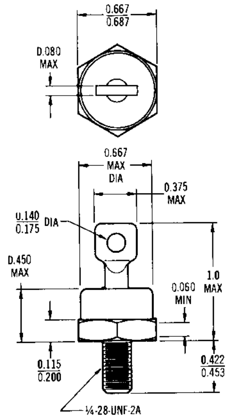


CASE 41

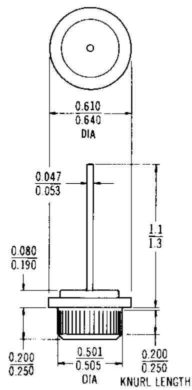


PKG.	A MAX	B MAX	C ±0.002	D MIN
	OUTLINE DIMENSIONS (INCHES)			
41-1	1.00	0.500	0.032	1.25
41-2	0.500	0.375	0.032	1.25
41-3	1.030	0.378	0.032	1.25
41-4	1.220	0.641	0.032	1.75
41-5	0.655	0.641	0.032	1.25
41-6	0.520	0.275	0.022	1.25
41-7	1.000	0.375	0.032	1.25

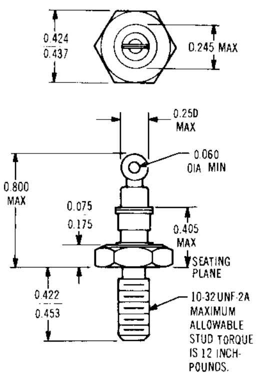
CASE 42 DO-5 PACKAGE



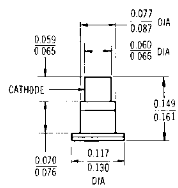
CASE 43 DO-21 PACKAGE



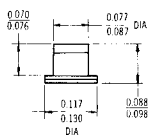
CASE 44 DO-4 PACKAGE



CASE 45

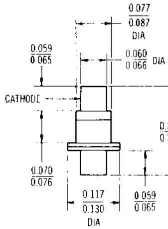


CASE 45A

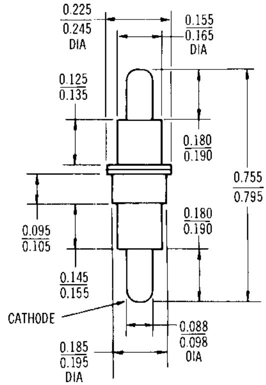


All dimensions are in inches

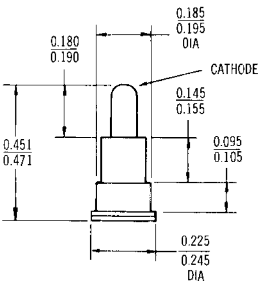
CASE 46



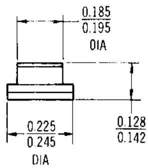
CASE 47



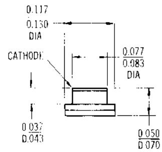
CASE 47A



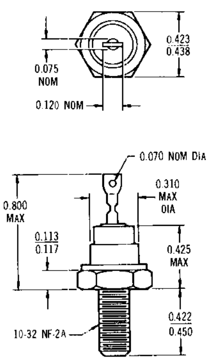
CASE 47B



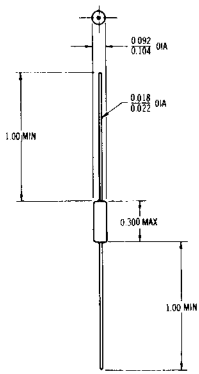
CASE 48



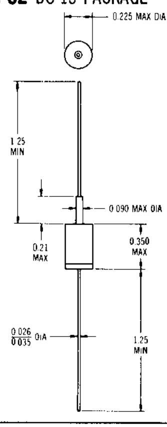
CASE 49



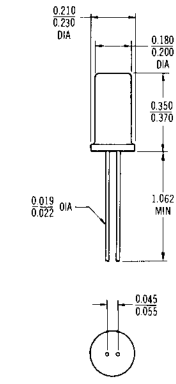
CASE 51 DO-7 PACKAGE



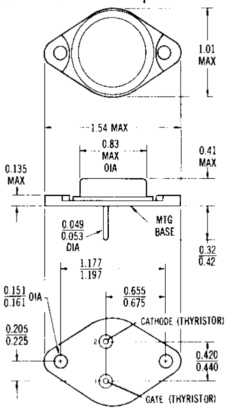
CASE 52 DO-13 PACKAGE



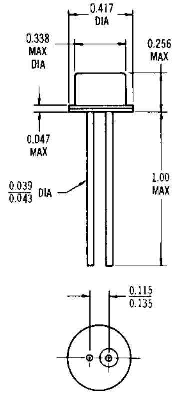
CASE 53



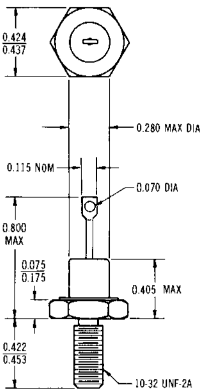
CASE 54 TO-3 Except Pin Diameter



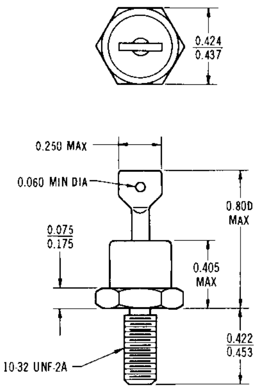
CASE 55



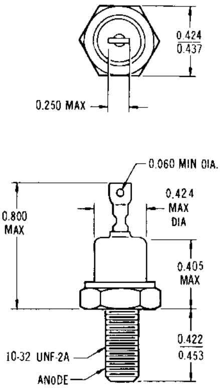
CASE 56 DO-4 PACKAGE



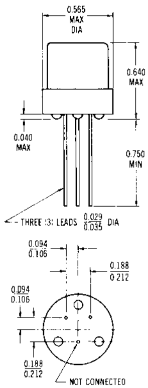
CASE 56A DO-4 PACKAGE



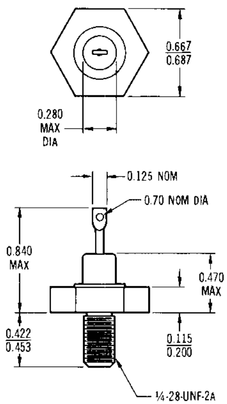
CASE 56B



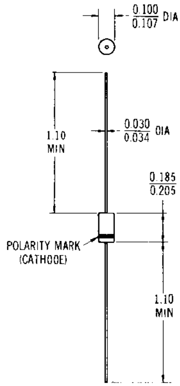
CASE 57



CASE 58

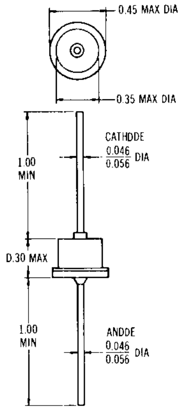


CASE 59

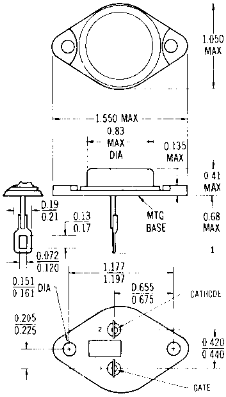


All dimensions are in inches

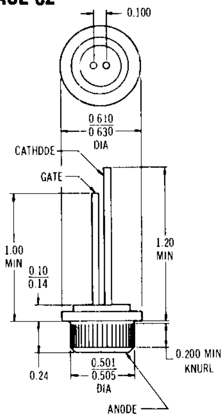
CASE 60



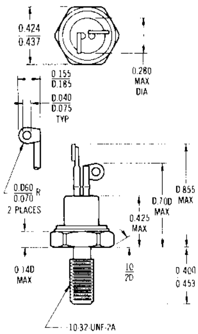
CASE 61 TO-41 PACKAGE



CASE 62

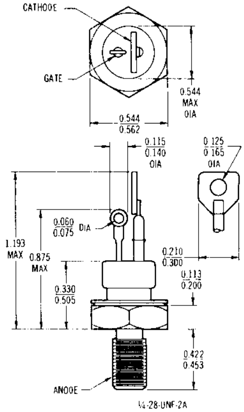


CASE 63

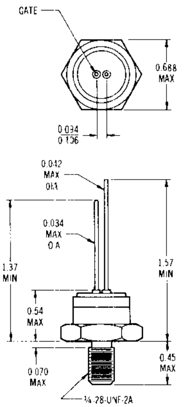


Contour not defined in area bounded by 0.280 max diameter (A) and 0.425 max dimensions (B).

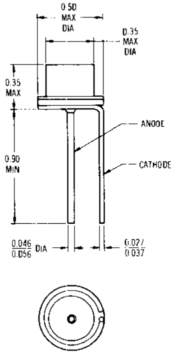
CASE 64 TO-48 PACKAGE



CASE 68

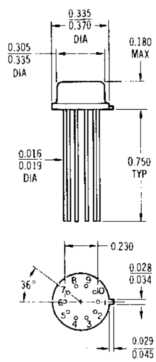


CASE 70



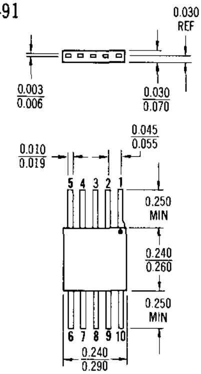
CASE 71, 71A

CASE 71A –
PIN IO UNDER
TAB



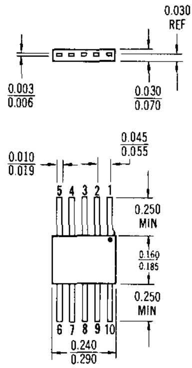
All dimensions are in inches

CASE 72 10-LEAD FLAT PACKAGE
TO-91



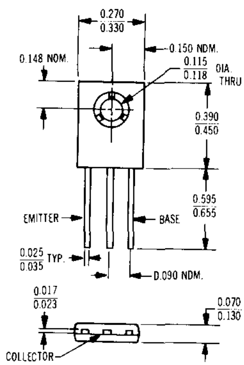
Lead 1 identified by color dot or by shoulder on lead. All leads electrically isolated from package.

CASE 73 10-LEAD FLAT PACKAGE

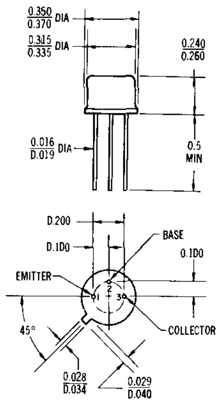


Lead 1 identified by color dot or by shoulder on lead. All leads electrically isolated from package.

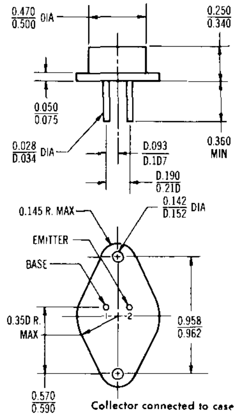
CASE 77
PLASTIC TRANSISTOR



CASE 79 TO-39 PACKAGE

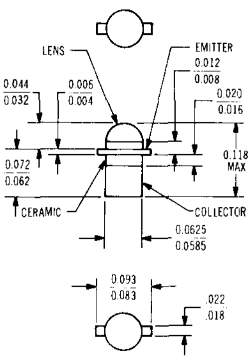


CASE 80 TO-66 PACKAGE

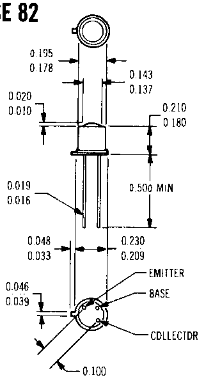


Collector connected to case

CASE 81



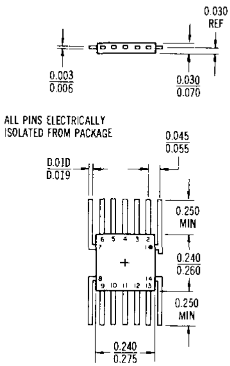
CASE 82



NOTES: Leads are gold-plated kovar
Collector internally connected to case.
Package weight ≈ 0.45 grams

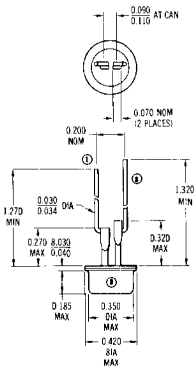
CASE 83 14-LEAD FLAT PACKAGE
TO-86

LEAD 1 IDENTIFIED BY COLOR DOT OR BY ELBOW ON PIN.

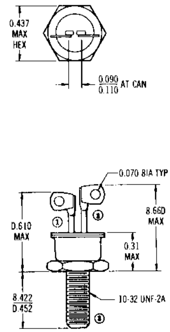


LEAD	THYRISTOR	TRIAC
①	GATE	GATE
②	CATHODE	A1
③	ANODE	A2

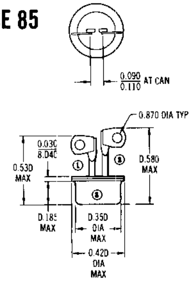
CASE 85L



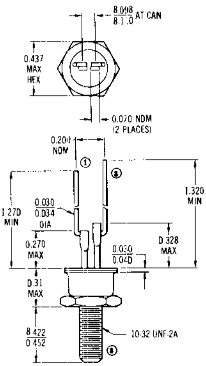
CASE 86



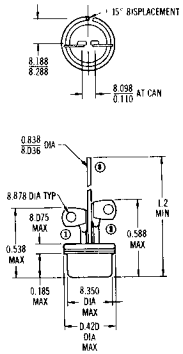
CASE 85



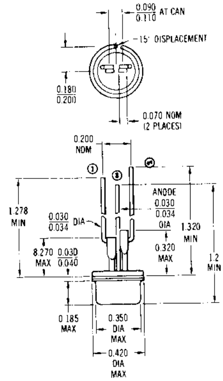
CASE 86L



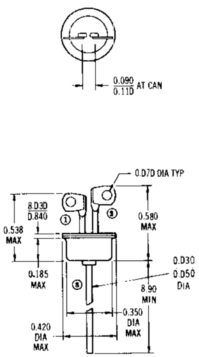
CASE 87



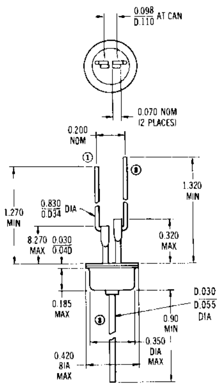
CASE 87L



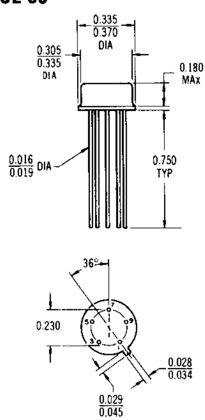
CASE 88



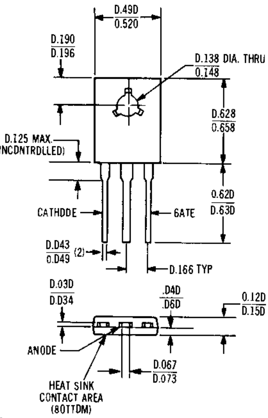
CASE 88L



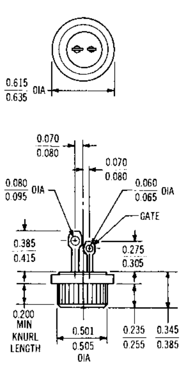
CASE 89



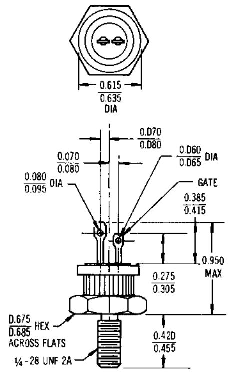
CASE 90



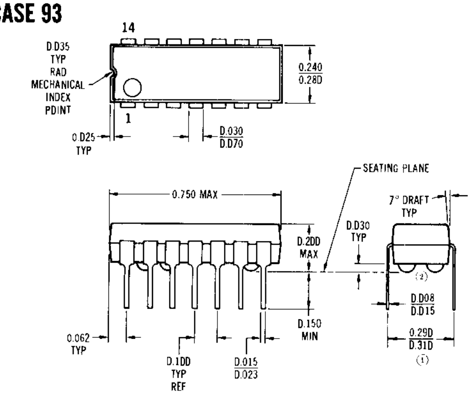
CASE 91



CASE 92

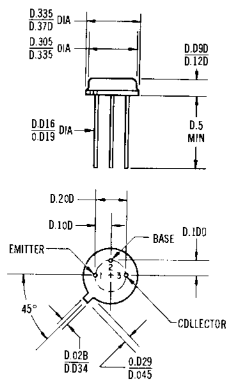


CASE 93

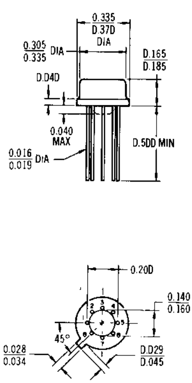


(1) This dimension is measured at the seating plane.
(2) 4 insulating stand-offs are provided.

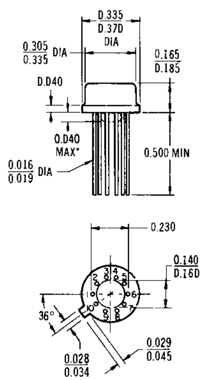
CASE 94



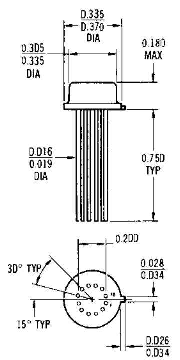
CASE 96 TO-99 PACKAGE



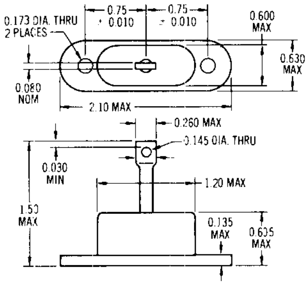
CASE 96A TO-100 PACKAGE



CASE 98



CASE 100



I_O Output Current	A HEX	B_1 MAX	B_2 MAX	C MAX DIA	D_1 MAX	D_2 MAX	E_1 DIA
80	1.250	0.135	0.113	1.20	0.525	0.590	0.250
160	1.75	0.260	0.155	1.72	0.760	0.64	0.375
240	2.00	0.260	0.200	1.94	1.10	1.00	0.562
400	2.250	0.320	0.260	2.20	1.10	1.155	0.562

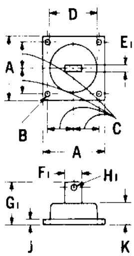
I_O Output Current	E_2 DIA	F_1 MAX	F_2 MAX	G	H THREAD	J MAX	K MAX
80	0.281	2.25	6.25	0.125	10-32	0.500	0.570
160	0.343	3.0	8.10	0.375	¾-16 UNF	1.00	1.10
240	0.531	3.50	8.10	0.375	¾-16 UNF	1.00	1.10
400	0.562	3.72	8.10	0.375	¾-16 UNF	1.00	1.10

Dimensions — Inches

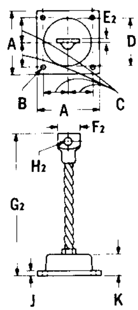
I_O Output Current	A	B DIA	C MAX	D MAX DIA	E_1 MAX	E_2 MAX	F_1 MAX
160	2.25	0.203	0.880	1.720	0.260	0.155	0.760
240	3.00	0.281	1.255	2.100	0.260	0.200	1.100
400	3.00	0.281	1.255	2.200	0.320	0.260	1.100
650	3.25	0.281	1.380	2.885	0.500	—	1.30

I_O Output Current	F_2 MAX	G_1 MAX	G_2 MAX	H_1 DIA	H_2 DIA	J MAX	K MAX
160	0.64	1.9	7.10	0.375	0.343	0.260	1.00
240	1.00	2.50	6.90	0.562	0.531	0.260	1.00
400	1.155	2.70	6.90	0.562	0.562	0.260	1.00
650	—	2.50	—	0.562	—	0.260	1.00

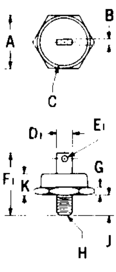
CASE 103



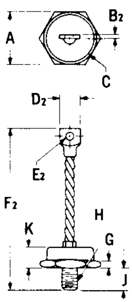
CASE 104



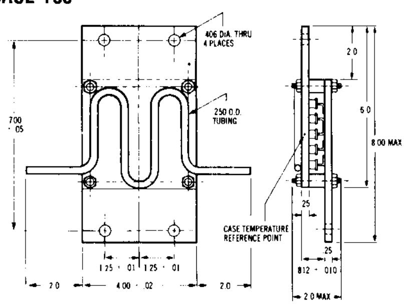
CASE 101



CASE 102



CASE 105



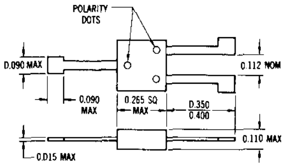
COLOR-CODED POLARITY DOTS:

Y = AC INPUT

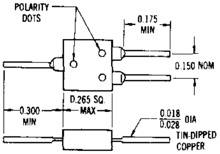
R = +DC OUTPUT

(NO MARK) = −DC OUTPUT

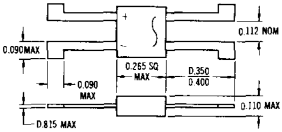
CASE 106



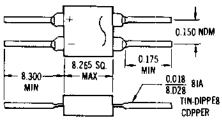
CASE 107



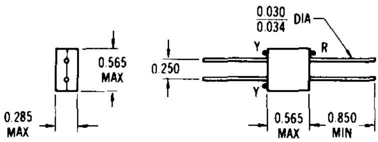
CASE 108



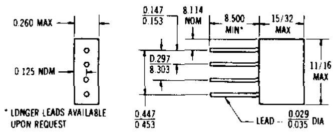
CASE 109



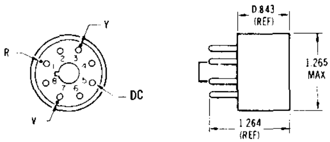
CASE 110



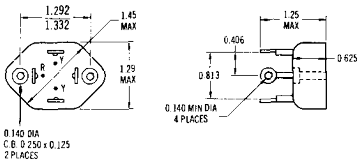
CASE 111



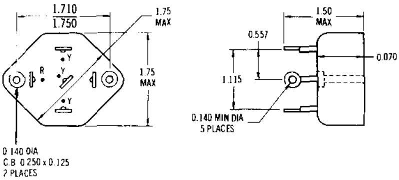
CASE 112



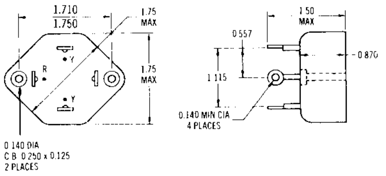
CASE 113



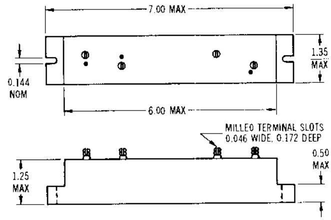
CASE 114



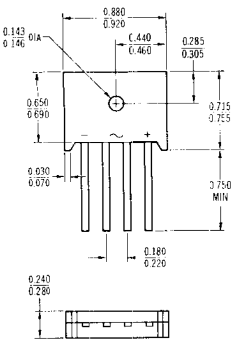
CASE 115



CASE 116

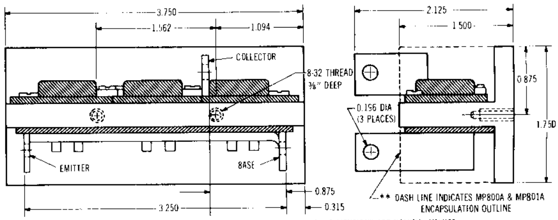


CASE 117



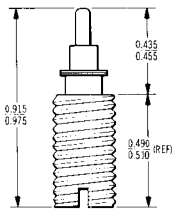
LEAD PATTERN CENTERED
LEADS MUST FIT INTO
0.055 MIN. DIA. HOLE

CASE 118

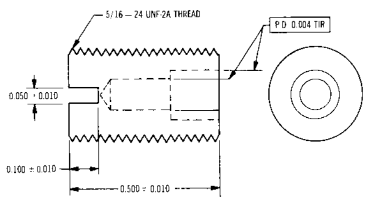


ALL DIMENSIONS ARE NOMINAL VALUES
COLLECTOR IS ELECTRICALLY ISOLATED FROM HEAT SINK CHASSIS

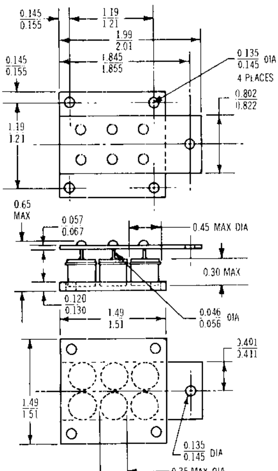
CASE 120



CASE 120, 121 ADAPTER DETAIL



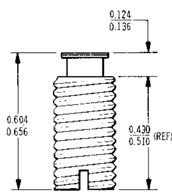
CASE 119



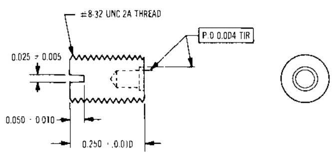
HEAT SINK MAT'L: AL ALLOY 3003
WITH NICKEL PLATING

WEIGHT 30 GRAMS (APPROX)

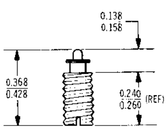
CASE 121



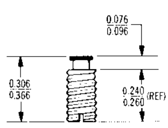
CASE 122, 123, 124 ADAPTER DETAIL



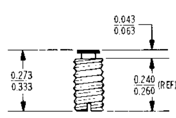
CASE 122



CASE 123



CASE 124



SILICON ZENER DIODES and CURRENT REGULATORS

THE FOLLOWING ZENER DIODES ARE INCLUDED IN THIS SECTION

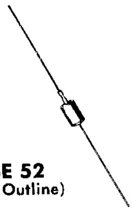
1N2163
1N2163A
1N2164
1N2164A
1N2165
1N2165A
1N2166
1N2166A
1N2167
1N2167A
1N2168
1N2168A
1N2169
1N2169A
1N2170
1N2170A
1N2171
1N2171A
1N5221
thru
1N5281

CURRENT REGULATORS

1N5283
thru
1N5314

1N2163, A thru 1N2171, A

750 mW
9.4 V



CASE 52
(DO-13 Outline)

750 Milliwatt, 9.4 volt reference diodes designed for long-term voltage stability in applications requiring stable, reliable operation under severe environmental conditions.

MAXIMUM RATINGS

Junction and Storage Temperature: -65°C to +200°C

DC Power Dissipation: 750 Milliwatts at 25°C Ambient

ELECTRICAL CHARACTERISTICS

(at I_{ZT} = 10 mA & T_A = 25°C unless otherwise specified)

V_Z = 9.4 Volts ±0.4 V (±0.2 V Suffix "A") @ I_{ZT} = 10 ma (Note 1)				
JEDEC Number	Max Voltage Change (Note 2) ΔV_Z (Volts)	Test Temperatures °C	Temperature Coefficient For Reference %/°C	Max Dynamic Impedance (Note 3) Z_{ZT} (Ohms)
1N2163, A	0.033	0, +25, +70	0.005	
1N2164, A	0.086	-55, 0, +25, +75, +125	0.005	
1N2165, A	0.115	-55, 0, +25, +75, +125, +185	0.005	
1N2166, A	0.007	0, +25, +70	0.001	15
1N2167, A	0.017	-55, 0, +25, +75, +125	0.001	
1N2168, A	0.023	-55, 0, +25, +75, +125, +185	0.001	
1N2169, A	0.004	0, +25, +70	0.0005	
1N2170, A	0.009	-55, 0, +25, +75, +125	0.0005	
1N2171, A	0.012	-55, 0, +25, +75, +125, +185	0.0005	

1N2163, A thru 1N2171, A (continued)

MECHANICAL CHARACTERISTICS

CASE: Welded, hermetically sealed, metal and glass.
FINISH: All external surfaces are corrosion resistant and leads readily solderable.
POLARITY: Cathode end indicated by diode symbol. When operated as a reference diode, the cathode end will be positive with respect to anode end.
WEIGHT: 1.5 grams (approx).
MOUNTING POSITION: Any.

TEMPERATURE COMPENSATED REFERENCE DIODES

Temperature compensated reference diodes are made possible by taking advantage of the differing thermal characteristics of forward and reverse biased silicon PN junctions. A forward biased junction has a negative temperature coefficient of approximately 2.0 millivolts/°C. Reverse biased junctions above 5.0 volts have a positive temperature coefficient and therefore it is possible by judicious selection of combinations of forward and reverse biased junctions to obtain a device which shows a very low temperature coefficient due to cancellation. Because of the differing impedance versus temperature characteristics of the junctions involved, optimum temperature stability is obtained by operating in the zener current range at which the temperature coefficient is a minimum.

Further information, including a method of effective impedance cancellation in a bridge circuit for ultra-stable reference supplies, is contained in the Motorola Zener Diode Handbook. The handbook, containing valuable theory, design, and application information, is available from your distributor.

NOTE 1 – Voltage-Current Relationship

Because of device impedance, the reference voltage will vary with changes in zener current. These variations can be minimized by driving the device from a constant current source.

NOTE 2 – Voltage Variation (ΔV_Z) and Temperature Coefficient

All Motorola reference diodes are characterized by the "box" method. This method provides for a guaranteed maximum voltage variation (ΔV_Z in mV) over a specified temperature range, verified by tests at several points within the range. (Maximum voltage variations over the specified temperature ranges are given in the table). The design engineer now has a number (without any calculations) telling him the stability of the voltage over the temperature range of interest thus giving him the maximum flexibility as well as economy in selecting the temperature stability required.

Since reference diodes have a non-linear voltage-temperature relationship the temperature coefficients in %/°C are tabulated primarily for reference purposes.

NOTE 3 – Zener Impedance Derivation

The dynamic zener impedance, Z_{ZT}, is derived from the 60 cycle ac voltage which results when an ac current having an rms value equal to 10% of the dc zener current, I_{ZT}, is superimposed on I_{ZT}. A 100% cathode-ray tube curve trace test is used to ensure that each zener characteristic has a sharp and stable knee region.

1N5221 thru 1N5281 series (SILICON)

P_D = 500 mW
V_Z = 2.4-200 V

CASE 51
(DO-7)

500 Milliwatt surmetic 20 silicon zener diodes-a complete new series of Zener Diodes in the popular DO-7 case with higher ratings, tighter limits, better operating characteristics and a full set of designers' curves that reflect the superior capabilities of silicon-oxide-passivated junctions. All this in an axial-lead, transfer-molded plastic package offering protection in all common environmental conditions.

MAXIMUM RATINGS

Junction and Storage Temperature: −65 to +200°C

Lead Temperature not less than 1/16" from the case for 10 seconds: 230°C

DC Power Dissipation: 500 mW @ T_L = 75°C, Lead Length = ⅜"
(Derate 4.0 mW/°C above 75°C)

Surge Power: 10 Watts (Non-recurrent square wave @ PW = 8.3 ms, T_J = 55°C, Figure 16)

MECHANICAL CHARACTERISTICS

CASE: Void free, transfer molded, thermosetting plastic.

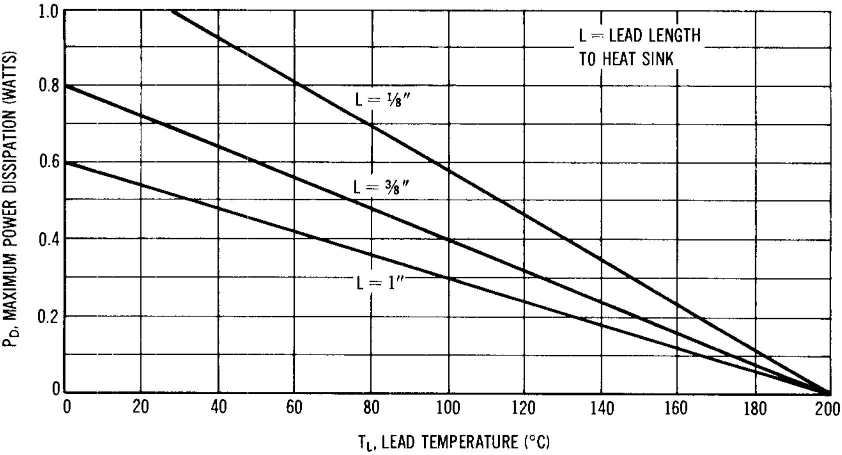
FINISH: All external surfaces are corrosion resistant. Leads are readily solderable and weldable.

POLARITY: Cathode indicated by color band. When operated in zener mode, cathode will be positive with respect to anode.

MOUNTING POSITION: Any.

WEIGHT: 0.18 gram (approximately).

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



1N5221 thru 1N5281 series (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted. Based on dc measurements at thermal equilibrium; lead length = 3/8"; thermal resistance of heat sink = 30°C/W) **V_F = 1.1 Max @ I_F = 200 mA for all types.**

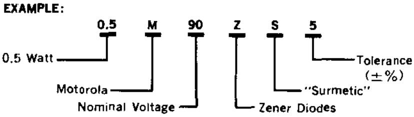
JEDEC Type No. (Note 1)	Nominal Zener Voltage V_Z @ I_{ZT} Volts (Note 2)	Test Current I_{ZT} mA	Max Zener Impedance A & B Suffix Only		Max Reverse Leakage Current				Max Zener Voltage Temp. Coeff. (A & B Suffix Only) θ_{VZ} (%/°C) (Note 3)
			Z_{ZT} @ I_{ZT} Ohms	Z_{ZK} @ I_{ZK} = 0.25 mA Ohms	A & B Suffix Only: I_R μA	@ V_R Volts A	@ V_R Volts B	Non-Suffix: I_R @ V_R Used For Suffix A μA	
1N5221	2.4	20	30	1200	100	0.95	1.0	200	-0.085
1N5222	2.5	20	30	1250	100	0.95	1.0	200	-0.085
1N5223	2.7	20	30	1300	75	0.95	1.0	150	-0.080
1N5224	2.8	20	30	1400	75	0.95	1.0	150	-0.080
1N5225	3.0	20	29	1600	50	0.95	1.0	100	-0.075
1N5226	3.3	20	28	1600	25	0.95	1.0	100	-0.070
1N5227	3.6	20	24	1700	15	0.95	1.0	100	-0.065
1N5228	3.9	20	23	1900	10	0.95	1.0	75	-0.060
1N5229	4.3	20	22	2000	5.0	0.95	1.0	50	±0.055
1N5230	4.7	20	19	1900	5.0	1.9	2.0	50	±0.030
1N5231	5.1	20	17	1600	5.0	1.9	2.0	50	±0.030
1N5232	5.6	20	11	1600	5.0	2.9	3.0	50	+0.038
1N5233	6.0	20	7.0	1600	5.0	3.3	3.5	50	+0.038
1N5234	6.2	20	7.0	1000	5.0	3.8	4.0	50	+0.045
1N5235	6.8	20	5.0	750	3.0	4.8	5.0	30	+0.050
1N5236	7.5	20	6.0	500	3.0	5.7	6.0	30	+0.058
1N5237	6.2	20	8.0	500	3.0	6.2	6.5	30	+0.062
1N5238	8.7	20	8.0	600	3.0	6.2	6.5	30	+0.065
1N5239	9.1	20	10	600	3.0	6.7	7.0	30	+0.068
1N5240	10	20	17	600	3.0	7.6	8.0	30	+0.075
1N5241	11	20	22	600	2.0	8.0	8.4	30	+0.076
1N5242	12	20	30	600	1.0	8.7	9.1	10	+0.077
1N5243	13	9.5	13	600	0.5	9.4	9.9	10	+0.079
1N5244	14	9.0	15	600	0.1	9.5	10	10	+0.082
1N5245	15	8.5	16	600	0.1	10.5	11	10	+0.082
1N5246	16	7.8	17	600	0.1	11.4	12	10	+0.083
1N5247	17	7.4	19	600	0.1	12.4	13	10	+0.084
1N5248	18	7.0	21	600	0.1	13.3	14	10	+0.085
1N5249	19	6.6	23	600	0.1	13.3	14	10	+0.086
1N5250	20	6.2	25	600	0.1	14.3	15	10	+0.086
1N5251	22	5.6	29	600	0.1	16.2	17	10	+0.087
1N5252	24	5.2	33	600	0.1	17.1	18	10	+0.088
1N5253	25	5.0	35	600	0.1	18.1	19	10	+0.089
1N5254	27	4.6	41	600	0.1	20	21	10	+0.090
1N5255	28	4.5	44	600	0.1	20	21	10	+0.091
1N5256	30	4.2	49	600	0.1	22	23	10	+0.091
1N5257	33	3.8	58	700	0.1	24	25	10	+0.092
1N5258	36	3.4	70	700	0.1	26	27	10	+0.093
1N5259	39	3.2	80	800	0.1	29	30	10	+0.094
1N5260	43	3.0	93	900	0.1	31	33	10	+0.095
1N5261	47	2.7	105	1000	0.1	34	36	10	+0.095
1N5262	51	2.5	125	1100	0.1	37	39	10	+0.096
1N5263	56	2.2	150	1300	0.1	41	43	10	+0.096
1N5264	60	2.1	170	1400	0.1	44	46	10	+0.097
1N5265	62	2.0	185	1400	0.1	45	47	10	+0.097
1N5266	68	1.8	230	1600	0.1	49	52	10	+0.097
1N5267	75	1.7	270	1700	0.1	53	56	10	+0.098
1N5268	82	1.5	330	2000	0.1	59	62	10	+0.098
1N5269	87	1.4	370	2200	0.1	65	68	10	+0.099
1N5270	91	1.4	400	2300	0.1	66	69	10	+0.099
1N5271	100	1.3	500	2600	0.1	72	76	10	+0.110
1N5272	110	1.1	750	3000	0.1	80	84	10	+0.110
1N5273	120	1.0	900	4000	0.1	86	91	10	+0.110
1N5274	130	0.95	1100	4500	0.1	94	99	10	+0.110
1N5275	140	0.90	1300	4500	0.1	101	106	10	+0.110
1N5276	150	0.85	1500	5000	0.1	108	114	10	+0.110
1N5277	160	0.80	1700	5500	0.1	116	122	10	+0.110
1N5278	170	0.74	1900	5500	0.1	123	129	10	+0.110
1N5279	180	0.68	2200	6000	0.1	130	137	10	+0.110
1N5280	190	0.66	2400	6500	0.1	137	144	10	+0.110
1N5281	200	0.65	2500	7000	0.1	144	152	10	+0.110

NOTE 1 — TOLERANCE AND VOLTAGE DESIGNATION

Tolerance designation — The JEDEC type numbers shown indicate a tolerance of ±10% with guaranteed limits on only V_Z, I_R and V_F as shown in the above table. Units with guaranteed limits on all six parameters are indicated by suffix "A" for ±10% tolerance and suffix "B" for ±5.0% units.

Non-Standard voltage designation — To designate units with zener voltages other than those assigned JEDEC numbers, the Motorola type number should be used.

EXAMPLE:



NOTE 2 — SPECIAL SELECTIONS AVAILABLE INCLUDE:

1 — Nominal zener voltages between those shown.

2 — Matched sets: (Standard Tolerances are ±5.0%, ±2.0%, ±1.0%)

a. Two or more units for series connection with specified tolerance on total voltage. Series matched sets make zener voltages in excess of 200 volts possible as well as providing lower temperature coefficients, lower dynamic impedance and greater power handling ability.

b. Two or more units matched to one another with any specified tolerance.

3 — Tight voltage tolerances: 1.0%, 2.0%, 3.0%.

NOTE 3 — TEMPERATURE COEFFICIENT (θ_{VZ})

Test conditions for temperature coefficient are as follows:

a. I_{ZT} = 7.5 mA, T_1 = 25°C,
T_2 = 125°C (1N5221A, B thru 1N5242A, B.)

b. I_{ZT} = Rated I_{ZT}, T_1 = 25°C,
T_2 = 125°C (1N5243A, B thru 1N5281A, B.)

Device to be temperature stabilized with current applied prior to reading breakdown voltage at the specified ambient temperature.

1N5221 thru 1N5281 series (continued)

TYPICAL REVERSE CHARACTERISTICS FOR SELECTED ZENER DIODES

Curves marked T_A were obtained from dc measurements at thermal equilibrium; lead length = 3/8"; thermal resistance of heat sink = 30°C/W.
Curves marked T_J were obtained from pulse tests; mounting conditions are not a factor.

$V_{Z(Nominal)}$ = 3.3 Volts

FIGURE 2

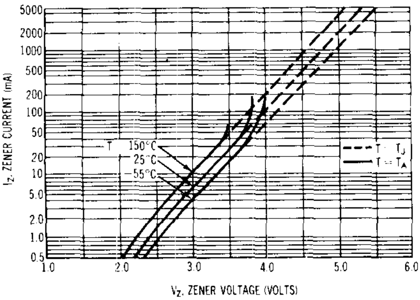
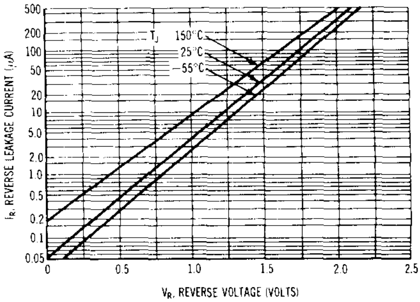


FIGURE 3



$V_{Z(Nominal)}$ = 5.1 Volts

FIGURE 4

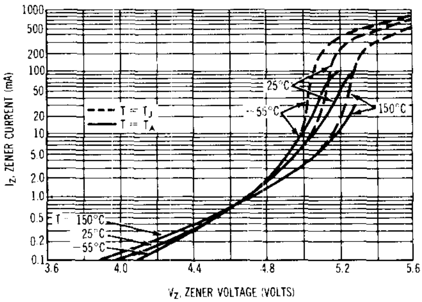
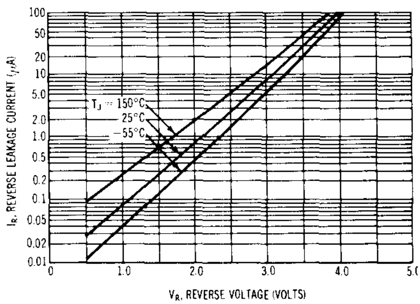


FIGURE 5



$V_{Z(Nominal)}$ = 27 Volts

FIGURE 6

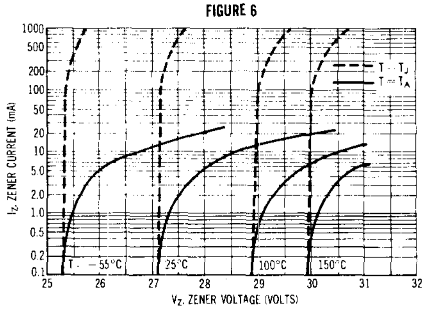
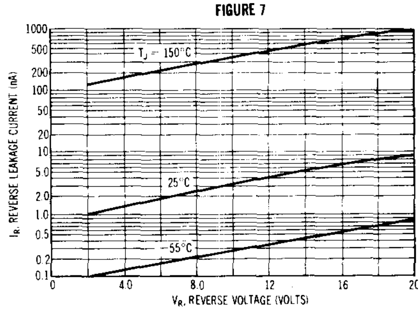


FIGURE 7



1N5221 thru 1N5281 series (continued)

TEMPERATURE COEFFICIENTS AND VOLTAGE REGULATION

(90% of the units are in the ranges indicated)

FIGURE 8 — RANGE FOR UNITS TO 12 VOLTS

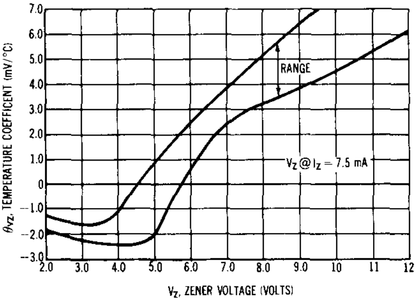


FIGURE 9 — RANGE FOR UNITS 12 TO 200 VOLTS

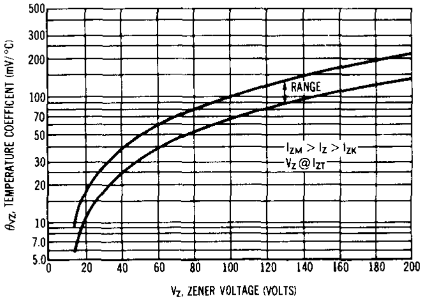


FIGURE 10 — EFFECT OF ZENER CURRENT

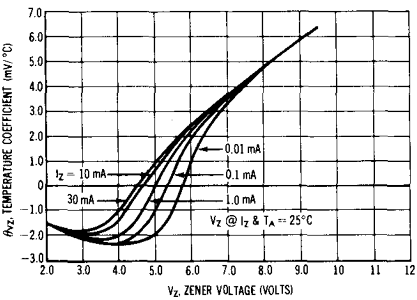
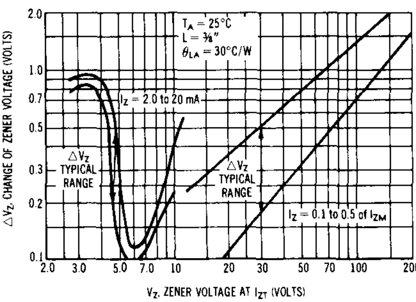


FIGURE 11 — VOLTAGE REGULATION



TYPICAL ZENER IMPEDANCE

FIGURE 12 — EFFECT OF ZENER CURRENT

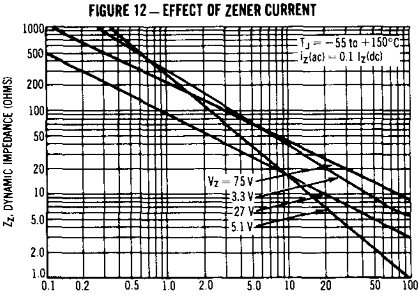
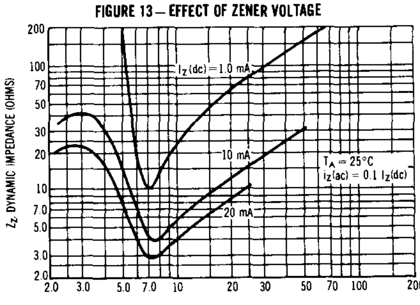


FIGURE 13 — EFFECT OF ZENER VOLTAGE



1N5221 thru 1N5281 Series (continued)

FIGURE 14 — TYPICAL THERMAL RESPONSE

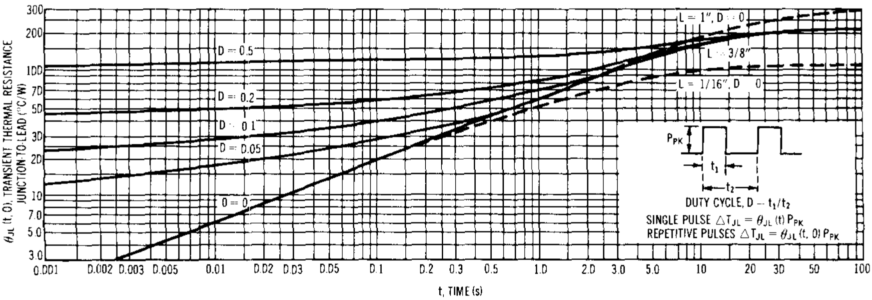


FIGURE 15 — TYPICAL THERMAL RESISTANCE

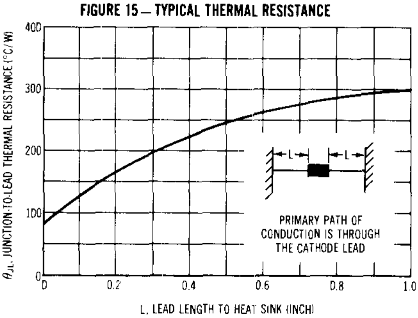
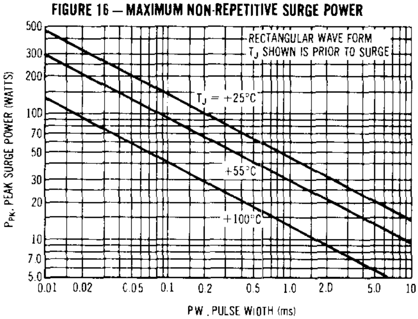


FIGURE 16 — MAXIMUM NON-REPETITIVE SURGE POWER



APPLICATION NOTE

Since the actual voltage available from a given zener diode is temperature dependent, it is necessary to determine junction temperature under any set of operating conditions, in order to calculate its value. The following procedure is recommended:

Lead Temperature, T_L, should be determined from:

$$T_L = \theta_{LA} P_D + T_A$$

θ_{LA} is the lead-to-ambient thermal resistance and P_D is the power dissipation. θ_{LA} is generally 30-40°C/W for the various clips and tie points in common use and for printed circuit board wiring.

Junction Temperature, T_J, may be found from:

$$T_J = T_L + \Delta T_{JL}$$

ΔT_{JL} is the increase in junction temperature above the lead temperature and may be found from Figure 14 for a train of power pulses or from Figure 15 for dc power.

For worst-case design, using expected limits of I_Z, limits of P_D and the extremes of T_J (ΔT_J) may be estimated. Changes in voltage, V_Z, can then be found from:

$$\Delta V = \theta_{VZ} \Delta T_J$$

θ_{VZ}, the zener voltage temperature coefficient, is found from Figures 8, 9, and 10.

Under high power-pulse operation, the zener voltage will vary with time and may also be affected significantly by the zener resistance. For best regulation, use short leads, especially to the cathode, and keep current excursions as low as possible.

Data of Figure 14 should not be used to compute surge capability. Surge limitations are given in Figure 16. They are lower than would be expected by considering only junction temperature, as current crowding effects cause temperatures to be extremely high in small spots resulting in device degradation should the limits of Figure 16 be exceeded.

1N5221 thru 1N5281 Series (continued)

FIGURE 17 — TYPICAL CAPACITANCE

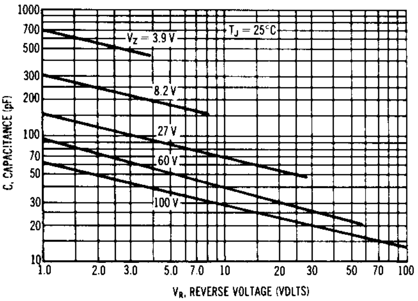


FIGURE 18 — TYPICAL FORWARD CHARACTERISTICS

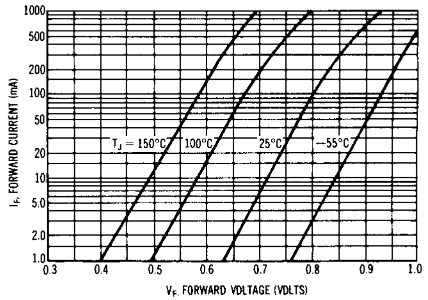


FIGURE 19 — TYPICAL NOISE DENSITY

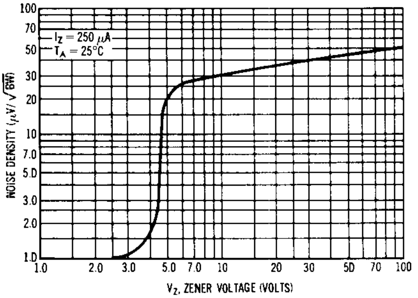
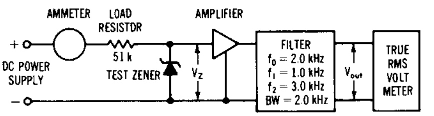


FIGURE 20 — NOISE DENSITY MEASUREMENT METHOD



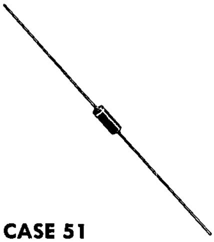
$$\text{NOISE DENSITY (VOLTS PER SQUARE ROOT BANDWIDTH)} = \frac{V_{out}}{\text{OVERALL GAIN} \sqrt{BW}}$$

WHERE: BW = FILTER BANDWIDTH (Hz)
V_{out} = OUTPUT NOISE (VOLTS RMS)

The input voltage and load resistance are high so that the zener diode is driven from a constant current source. The amplifier is low noise so that the amplifier noise is negligible compared to that of the test zener. The filter bandpass is known so that the noise density can be calculated from the formula shown. The data of Figure 19 and the formula can also be used to find noise for any system bandwidth.

1N5283 thru 1N5314

I_P = 0.22-4.7 mA min
P_D = 600 mW



CASE 51
(DO-7)

Field-effect current regulator diodes are circuit elements that provide a current essentially independent of voltage. These diodes are especially designed for maximum impedance over the operating range.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Operating Voltage (T_J = -55°C to +200°C)	POV	100	Volts
Steady State Power Dissipation @ T_L = 75°C Derate above T_L = 75°C Lead Length = 3/8" (Forward or Reverse Bias)	P_D	600 4.8	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200	°C

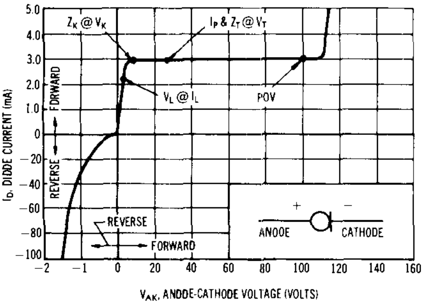
1N5283 thru 1N5314 (continued)

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Type No.	Regulator Current I_P (mA) @ V_T = 25 V nom	min	max	Minimum Dynamic Impedance @V_T = 25 V Z_T (MΩ)	Minimum Knee Impedance @V_K = 6.0 V Z_K (MΩ)	Maximum Limiting Voltage @I_L = 0.8 I_P (min) V_L (Volts)
1N5283	0.22	0.198	0.242	25.0	2.75	1.00
1N5284	0.24	0.216	0.264	19.0	2.35	1.00
1N5285	0.27	0.243	0.297	14.0	1.95	1.00
1N5286	0.30	0.270	0.330	9.0	1.60	1.00
1N5287	0.33	0.297	0.363	6.6	1.35	1.00
1N5288	0.39	0.351	0.429	4.10	1.00	1.05
1N5289	0.43	0.387	0.473	3.30	0.870	1.05
1N5290	0.47	0.423	0.517	2.70	0.750	1.05
1N5291	0.56	0.504	0.616	1.90	0.560	1.10
1N5292	0.62	0.558	0.682	1.55	0.470	1.13
1N5293	0.68	0.612	0.748	1.35	0.400	1.15
1N5294	0.75	0.675	0.825	1.15	0.335	1.20
1N5295	0.82	0.738	0.902	1.00	0.290	1.25
1N5296	0.91	0.819	1.001	0.880	0.240	1.29
1N5297	1.00	0.900	1.100	0.800	0.205	1.35
1N5298	1.10	0.990	1.210	0.700	0.180	1.40
1N5299	1.20	1.08	1.32	0.640	0.155	1.45
1N5300	1.30	1.17	1.43	0.580	0.135	1.50
1N5301	1.40	1.26	1.54	0.540	0.115	1.55
1N5302	1.50	1.35	1.65	0.510	0.105	1.60
1N5303	1.60	1.44	1.76	0.475	0.092	1.65
1N5304	1.80	1.62	1.98	0.420	0.074	1.75
1N5305	2.00	1.80	2.20	0.395	0.061	1.85
1N5306	2.20	1.98	2.42	0.370	0.052	1.95
1N5307	2.40	2.16	2.64	0.345	0.044	2.00
1N5308	2.70	2.43	2.97	0.320	0.035	2.15
1N5309	3.00	2.70	3.30	0.300	0.029	2.25
1N5310	3.30	2.97	3.63	0.280	0.024	2.35
1N5311	3.60	3.24	3.96	0.265	0.020	2.50
1N5312	3.90	3.51	4.29	0.255	0.017	2.60
1N5313	4.30	3.87	4.73	0.245	0.014	2.75
1N5314	4.70	4.23	5.17	0.235	0.012	2.90

1N5283 thru 1N5314 (continued)

FIGURE 1 — TYPICAL CURRENT REGULATOR CHARACTERISTICS



SYMBOLS AND DEFINITIONS

I_D — Diode Current.

I_L — Limiting Current: 80% of I_P minimum used to determine Limiting voltage, V_L.

I_P — Pinch-off Current: Regulator current at specified Test Voltage, V_T.

POV — Peak Operating Voltage: Maximum voltage to be applied to device.

θ_I — Current Temperature Coefficient.

V_{AK} — Anode-to-cathode Voltage.

V_K — Knee Impedance Test Voltage: Specified voltage used to establish Knee Impedance, Z_K.

V_L — Limiting Voltage: Measured at I_L. V_L, together with Knee AC Impedance, Z_K, indicates the Knee characteristics of the device.

V_T — Test Voltage: Voltage at which I_P and Z_T are specified.

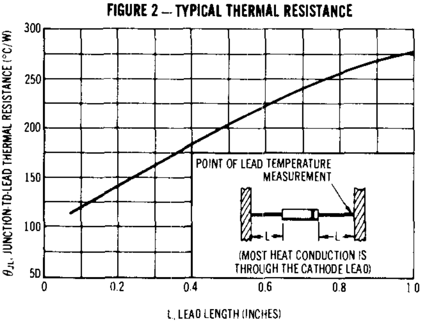
Z_K — Knee AC Impedance at Test Voltage: To test for Z_K, a 90 Hz signal v_K with RMS value equal to 10% of test voltage, V_K, is superimposed on V_K:

$$Z_K = v_K / i_K$$

where i_K is the resultant ac current due to v_K.
To provide the most constant current from the diode, Z_K should be as high as possible; therefore, a minimum value of Z_K is specified.

Z_T — AC Impedance at Test Voltage: Specified as a minimum value. To test for Z_T, a 90 Hz signal with RMS value equal to 10% of Test Voltage, V_T, is superimposed on V_T.

FIGURE 2 — TYPICAL THERMAL RESISTANCE



APPLICATION NOTE

As the current available from the diode is temperature dependent, it is necessary to determine junction temperature, T_J, under specific operating conditions to calculate the value of the diode current. The following procedure is recommended:

Lead Temperature, T_L, shall be determined from:

$$T_L = \theta_{LA} P_D$$

where θ_{LA} is lead-to-ambient thermal resistance
and P_D is power dissipation.
θ_{LA} is generally 30-40°C/W for the various clips and tie points in common use, and for printed circuit-board wiring.

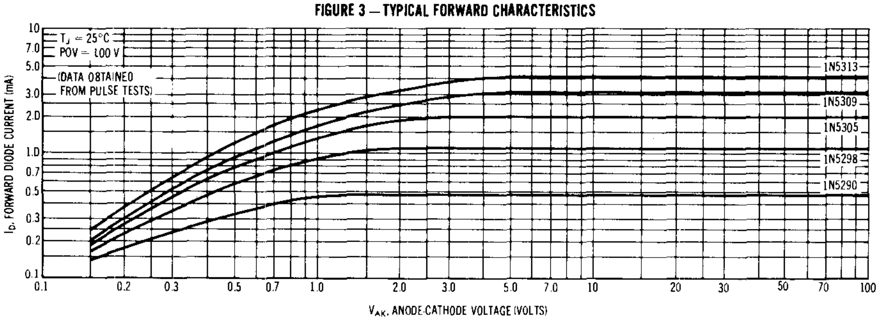
Junction Temperature, T_J, shall be calculated from:

$$T_J = T_L + \theta_{JL} P_D$$

where θ_{JL} is taken from Figure 2.

For circuit design limits of V_{AK}, limits of P_D may be estimated and extremes of T_J may be computed. Using the information on Figures 4 and 5, changes in current may be found. To improve current regulation, keep V_{AK} low to reduce P_D and keep the leads short, especially the cathode lead, to reduce θ_{JL}.

FIGURE 3 — TYPICAL FORWARD CHARACTERISTICS



1N5283 thru 1N5314 (continued)

FIGURE 4 — TEMPERATURE COEFFICIENT

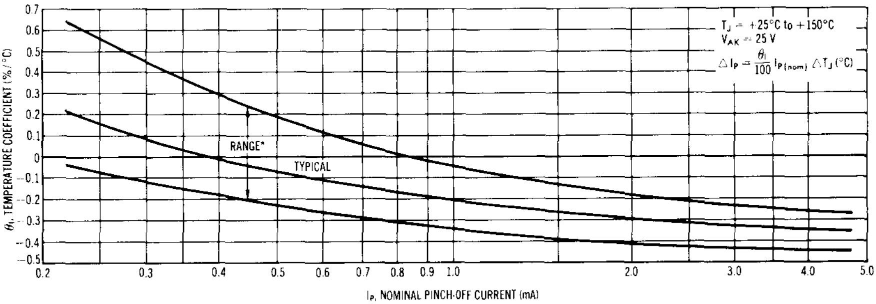


FIGURE 5 — TEMPERATURE COEFFICIENT

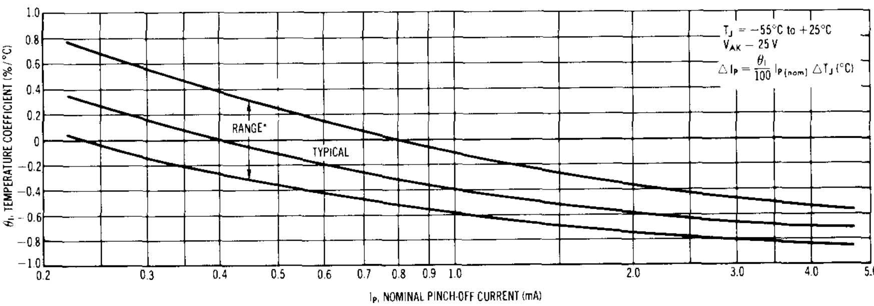
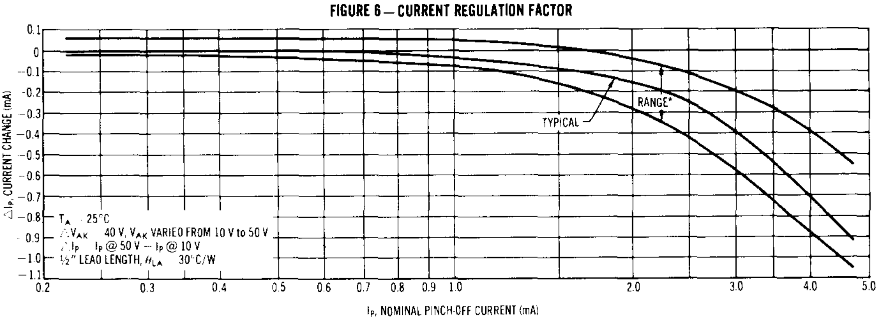


FIGURE 6 — CURRENT REGULATION FACTOR



*90% of the units will be in the ranges shown.

[redacted]

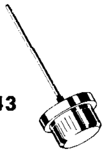
SILICON RECTIFIERS

THE FOLLOWING RECTIFIERS ARE INCLUDED IN THIS SECTION

1N3491	1N3909	MR325	MR842
1N3492	1N3910	MR326	MR844
1N3493	1N3911	MR327	MR846
1N3494	1N3912	MR328	MR880
1N3495	1N3913	MR330	MR881
1N3879	1N4001	MR331	MR882
1N3880	1N4002	MR810	MR884
1N3881	1N4003	MR811	MR886
1N3882	1N4004	MR812	MR890
1N3883	1N4005	MR814	MR891
1N3889	1N4006	MR816	MR892
1N3890	1N4007	MR830	MR894
1N3891	1N4933	MR831	MR896
1N3892	1N4934	MR832	MR1366
1N3893	1N4935	MR833	MR1376
1N3899	1N4936	MR834	MR1386
1N3900	1N4937	MR835	MR1396
1N3901	MR322	MR836	
1N3902	MR323	MR840	
1N3903	MR324	MR841	

1N3491 thru 1N3495 (SILICON)
(MR322 thru MR326)
MR327, MR328, MR330, MR331

I_O = 25 A
V_R — to 1000 V



CASE 43
(DO-21)

Medium-current silicon rectifiers – compact, highly efficient silicon rectifiers for medium-current applications.

MAXIMUM RATINGS

Rating	Symbol	1N3491 MR322	1N3492 MR323	1N3493 MR324	1N3494 MR325	1N3495 MR326	MR327	MR328	MR330	MR331	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	$V_{RM(rep)}$ $V_{RM(wkg)}$ V_R	50	100	200	300	400	500	600	800	1000	Volts
Non-Repetitive Peak Reverse Voltage (halfwave, single phase, 60 cycle peak)	$V_{RM(non-rep)}$	100	200	300	400	500	600	720	1000	1200	Volts
RMS Reverse Voltage	V_r	35	70	140	210	280	350	420	560	700	Volts
Average Rectified Forward Current (single phase, resistive load, 60 Hz, see Figure 3) T_C = 130°C	I_O	← 25 →									Amperes
Non-Repetitive Peak Surge Current (surge applied at rated load conditions, see Figure 5)	$I_{FM(surge)}$	← 300 (for 1/2 cycle) →									Amperes
I^2t Rating (non-repetitive, for t greater than 1 ms and less than 8.3 ms)	I^2t	← 375 →									$A_{(rms)}^2$ sec
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +175 →									°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.2	°C/Watt

MECHANICAL CHARACTERISTICS

CASE: Welded, hermetically sealed construction.

FINISH: All external surfaces corrosion-resistant and the terminal lead is readily solderable.

POLARITY: CATHODE TO CASE (reverse polarity units are available upon request and are designated by an "R" suffix i.e. MR327R or 1N3491R).

MOUNTING POSITIONS: Any.

1N3491 thru 1N3495 (continued)

ELECTRICAL CHARACTERISTICS

Characteristic and Conditions	Symbol	Max	Unit
Full Cycle Average Forward Voltage Drop (rated I_O and V_r, single phase, 60 Hz, T_C = 150°C)	$V_{F(AV)}$	0.6	Volts
Instantaneous Forward Voltage Drop (i_F = 100 Amps, T_J = 25°C)	V_F	1.5	Volts
Full Cycle Average Reverse Current (rated I_O and V_r, single phase, 60 Hz, T_C = 150°C)	$I_{R(AV)}$		mA
1N3491/MR322		10	
1N3492/MR323		10	
1N3493/MR324		8	
1N3494/MR325		6	
1N3495/MR326		4	
MR327		3	
MR328		2.5	
MR330		2	
MR331		1.5	
DC Reverse Current (Rated V_R, T_C = 25°C)	I_R	1.0	mA

FIGURE 1 — MAXIMUM FORWARD VOLTAGE DROP

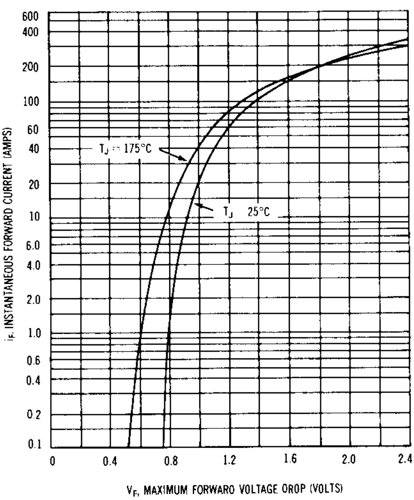
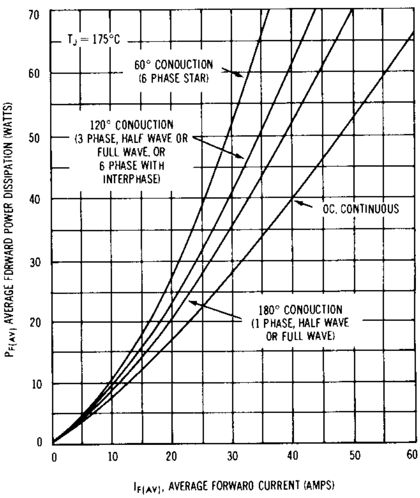


FIGURE 2 — MAXIMUM FORWARD POWER DISSIPATION



1N3491 thru 1N3495 (continued)

FIGURE 3 — MAXIMUM CURRENT RATINGS

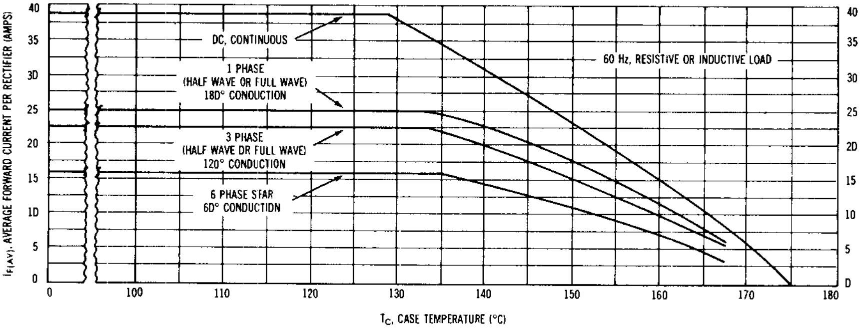


FIGURE 4 — MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE

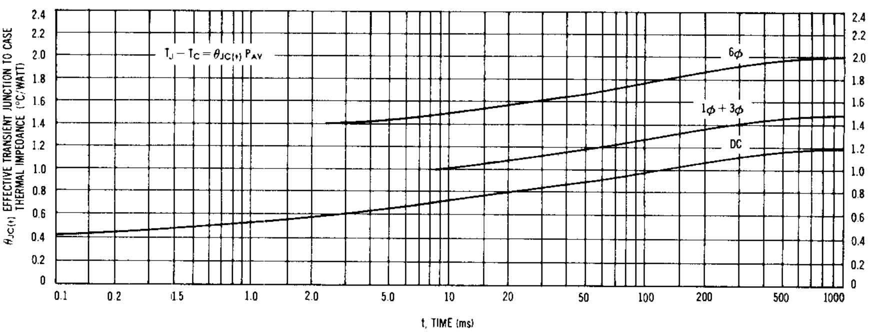
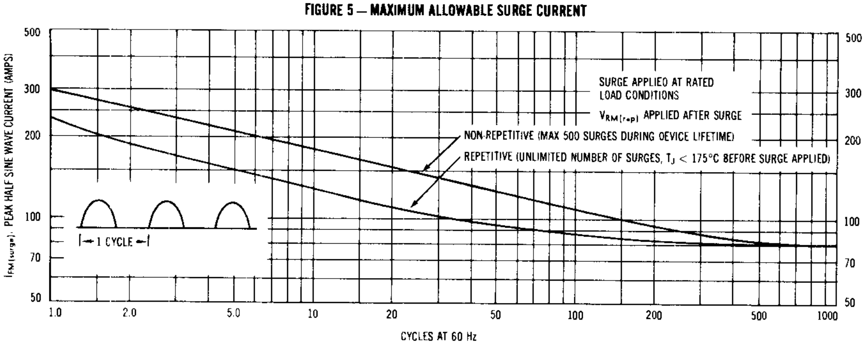


FIGURE 5 — MAXIMUM ALLOWABLE SURGE CURRENT



1N3491 thru 1N3495 (continued)

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 6 — RECTIFICATION EFFICIENCY

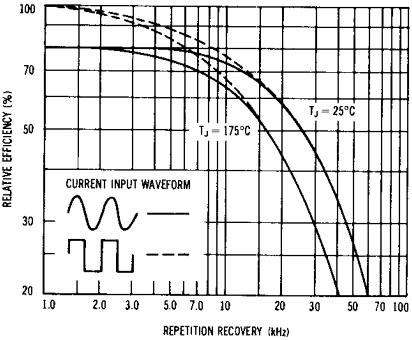


FIGURE 7 — REVERSE RECOVERY TIME

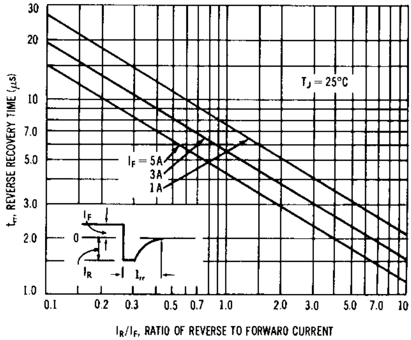


FIGURE 8 — JUNCTION CAPACITANCE

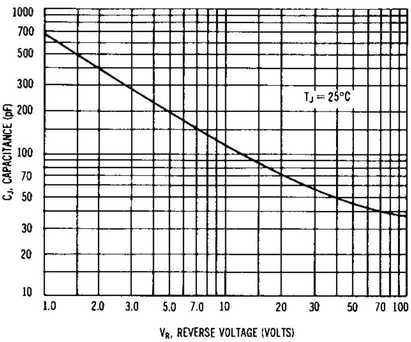
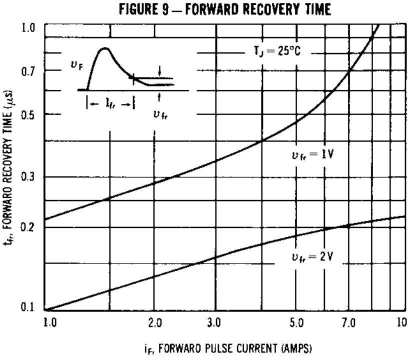
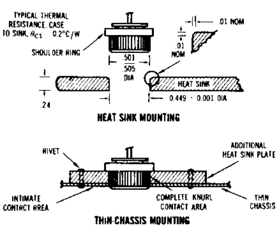


FIGURE 9 — FORWARD RECOVERY TIME





MOUNTING PROCEDURES

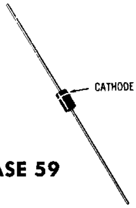
Motorola MR322-MR331 and 1N3491-1N3495 rectifiers are designed to be press-fitted in a heat sink in order to attain full device ratings. Recommended procedures for this type of mounting are as follows:

1. Drill a hole in the heat sink 0.499 ± .001 inch in diameter.
2. Break the hole edge as shown to prevent shearing off the knurled edge of the rectifier when it is pressed into the hole.
3. The depth and width of the break should be 0.010 inch maximum to retain maximum heat sink surface contact.
4. To prevent damage to the rectifier during press-in, the pressing force should be applied only on the shoulder ring of the rectifier case as shown in the figure.
5. The pressing force should be applied evenly about the shoulder ring to avoid tilting or canting of the rectifier case in the hole during the press-in operation. Also, the use of a light industrial lubricant will be of considerable aid.

NOTE:
Refer to Motorola brochure PR-104 for additional suggested mounting methods, examples and information.

1N4001 thru 1N4007

$I_O = 1$ A
$V_R = 50\text{-}1000$ V



CASE 59

Surmetic rectifiers, subminiature size, axial lead mounted rectifiers for general purpose low-power applications.

MAXIMUM RATINGS

Rating	Symbol	1N4001	1N4002	1N4003	1N4004	1N4005	1N4006	1N4007	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	$V_{RM(rep)}$ $V_{RM(wkg)}$ V_R	50	100	200	400	600	800	1000	Volts
Non-Repetitive Peak Reverse Voltage (halfwave, single phase, 60 Hz peak)	$V_{RM(non-rep)}$	60	120	240	480	720	1000	1200	Volts
RMS Reverse Voltage	V_r	35	70	140	280	420	560	700	Volts
Average Rectified Forward Current (single phase, resistive load, 60 Hz, see Figure 6, $T_A = 75°C$)	I_O	1.0							Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions, see Figure 2)	$I_{FM(surge)}$	30 (for 1 cycle)							Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175							°C

ELECTRICAL CHARACTERISTICS

Characteristic and Conditions	Symbol	Max	Unit
Maximum Instantaneous Forward Voltage Drop ($i_F = 1.0$ Amp. $T_J = 25°C$) Figure 1	V_F	1.1	Volts
Maximum Full-Cycle Average Forward Voltage Drop ($I_O = 1.0$ Amp, $T_L = 75°C$, 1 inch leads)	$V_{F(AV)}$	0.8	Volts
Maximum Reverse Current (rated dc voltage) $T_J = 25°C$ $T_J = 100°C$	I_R	0.01 0.05	mA
Maximum Full-Cycle Average Reverse Current ($I_O = 1.0$ Amp. $T_L = 75°C$, 1 inch leads)	$I_{R(AV)}$	0.03	mA

MECHANICAL CHARACTERISTICS

CASE: Void free, Transfer Molded

MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES: 350°C, 3/8" from case for 10 seconds at 5 lbs. tension

FINISH: All external surfaces are corrosion-resistant, leads are readily solderable

POLARITY: Cathode indicated by color band

WEIGHT: 0.40 Grams (approximately)

1N4001 thru 1N4007 (continued)

FIGURE 1 — FORWARD VOLTAGE

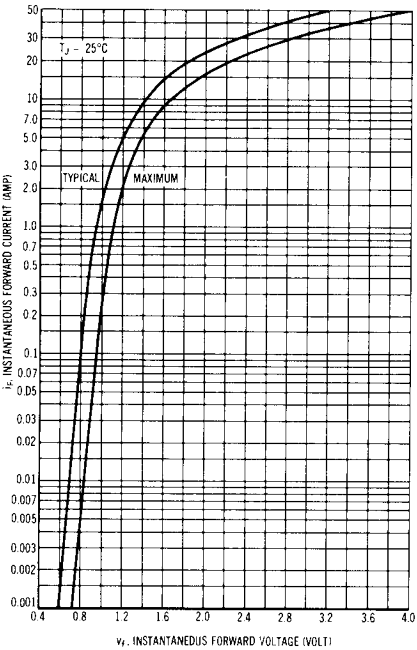


FIGURE 2 — MAXIMUM SURGE CAPABILITY

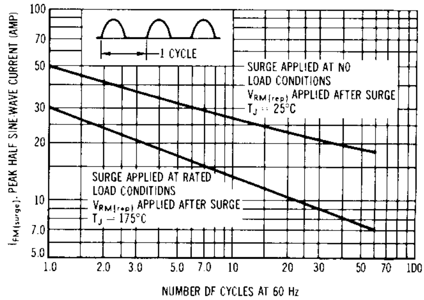


FIGURE 3 — FORWARD VOLTAGE TEMPERATURE COEFFICIENT

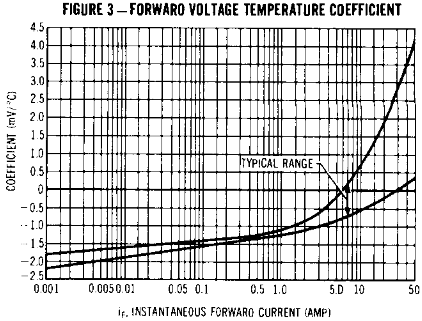
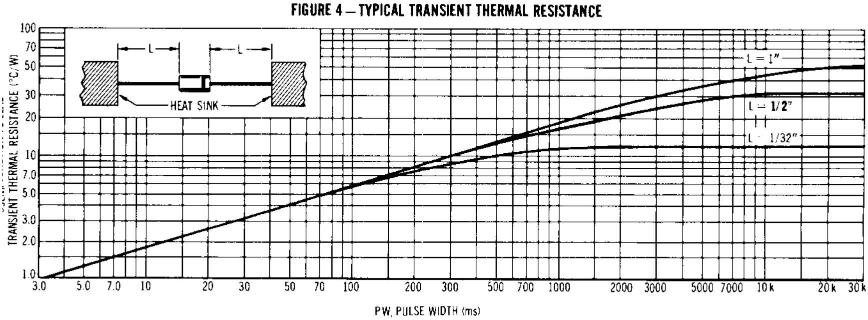


FIGURE 4 — TYPICAL TRANSIENT THERMAL RESISTANCE



FOR $\theta_{JL(t)}$ VALUES AT PULSE WIDTHS LESS THAN 3.0 ms, THE ABOVE CURVE CAN BE EXTRAPOLATED DOWN TO 10 μs AT A CONTINUING SLOPE OF 1/2

1N4001 thru 1N4007 (continued)

CURRENT DERATING DATA

FIGURE 5 — LEAD TEMPERATURE DERATING (DC ONLY)

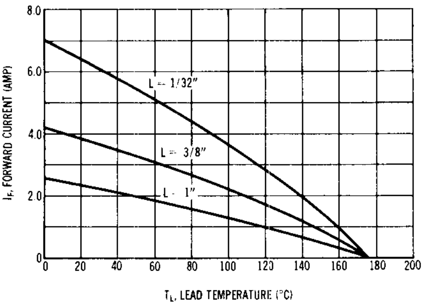


FIGURE 6 — RESISTIVE,INDUCTIVE LOADS

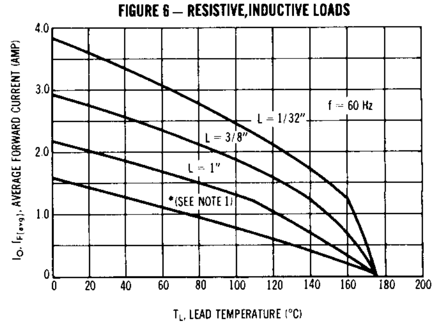


FIGURE 7 — CAPACITIVE LOADS

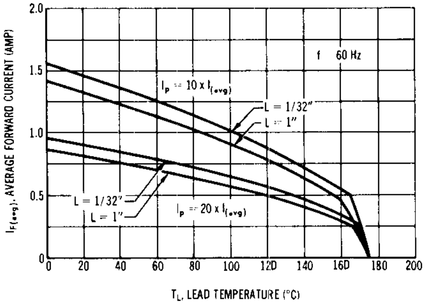
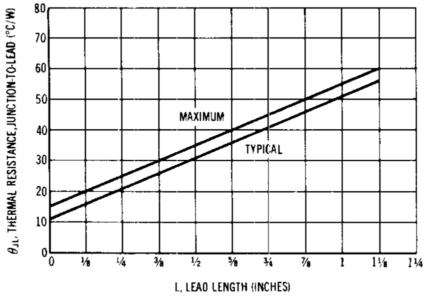


FIGURE 8 — STEADY-STATE THERMAL RESISTANCE

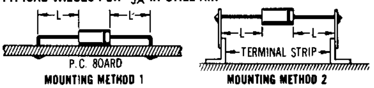


NOTES

NOTE 1

Data shown for thermal resistance junction-to-ambient (θ_{JA}) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

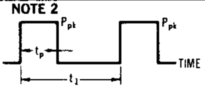
TYPICAL VALUES FOR θ_{JA} IN STILL AIR



MOUNTING METHOD	LEAD LENGTH, L (IN.) 1/32	3/8	1	θ_{JA}
1	—	75	85	°C/W
2	55	72	85	°C/W

***Using Mounting Method 1 or 2 with L = 1" the curve marked * in Figure 6 can be used for 60 Hz half-wave resistive/inductive load (Rating vs. Ambient Temperature). The abscissa of Figure 6 then indicates T_A in °C.**

NOTE 2



DUTY CYCLE, $D = t_p/t_1$
PEAK POWER, P_{pk}, is peak of an equivalent square power pulse.

To determine maximum junction temperature of the diode in a given situation, the following procedure is recommended:

The temperature of the lead should be measured using a thermocouple placed on the lead as close as possible to the tie point. The thermal mass connected to the tie point is normally large enough so that it will not significantly respond to heat surges generated in the diode as a result of pulsed operation once steady-state conditions are achieved. Using the measured value of T_L, the junction temperature may be determined by:

$$T_J = T_L + \Delta T_{JL}$$

where ΔT_{JL} is the increase in junction temperature above the lead temperature. It may be determined by:

$$\Delta T_{JL} = P_{pk}\left[\theta_{JL(\infty)} \cdot D + (1 - D) \cdot \theta_{JL(t_1 + t_p)} + \theta_{JL(t_p)} - \theta_{JL(t_1)}\right]$$

where $\theta_{JL(t)}$ = value of transient thermal resistance at time t, i.e.:

$\theta_{JL(t_1+t_p)}$ = value of $\theta_{JL(t)}$ at time t_1+t_p

$\theta_{JL(t_p)}$ = value of $\theta_{JL(t)}$ at end of pulse width t_p

$\theta_{JL(t_1)}$ = value of $\theta_{JL(t)}$ at time t_1

1N4001 thru 1N4007 (continued)

TYPICAL DYNAMIC CHARACTERISTICS

FIGURE 9 — FORWARD RECOVERY TIME

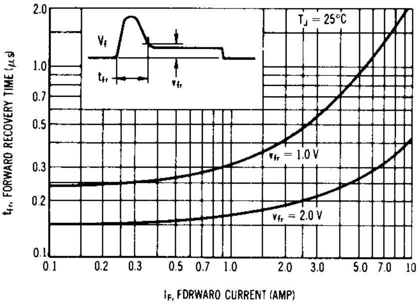


FIGURE 10 — REVERSE RECOVERY TIME

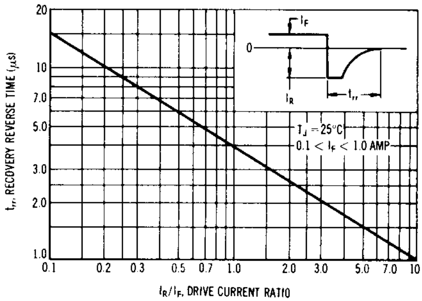


FIGURE 11 — RECTIFICATION WAVEFORM EFFICIENCY

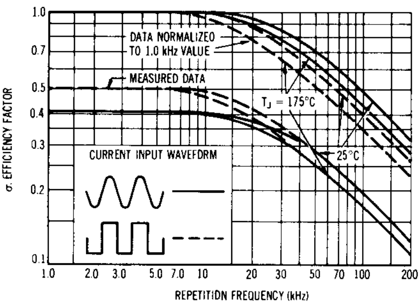
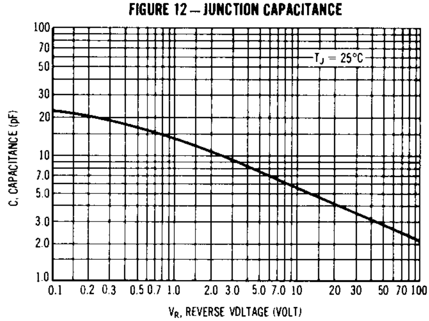
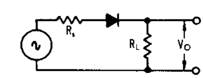


FIGURE 12 — JUNCTION CAPACITANCE



RECTIFIER EFFICIENCY NOTE

FIGURE 13 — SINGLE-PHASE HALF-WAVE RECTIFIER CIRCUIT



The rectification efficiency factor σ shown in Figure 11 was calculated using the formula:

$$\sigma = \frac{P_{dc}}{P_{rms}} = \frac{\frac{V^2_{O(dc)}}{R_L}}{\frac{V^2_{O(rms)}}{R_L}} \cdot 100\% = \frac{V^2_{O(dc)}}{V^2_{O(ac)} + V^2_{O(dc)}} \cdot 100\% \quad (1)$$

For a sine wave input $V_m \sin(\omega t)$ to the diode, assumed lossless, the maximum theoretical efficiency factor becomes:

$$\sigma_{(sine)} = \frac{\frac{V^2_m}{\pi^2 R_L}}{\frac{V^2_m}{4R_L}} \cdot 100\% = \frac{4}{\pi^2} \cdot 100\% = 40.6\% \quad (2)$$

For a square wave input of amplitude V_m, the efficiency factor becomes:

$$\sigma_{(square)} = \frac{\frac{V^2_m}{2R_L}}{\frac{V^2_m}{R_L}} \cdot 100\% = 50\% \quad (3)$$

(A full wave circuit has twice these efficiencies)

As the frequency of the input signal is increased, the reverse recovery time of the diode (Figure 10) becomes significant, resulting in an increasing ac voltage component across R_L which is opposite in polarity to the forward current, thereby reducing the value of the efficiency factor σ, as shown on Figure 11.

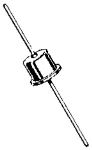
It should be emphasized that **Figure 11 shows waveform efficiency only; it does not provide a measure of diode losses.** Data was obtained by measuring the ac component of V_O with a true rms ac voltmeter and the dc component with a dc voltmeter. The data was used in Equation 1 to obtain points for Figure 11.

1N4933 thru 1N4937 (SILICON)

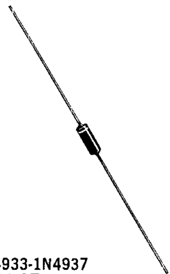
1N3879 thru 1N3883 — 1N3889 thru 1N3893
1N3899 thru 1N3903 — 1N3909 thru 1N3913
MR830 thru MR836 — MR1366, MR1376, MR1386, MR1396

I_O = 1.0-30 A
V_R = 50-600 V

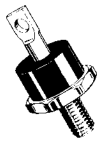
Fast recovery silicon rectifiers designed for special applications such as high frequency rectification, inverters, free-wheeling diodes, and other fast switching circuits. A complete line of rectifiers having typical recovery time of 0.1 microseconds providing high efficiency at frequencies of 250 kHz and higher.



MR830-MR836
CASE 60



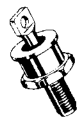
1N4933-1N4937
CASE 59



1N3899-1N3903
MR1386

1N3909-1N3913
MR1396

CASE 42
(DO-5)



1N3879-1N3883
MR1366

1N3889-1N3893
MR1376

CASE 56A (DO-4)

MAXIMUM RATINGS

I_O* Ampere	$I_{FM(surge)}$** Ampere	$V_{RM(rep)}$, $V_{RM(wkg)}$, $V_{R(Volts)}$					
		50	100	200	300	400	600
1.0	30	1N4933	1N4934	1N4935	—	1N4936	1N4937
3.0	100	MR830	MR831	MR832	—	MR834	MR836
6.0	150	1N3879	1N3880	1N3881	1N3882	1N3883	MR1366
12	200	1N3889	1N3890	1N3891	1N3892	1N3893	MR1376
20	225	1N3899	1N3900	1N3901	1N3902	1N3903	MR1386
30	300	1N3909	1N3910	1N3911	1N3912	1N3913	MR1396

* Figure 3 ** Figure 4

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max Limit	Unit
Maximum Junction Operating Temperature Range	T_J	-65 to +150	°C
Maximum Case Storage Temperature Range	T_{stg}	-65 to +175	°C

1N4933 thru 1N4937 (continued)

ELECTRICAL CHARACTERISTICS

Characteristics		Symbol	Max Limit	Unit
1N4933 thru 1N4937				
DC Forward Voltage Drop (I_F = 1.0 Adc, T_A = 25°C)		V_F	1.2	Vdc
DC Reverse Current (Rated V_R)	T_A = 25°C	I_R	5.0	µA
	T_A = 100°C		100	
MR830 thru MR836				
DC Forward Voltage Drop (I_F = 3.0 Adc, T_A = 25°C)		V_F	1.1	Vdc
DC Reverse Current (Rated V_R)	T_A = 25°C	I_R	0.05	mA
	T_A = 100°C		2.5	
1N3879 thru 1N3883, MR1366				
DC Forward Voltage Drop (I_F = 6.0 Adc, T_C = 25°C)		V_F	1.4	Vdc
DC Reverse Current (Rated V_R)	T_A = 25°C	I_R	0.015	mA
	T_A = 100°C		1.0	
1N3889 thru 1N3893, MR1376				
DC Forward Voltage Drop (I_F = 12 Adc, T_C = 25°C)		V_F	1.4	Vdc
DC Reverse Current (Rated V_R)	T_C = 25°C	I_R	0.025	mA
	T_C = 100°C		3.0	
1N3899 thru 1N3903, MR1386				
DC Forward Voltage Drop (I_F = 20 Adc, T_A = 25°C)		V_F	1.4	Vdc
DC Reverse Current (Rated V_R)	T_A = 25°C	I_R	0.05	mA
	T_A = 100°C		6.0	
1N3909 thru 1N3913, MR1396				
DC Forward Voltage Drop (I_F = 30 Adc, T_A = 25°C)		V_F	1.4	Vdc
DC Reverse Current (Rated V_R)	T_A = 25°C	I_R	0.08	mA
	T_A = 100°C		10	

1N4933 thru 1N4937 (continued)

REVERSE RECOVERY TIME CHARACTERISTICS

Characteristics	Symbol	Max Limit	Unit
Maximum Reverse Recovery Time (I_F = 1.0 Amp min, Figure 2 test circuit) All Types	t_{rr}	0.2	μs
Maximum Overshoot Current (Figure 2)	I_{os}		Amp
1N4933, MR830, 1N3879, 1N3889 Series MR1386, MR1367		2.0	
1N3890, 1N3909 Series MR1386, MR1396		3.0	

FIGURE 1 — TYPICAL RECOVERY PATTERN

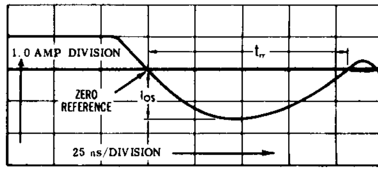
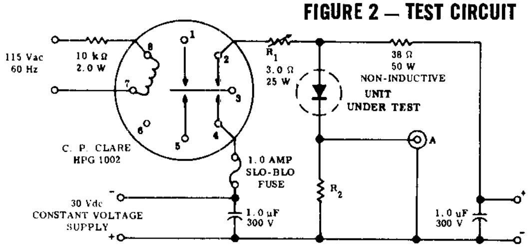


FIGURE 2 — TEST CIRCUIT



A — TEKTRONIX 545A, K PLUG-IN PRE-AMP, P6000 PROBE OR EQUIVALENT

R_1 — ADJUST TO APPROXIMATELY 1.4 Ω TO GIVE A MAX I_{os} WHICH IS NOT GREATER THAN THE MAX SPECIFIED VALUE. t_{rr} IS THEN MEASURED.

R_2 — TEN 1.0 W, 10 Ω, 1% CARBON COMPOUND RESISTORS IN PARALLEL

T_A = 25 $^{+10}_{-0}$ °C FOR RECTIFIER

MINIMIZE ALL LEAD LENGTHS

1.8 Adc FROM CONSTANT VOLTAGE SUPPLY
RIPPLE = 3.0 mV RMS MAX
Z_{out} = 1/2 Ω Max dc to 2.0 kHz.

FIGURE 3 — MAXIMUM CURRENT RATING

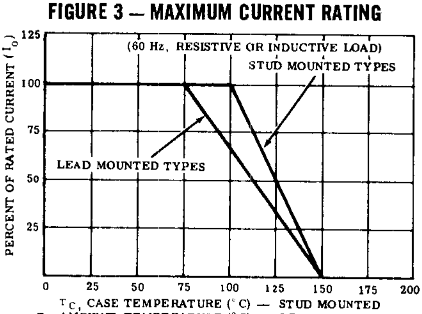
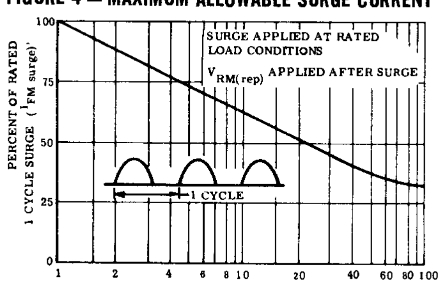


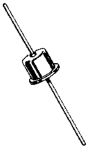
FIGURE 4 — MAXIMUM ALLOWABLE SURGE CURRENT



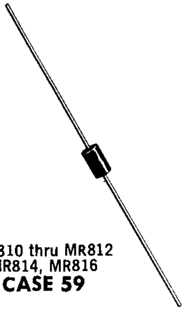
MR810 thru MR812 (SILICON)
MR814, MR816, MR840 thru MR842
MR844, MR846, MR880 thru MR882
MR884, MR886, MR890 thru MR892
MR894, MR896

I_O = 0.75-30 A
V_R = 50-600 V

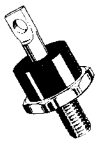
Fast recovery silicon rectifiers designed for special applications such as high frequency rectification, inverters, free-wheeling diodes, and other fast switching circuits. A complete line of rectifiers having typical recovery time of 0.5 microseconds providing high efficiency at frequencies of 50 kHz and higher.



MR840 thru MR842
MR844, MR846
CASE 60

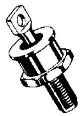


MR810 thru MR812
MR814, MR816
CASE 59



MR890 thru MR892
MR894, MR896

CASE 42
(DO-5)



MR880 thru MR882
MR884, MR886

CASE 56A (DO-4)

MAXIMUM RATINGS

I_O * Ampere	$I_{FM(surge)}$ ** Ampere	$V_{RM(rep)}$, $V_{RM(wkg)}$, V_R (volts)				
		50	100	200	400	600
0.75	30	MR810	MR811	MR812	MR814	MR816
3.0	100	MR840	MR841	MR842	MR844	MR846
12	200	MR880	MR881	MR882	MR884	MR886
30	350	MR890	MR891	MR892	MR894	MR896

* Figure 3 ** Figure 4

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max Limit	Units
Maximum Junction Operating Temperature Range	T_J	-65 to +150	°C
Maximum Case Storage Temperature Range	T_{stg}	-65 to +175	°C

MR810 thru MR812 (continued)

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Max Limit	Unit
MR810 - MR816			
DC Forward Voltage Drop (I_F = 1.0 Adc, T_A = 25°C)	V_F	1.4	Vdc
DC Reverse Current (Rated V_R) T_A = 25°C	I_R	0.01	mA
T_A = 100°C		0.2	
MR840 - MR846			
DC Forward Voltage Drop (I_F = 3.0 Adc, T_A = 25°C	V_F	1.4	Vdc
DC Reverse Current (Rated V_R) T_A = 25°C	I_R	0.075	mA
T_A = 100°C		3.5	
MR880 - MR886			
DC Forward Voltage Drop (I_F = 12 Adc, T_C = 25°C)	V_F	1.4	Vdc
DC Reverse Current (Rated V_R) T_C = 25°C	I_R	0.5	mA
T_C = 100°C		4.0	
MR890 - MR896			
DC Forward Voltage Drop (I_F = 30 Adc, T_C = 25°C)	V_F	1.4	Vdc
DC Reverse Current (Rated V_R) T_C = 25°C	I_R	1.2	mA
T_C = 100°C		15	

MR810 thru MR812 (continued)

REVERSE RECOVERY TIME CHARACTERISTICS

Characteristic	Symbol	Max Limit	Unit
Maximum Reverse Recovery Time (I_F = 1 Amp min, Figure 2 test circuit) All Types	t_{rr}	1.0	μs
Maximum Overshoot Current (Figure 2)	I_{os}		
MR810, 840, 880 Series		2.0	Amp
MR890 Series		3.0	

FIGURE 1 — TYPICAL RECOVERY PATTERN

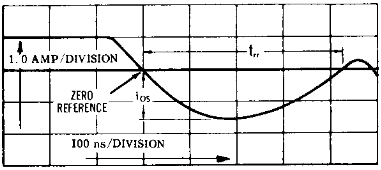
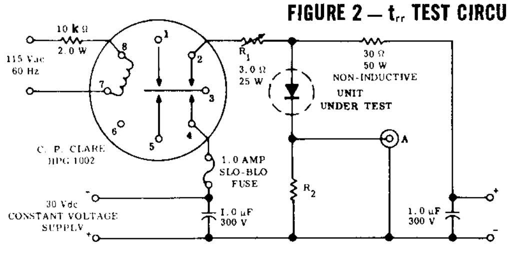


FIGURE 2 — t_{rr} TEST CIRCUIT



A - TEKTRONIX 545A, K PLUG-IN PRE-AMP, P6000 PROBE OR EQUIVALENT

R_1 - ADJUST TO APPROXIMATELY 1.4 Ω TO GIVE A MAX I_{os} WHICH IS NOT GREATER THAN THE MAX SPECIFIED VALUE. t_{rr} IS THEN MEASURED.

R_2 - TEN 1.0 W, 10 Ω, 1% CARBON COMPOUND RESISTORS IN PARALLEL

T_A = 25^{+10}_{-0} °C FOR RECTIFIER

MINIMIZE ALL LEAD LENGTHS

1.0 Adc FROM CONSTANT VOLTAGE SUPPLY
RIPPLE - 3.0 mV RMS MAX
Z_{out} = 1/2 Ω Max dc to 2.0 kHz.

FIGURE 3 — MAXIMUM CURRENT RATING

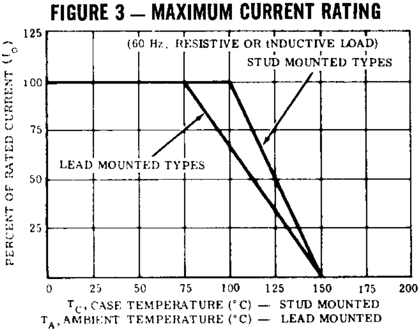
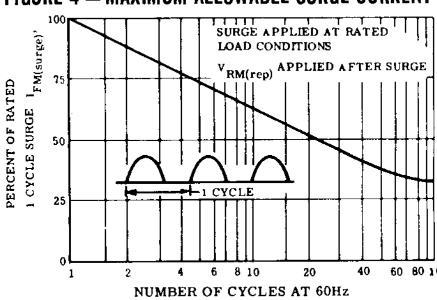


FIGURE 4 — MAXIMUM ALLOWABLE SURGE CURRENT



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THYRISTORS and TRIGGERS

SILICON CONTROLLED RECTIFIERS, 4-LAYER DIODES, UNIJUNCTION TRANSISTORS

THE FOLLOWING THYRISTORS ARE INCLUDED IN THIS SECTION

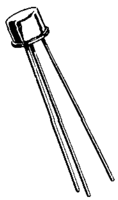
SILICON CONTROLLED RECTIFIERS

2N2322	2N4200	2N4216	2N5062
2N2323	2N4201	2N4441	2N5063
2N2324	2N4202	2N4442	MCR1906-1
2N2325	2N4203	2N4443	MCR1906-2
2N2326	2N4204	2N4444	MCR1906-3
2N4151	2N4212	2N4870	MCR1906-4
thru	2N4213	2N4871	MCR2818
2N4198	2N4214	2N5060	MCR2835
2N4199	2N4215	2N5061	MCR2918
			MCR2935

UNIJUNCTION TRANSISTORS	4-LAYER DIODES	3-LAYER DIODES
2N2646	M4L20M-3	MPT28
2N2647	thru	MPT32
2N3980	50M-28	MPT36
2N4851	M4L20-3	
2N4852	thru	
2N4853	50-28	
	M4L20A	
	thru	
	50A	

2N2322 thru 2N2326 (SILICON)

I_f = 1.6 A RMS
$V_{RXM(rep)}$ = 25-200 V



CASE 31A
(TO-5)

All-diffused PNPN thyristors designed for gating operation in mA/μA signal or detection circuits.

MAXIMUM RATINGS*(T_J = 125°C unless otherwise noted, R_{GK} = 1000 ohms)

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (Note 1) 2N2322 2N2323 2N2324 2N2325 2N2326	$V_{RXM(rep)}$	25 50 100 150 200	Volts
Non-Repetitive Peak Reverse Blocking Voltage (t < 5.0 ms) 2N2322 2N2323 2N2324 2N2325 2N2326	$V_{RXM(non-rep)}$	40 75 150 225 300	Volts
Forward Current RMS (All Conduction Angles)	I_f	1.6	Amp
Peak Surge Current (One-Half Cycle, 60 Hz) No Repetition Until Thermal Equilibrium is Restored	$I_{FM(surge)}$	15	Amp
Peak Gate Power — Forward	P_{GFM}	0.1	Watt
Average Gate Power — Forward	$P_{GF(AV)}$	0.01	Watt
Peak Gate Current — Forward	I_{GFM}	0.1	Amp
Peak Gate Voltage — Forward Reverse	V_{GFM} V_{GRM}	6.0 6.0	Volts
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Solder Temperature (> 1/16" from case, 10 sec. max)	-	+230	°C

* JEDEC Registered Values

2N3222 thru 2N2326 (continued)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms)

Characteristic	Symbol	Min	Max	Unit
Peak Forward Blocking Voltage (Note 1)	V_{FXM}			Volts
2N2322		25*	-	
2N2323		50*	-	
2N2324		100*	-	
2N2325		150*	-	
2N2326		200*	-	
Peak Reverse Blocking Current (Rated V_{RXM}, T_J = 125°C)	I_{RXM}	-	100*	µA
Peak Forward Blocking Current (Rated V_{FXM}, T_J = 125°C)	I_{FXM}	-	100*	µA
Forward "On" Voltage	V_F			Volts
(I_F = 1.0 A Peak)		-	1.5	
(I_F = 3.14 A Peak, T_C = 85°C)		-	2.0*	
Gate Trigger Current (Note 2)	I_{GT}			µA
(Anode Voltage = 6.0 Vdc, R_L = 100 ohms)		-	200	
(Anode Voltage = 6.0 Vdc, R_L = 100 ohms, T_C = -65°C)		-	350*	
Gate Trigger Voltage	V_{GT}			Volts
(Anode Voltage = 6.0 V, R_L = 100 ohms)		-	0.8	
(Anode Voltage = 6.0 V, R_L = 100 ohms, T_C = -65°C)		-	1.0*	
(Anode Voltage = Rated V_{FXM}, R_L = 100 ohms, T_J = 125°C)		0.1*	-	
Holding Current	I_{HX}			mA
(Anode Voltage = 6.0 V)		-	2.0	
(Anode Voltage = 6.0 V, T_C = -65°C)		-	3.0*	
(Anode Voltage = 6.0 V, T_C = 125°C)		0.15*	-	
Turn-On Time	t_{on}	Circuit dependent, consult manufacturer		
Turn-Off Time	t_{off}			

* JEDEC Registered Values

Notes: 1. V_{RXM} and V_{FXM} can be applied for all types on a continuous dc basis without incurring damage.

2. R_{GK} current is not included in measurement.

Thyristor devices shall not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

Thyristor devices shall not have a positive bias applied to the gate concurrently with a negative potential applied to the anode.

FIGURE 1 — CASE TEMPERATURE vs CURRENT

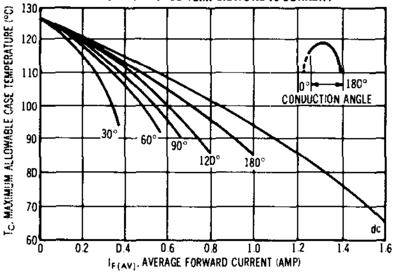
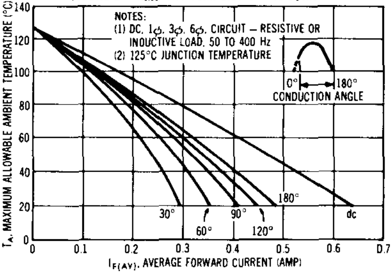


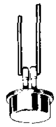
FIGURE 2 — AMBIENT TEMPERATURE vs CURRENT



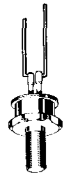
2N4151 thru 2N4198 (SILICON)

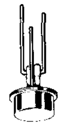
$I_f = 8$ A
$V_{ROM(rep)} = 25\text{-}600$ V

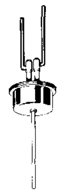

2N4151-58
CASE 85


2N4159-66
CASE 85L


2N4167-74
CASE 86


2N4175-82
CASE 86L


2N4183-90
CASE 87L


2N4191-98
CASE 88L

Multi-purpose silicon controlled rectifiers suited for industrial, consumer, and military applications. Offered in a choice of space-saving, economical packages for mounting versatility.

MAXIMUM RATINGS

(Apply over operating temperature range and for all case types unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage*†	$V_{ROM(rep)}$*†		Volts
2N4151, 59, 67, 75, 83, 91		25	
2N4152, 60, 68, 76, 84, 92		50	
2N4153, 61, 69, 77, 85, 93		100	
2N4154, 62, 70, 78, 86, 94		200	
2N4155, 63, 71, 79, 87, 95		300	
2N4156, 64, 72, 80, 88, 96		400	
2N4157, 65, 73, 81, 89, 97		500	
2N4158, 66, 74, 82, 90, 98		600	
Non-repetitive Peak Reverse Blocking Voltage	$V_{ROM(non\text{-}rep)}$		Volts
2N4151, 59, 67, 75, 83, 91		75	
2N4152, 60, 68, 76, 84, 92		100	
2N4153, 61, 69, 77, 85, 93		150	
2N4154, 62, 70, 78, 86, 94		300	
2N4155, 63, 71, 79, 87, 95		400	
2N4156, 64, 72, 80, 88, 96		500	
2N4157, 65, 73, 81, 89, 97		600	
2N4158, 66, 74, 82, 90, 98		700	
Forward Current RMS	I_f	8.0	Amp
Circuit Fusing Considerations (T_J = -40 to +100°C; t ≤ 8.3 ms)	I^2t	40	A^2s
Peak Forward Surge Current † (One cycle, 60 Hz, T_J = -40 to +100°C)	$I_{FM(surge)}$†	100	Amp
Peak Forward Gate Power †	P_{GFM}†	5.0	Watt
Average Forward Gate Power †	$P_{GF(AV)}$†	0.5	Watt
Peak Forward Gate Current †	I_{GFM}†	2.0	Amp
Peak Gate Voltage — Forward**	V_{GFM}**	10	Volts
Reverse	V_{GRM}	10	
Operating Temperature Range †	T_J†	-40 to +100	°C
Storage Temperature Range †	T_{stg}†	-40 to +150	°C
Stud Torque 2N4167-2N4182		15	in. lb.

2N4151 thru 2N4198 (continued)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.5	2.5 †	°C/W
Thermal Resistance, Case to Ambient (See Fig. 11) 2N4151-66, 2N4183-98	θ_{CA}	50	—	°C/W

*$V_{ROM(rep)}$ for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage applied exceeds the rated blocking voltage.
**Devices should not be operated with a positive bias applied to the gate concurrently with a negative potential applied to the anode.
† JEDEC Registered Values

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Peak Forward Blocking Voltage† (T_J = 100°C)	2N4151, 59, 67, 75, 83, 91	V_{FOM}†	25	—	Volts
	2N4152, 60, 68, 76, 84, 92		50	—	
	2N4153, 61, 69, 77, 85, 93		100	—	
	2N4154, 62, 70, 78, 86, 94		200	—	
	2N4155, 63, 71, 79, 87, 95		300	—	
	2N4156, 64, 72, 80, 88, 96		400	—	
	2N4157, 65, 73, 81, 89, 97		500	—	
	2N4158, 66, 74, 82, 90, 98		600	—	
Peak Forward Blocking Current† (Rated V_{FOM} @ T_J = 100°C, gate open)		I_{FOM}†	—	2.0	mA
Peak Reverse Blocking Current† (Rated V_{ROM} @ T_J = 100°C, gate open)		I_{ROM}†	—	2.0	mA
Gate Trigger Current (Continuous dc)** (Anode Voltage = 7.0 Vdc, R_L = 100 Ω)		I_{GT}**	—	20	mA
(Anode Voltage = 7.0 Vdc, R_L = 100 Ω T_C = -40°C)†			—	50†	
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 7.0 Vdc, R_L = 100 Ω)		V_{GT}	—	1.5	Volts
(Anode Voltage = 7.0 Vdc, R_L = 100 Ω, T_C = -40°C)†			—	2.5†	
(Anode Voltage = 7.0 Vdc, R_L = 100 Ω, T_J = 100°C)†			0.2†	—	
Forward "On" Voltage (pulsed, 1.0 ms max, duty cycle ≤ 1%) (I_F = 5.0 A)		V_F	—	1.3	Volts
(I_F = 15.7 A)†			—	2.0†	
Holding Current (Anode Voltage = 7.0 Vdc, gate open)		I_{HO}	—	25	mA
(Anode Voltage = 7.0 Vdc, gate open, T_C = -40°C)†			—	60†	
			Typical		
Turn-On Time (t_d + t_r) (I_G = 20 mAdc, I_F = 5.0 Adc)		t_{on}	1.0		μs
Turn-Off Time (I_F = 5.0 Adc, I_R = 5.0 Adc)		t_{off}	15		μs
(I_F = 5.0 Adc, I_R = 5.0 Adc, T_J = 100°C) (V_{FXM} = rated voltage) (dv/dt = 30 V/μs)			25		
Forward Voltage Application Rate (Gate open, T_J = 100°C)		dv/dt	50		V/μs

*V_{FOM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. These devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.
**For optimum operation, i.e. faster turn-on, lower switching losses, best di/dt capability, recommended I_{GT} = 200 mA.
† JEDEC Registered Values

2N4151 thru 2N4198 (continued)

EFFECT OF TEMPERATURE UPON TYPICAL TRIGGER CHARACTERISTICS

FIGURE 1 — GATE TRIGGER CURRENT

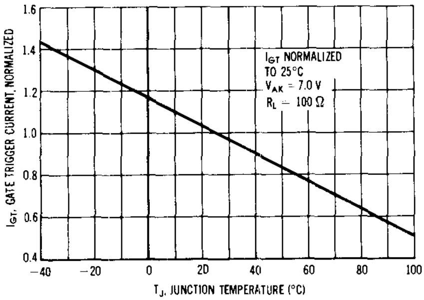
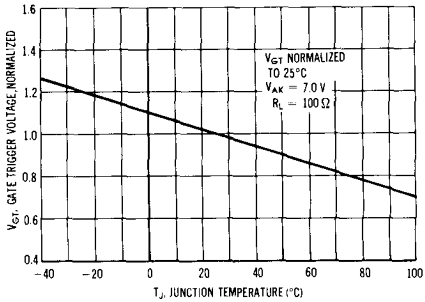


FIGURE 2 — GATE TRIGGER VOLTAGE



MAXIMUM ALLOWABLE NON-RECURRENT SURGE CURRENT

FIGURE 3 — 60 Hz SURGES

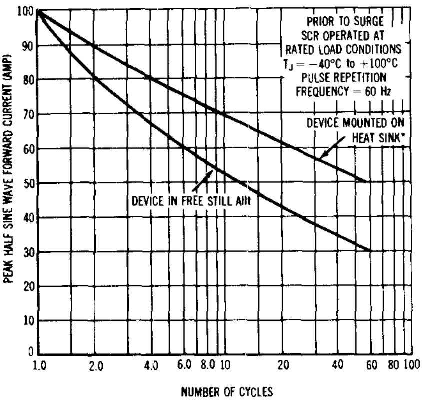


FIGURE 4 — SUB-CYCLE SURGES

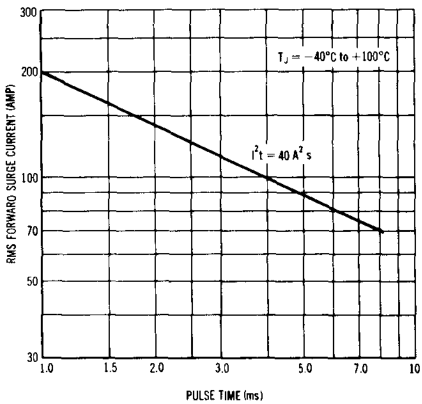


FIGURE 5 — GATE TRIGGER CHARACTERISTICS

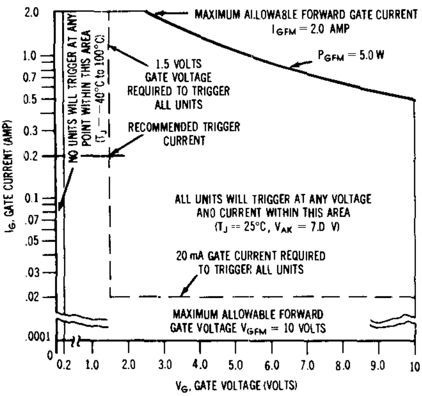
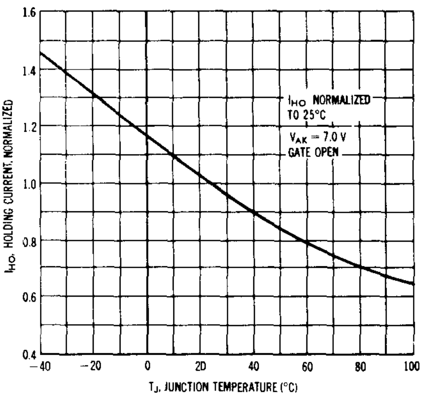


FIGURE 6 — TYPICAL HOLDING CURRENT



*Heat sink sufficient to maintain allowable case temperature for 180 degree conduction angle during normal operation, see Figure 7.

2N4151 thru 2N4198 (continued)

DERATING AND DISSIPATION FOR RESISTIVE AND INDUCTIVE LOADS (f = 60 to 400 Hz, SINE WAVE)

FIGURE 7 — CURRENT DERATING

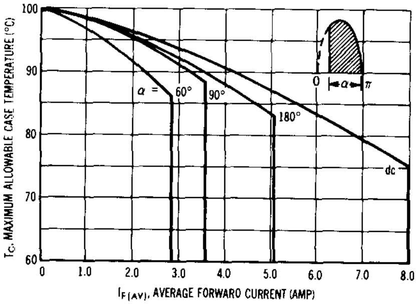


FIGURE 8 — FORWARD POWER DISSIPATION

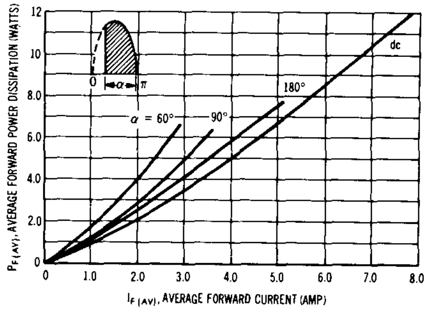


FIGURE 9 — FORWARO CONOUCTION CHARACTERISTICS

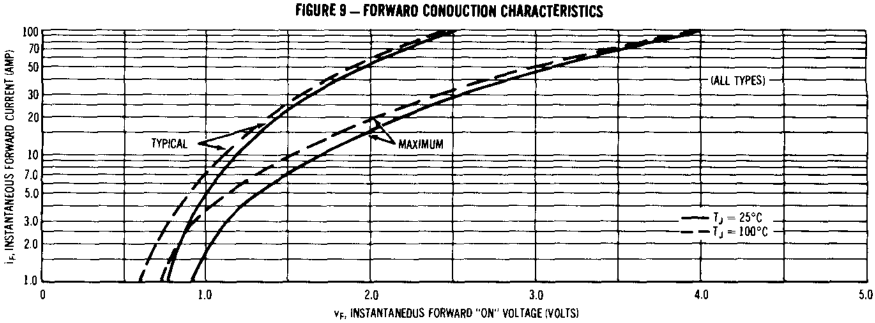


FIGURE 10 — TYPICAL THERMAL RESISTANCE OF PLATES

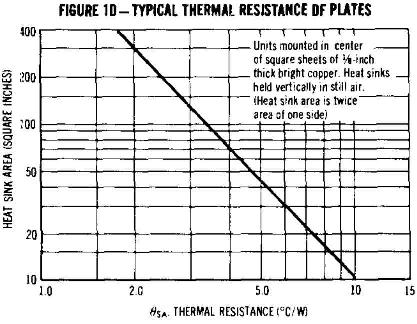
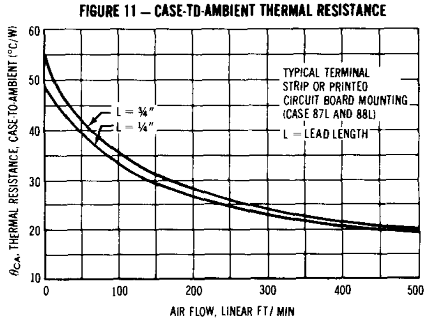
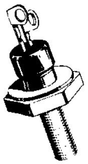


FIGURE 11 — CASE-TO-AMBIENT THERMAL RESISTANCE



2N4199 thru 2N4204

$I_{FM(rep)} = 100$ A
$V_{ROM(rep)} = 50$ V



CASE 63

Fast switching, high-voltage Thyristors especially designed for pulse modulator applications in radar and other similar equipment.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage* (T_J=105°C)	$V_{ROM(rep)}$*	50	Volts
Repetitive Peak Forward Current (PW = 3.0 μs, Duty Cycle = 0.6%, T_C = 85°C max)	$I_{FM(rep)}$	100	Amp
Current Application Rate**	di/dt**	5000	A/μs
Peak Gate Power-Forward	P_{GFM}	20	Watts
Average Gate Power-Forward	$P_{GF(AV)}$	1.0	Watt
Peak Gate Current-Forward	I_{GFM}	5.0	Amp
Peak Gate Voltage-Forward Reverse ***	V_{GFM} V_{GRM} ***	10 10	Volts
Operating Junction Temperature Range Blocking State Conducting State	T_J	 -65 to +105 -65 to +200	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C
Stud Torque	—	15	in. lb.

*Characterized for unilateral applications where reverse blocking capability is not important. Higher voltage units available upon request. $V_{ROM(rep)}$ may be applied as a continuous d c voltage for zero or negative gate voltage but positive gate voltage must not be applied concurrently with a negative potential on the anode. When checking blocking capability, do not permit the applied voltage to exceed the rated voltage.

**Minimum Gate Trigger Pulse: $i_G = 200$ mA, PW = 1 μs, $t_r = 20$ ns.

***Do not reverse bias gate during forward conduction if anode current exceeds 10 amperes.

2N4199 thru 2N4204 (continued)

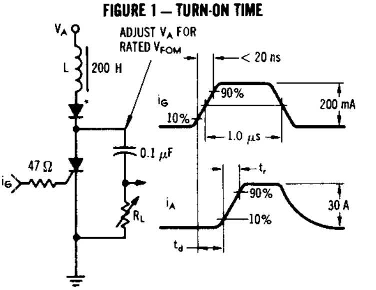
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
Peak Forward Blocking Voltage* (T_C = 105°C)	2N4199 2N4200 2N4201 2N4202 2N4203 2N4204	15	V_{FOM}*	300 400 500 600 700 800	— — — — — —	Volts
Peak Forward and Reverse Blocking Current (Rated V_{FOM} and V_{ROM}, T_C = 105°C, gate open)		17	I_{FOM} I_{ROM}	— —	2.0 2.0	mA
Gate Trigger Current (Continuous dc) (Anode Voltage = 7.0 Vdc, R_L = 100 ohms, T_C = 25°C) (Anode Voltage = 7.0 Vdc, R_L = 100 ohms, T_C = -65°C)		14	I_{GT}	— —	50 100	mA
Gate Trigger Voltage (Continuous dc) (Anode Voltage = rated V_{FOM}, R_L = 100 ohms, T_C = 105°C) (Anode Voltage = 7.0 Vdc, R_L = 100 ohms, T_C = 25°C) (Anode Voltage = 7.0 Vdc, R_L = 100 ohms, T_C = -65°C)		12	V_{GT}	0.2 — —	— 1.5 2.0	Volts
Holding Current (Anode Voltage = 7.0 Vdc, gate open, T_C = 105°C)		18	I_{HO}	3.0	—	mA
Forward "On" Voltage (I_f = 2 Adc, PW = 1.0 ms max, Duty cycle ≤ 1%)		8	V_F	—	1.5	Volts
Dynamic Forward "On" Voltage (0.5 μs after 50% decay point on dynamic forward voltage waveform.) Forward Current: 30 A pulse (PFN discharge circuit.) Gate Pulse: at 200 mA, PW = 1.0 μs, t_r = 20 ns		7	$V_{F(on)}$	—	25	Volts
Turn-On Time Delay Time Rise Time	 All types 2N4199 and 2N4200 2N4201 2N4202 2N4203 and 2N4204	 1, 9 1, 11	 t_d t_r	 — — — — —	 200 200 150 130 100	ns
Pulse Turn-Off Time Test Conditions: PFN discharge; Forward Current = 30 A pulse; Reverse Current = 5.0 A, T_C = 85°C, dv/dt = 250 V/μs to Rated V_{FOM}; Reverse anode voltage during turn-off interval = 0 V; Reverse gate bias during turn-off interval = 6.0 V.		2, 13	$t_{off(pulse)}$	—	20	μs
Forward Voltage Application Rate (Linear Rise of Voltage) (T_C = 105°C, gate open)		16	dv/dt	250	—	V/μs
Thermal Resistance (Junction to Case)		6	θ_{JC}	—	3.0	°C/W

*V_{FOM} for all types can be applied on a continous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. When checking forward or reverse blocking capability, these devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage. Other voltage units available upon request.

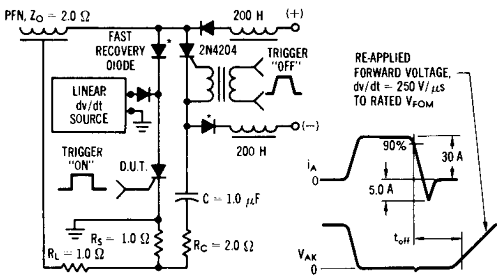
TEST CIRCUITS

FIGURE 1 — TURN-ON TIME



*Two MR1337-S fast recovery diodes in series (use voltage sharing network as described in Chapter 8 of Motorola Silicon Rectifier Handbook)

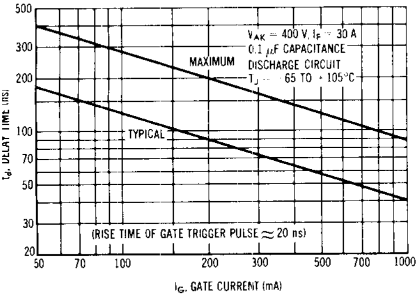
FIGURE 2 — TURN-OFF TIME



2N4199 thru 2N4204 (continued)

SWITCHING CHARACTERISTICS

FIGURE 9 — DELAY TIME



TRIGGERING CHARACTERISTICS

FIGURE 10 — TYPICAL PULSE TRIGGER CHARGE/CURRENT

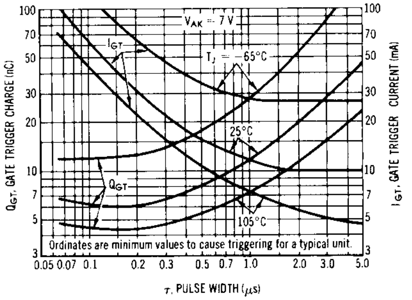


FIGURE 11 — CURRENT RISE TIME

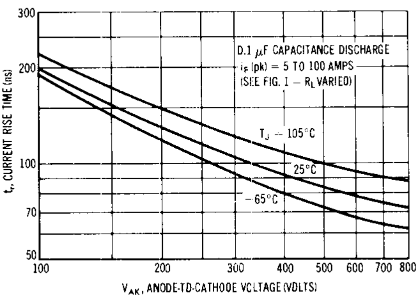


FIGURE 12 — DC GATE TRIGGER VOLTAGE

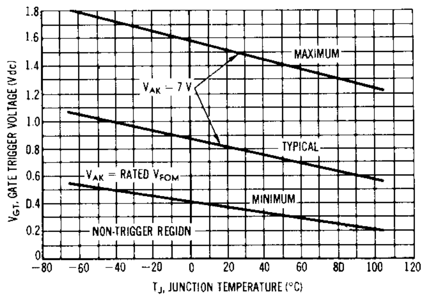


FIGURE 13 — TYPICAL TURN-OFF TIME

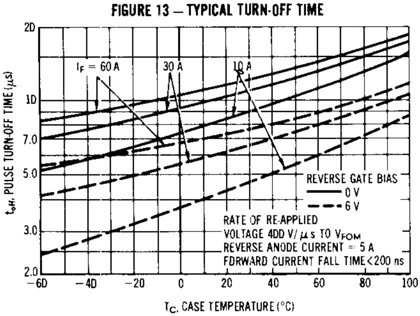
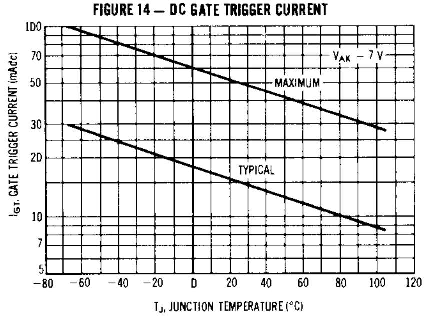


FIGURE 14 — DC GATE TRIGGER CURRENT



2N4199 thru 2N4204 (continued)

FIGURE 15 — TYPICAL BLOCKING VOLTAGE DERATING

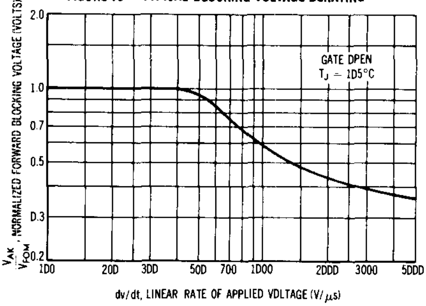


FIGURE 16 — TYPICAL dv/dt CAPABILITY

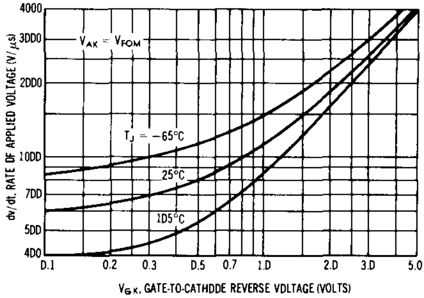


FIGURE 17 — FORWARD BLOCKING CURRENT

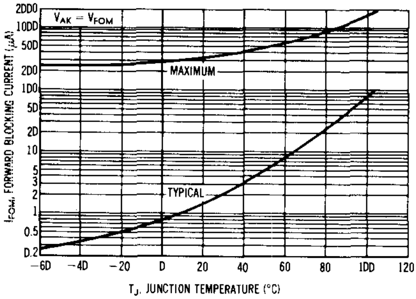


FIGURE 18 — HOLDING CURRENT

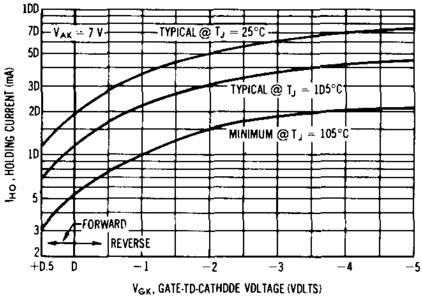


FIGURE 19 — TYPICAL ANODE-TO-CATHODE CAPACITANCE

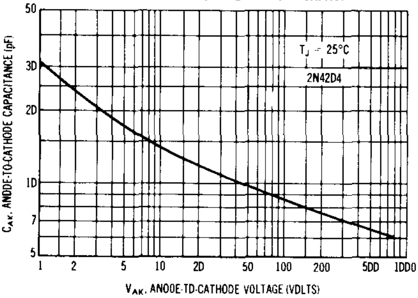
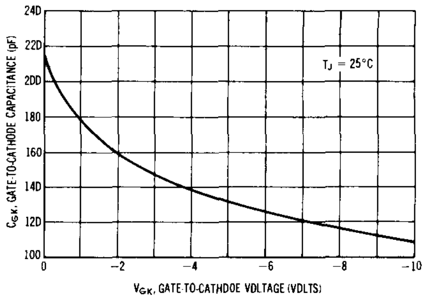
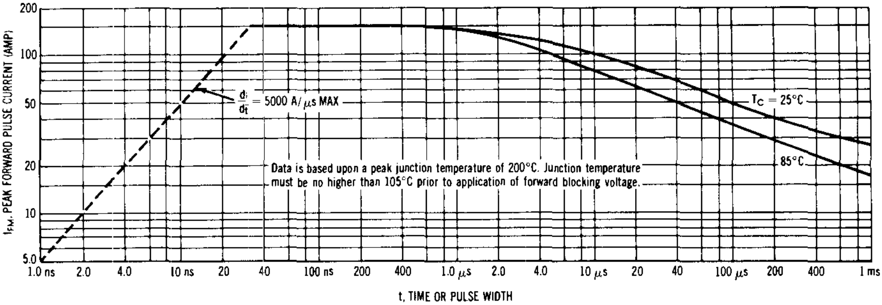


FIGURE 20 — TYPICAL GATE-TO-CATHODE CAPACITANCE



2N4199 thru 2N4204 (continued)

FIGURE 3 — MAXIMUM ALLOWABLE FORWARD PULSE CURRENT



CURRENT DERATING DATA

FIGURE 4 — DERATING USING NO SWITCHING LOSSES

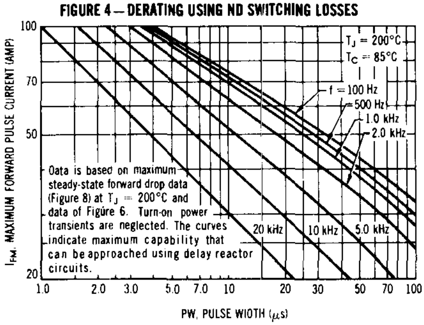
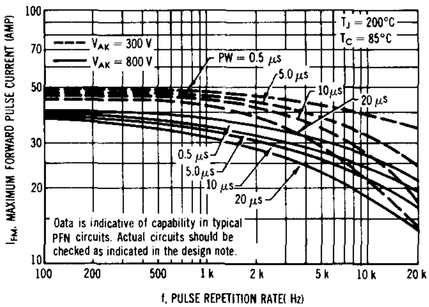


FIGURE 5 — DERATING USING TYPICAL SWITCHING LOSSES



DESIGN NOTE

Use of Transient Thermal Resistance Data

A train of periodical power pulses can be represented by the model shown in Fig. A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Fig. 6 was calculated for various duty cycles from:

$$r(t) = D + (1 - D) \cdot r(t_A + t_p) + r(t_A) - r(t_p)$$

To find $\theta_{JC}(t)$ multiply the value obtained from Fig. 6 by the steady-state value $\theta_{JC}(\infty)$. Use 3°C/W for worst-case results; use 2°C/W for typical information.

DESIGN EXAMPLE

A 2N4199 discharging a PFN, transient power pulse shown in Fig. C.

Conditions: V_{AK} = 150 V., I_{PK} = 44 A., f = 5000 Hz.

Determine: ΔT

Method 1: (See Fig. A) $P_A t_A$ is chosen to have the same energy as the actual power pulse, i.e.: the area under the curves are equal. P_A equals the peak of the actual power pulse. At a pulse repetition frequency of 5000 Hz and T_A = 2.14 μs (D = 0.0107); the reading on Fig. 6 is 0.039.

$$\therefore \Delta T = r(t)\theta_{JC}(\infty) P_A = (0.039)(3)(1000) = 120°C.$$

Method 2: For a power waveform where the time of the peak power is short compared to the total transient, the foregoing method results in an overly large safety factor. A pulse model closer to the real case is shown in Fig. B. Using the transient thermal resistance information for D = 0 in Fig. 6, $\Delta T(t_4)$ and $\Delta T(t_5)$ can be evaluated from

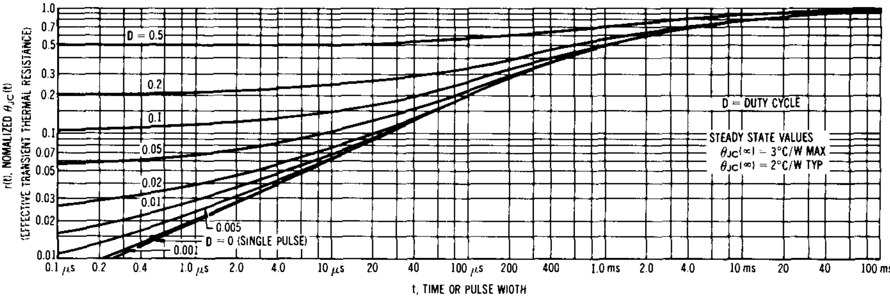
$$\Delta T(t_4) = \Big[P_1 \left[r(T_1) + (1 - D_1) \cdot r(T + T_1) + D - r(T)\right] + P_2\left[(1 - D_2) \cdot r(T) + D_2 - r(T - T_2)\right]\Big]\theta_{JC}(\infty)$$

$$\Delta T(t_5) = \Big[P_1\left[r(T_1 + T_2) + (1 - D_1) \cdot r(T + T_1 + T_2) - r(T + T_2) - r(T_2)\right] + P_2\left[r(T_2) + (1 - D_2) \cdot r(T + T_2) + D_2 - r(T)\right]\Big]\theta_{JC}(\infty)$$

The two results are compared; the one with higher value is taken for worst-case design. For the problem, values for the equivalent pulses of Fig. B are P_1 = 1000 W, P_2 = 700 W, T_1 = 1.05 μs, T_2 = 1.55 μs, $D_1 = 5.25(10^{-3})$, $D_2 = 7.75(10^{-3})$.

2N4199 thru 2N4204 (continued)

FIGURE 6 — NORMALIZED EFFECTIVE TRANSIENT THERMAL RESISTANCE



FORWARD "ON" VOLTAGE DATA

FIGURE 7 — TYPICAL DYNAMIC FORWARD "ON" VOLTAGE

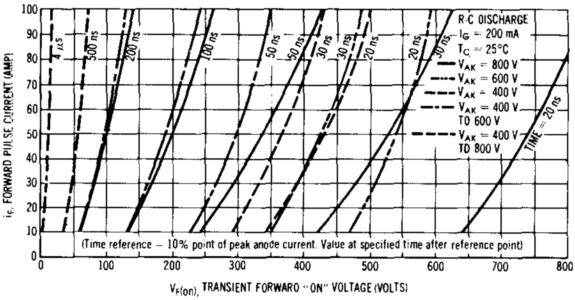
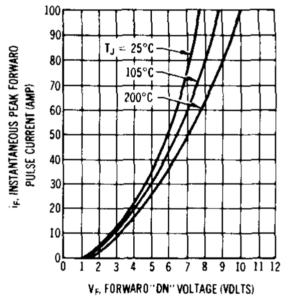


FIGURE 8 — MAXIMUM STEADY-STATE



$$\Delta T(t_4) = \left[1000\,[0.0205 + (1-5.25\cdot10^{-3})\,0.27 + 5.25\cdot10^{-3} - 0.27] + 700\,[(1-7.75\cdot10^{-3})\,0.27 + 7.75\cdot10^{-3} - 0.27]\right]3 = 93.51°C$$

$$\Delta T(t_5) = \left[1000\,[0.032 + (1-5.25\cdot10^{-3})\,0.27 + 5.25\cdot10^{-3} - 0.27 - 0.0205] + 700\,[0.025 + (1-7.75\cdot10^{-3})\,0.27 + 7.75\cdot10^{-3} - 0.27]\right]3 = 105.6°C$$

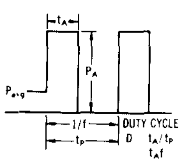


FIGURE A — SIMPLE MODEL

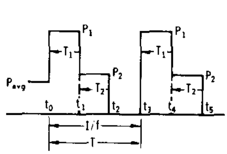


FIGURE B — MORE ACCURATE MODEL

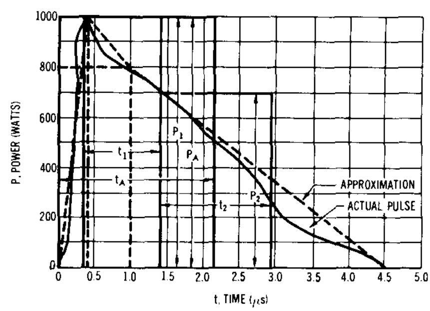
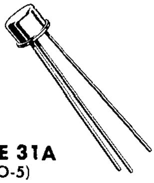


FIGURE C — AN ACTUAL TRANSIENT POWER PULSE

2N4212 thru 2N4216 (SILICON)

$I_f = 1.6\ A$
$V_{RXM(rep)} = 25\text{-}200\ V$



CASE 31A
(TO-5)

PNPN thyristors (silicon controlled rectifiers) designed for operation in mA/μA signal or detection circuits.

MAXIMUM RATINGS * (T_J = 125°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (Note 1) 2N4212 2N4213 2N4214 2N4215 2N4216	$V_{RXM(rep)}$	25 50 100 150 200	Volt
Forward Current RMS (All Conduction Angles)	I_f	1.6	Amp
Peak Surge Current (One Cycle, 60 Hz) No Repetition until Thermal Equilibrium is Restored	$I_{FM(surge)}$	15	Amp
Peak Gate Power - Forward	P_{GFM}	0.1	Watt
Average Gate Power - Forward	$P_{GF(AV)}$	0.01	Watt
Peak Gate Current - Forward	I_{GFM}	0.1	Amp
Peak Gate Voltage - Forward Reverse	V_{GFM} V_{GRM}	6.0 6.0	Volt
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Solder Temperature (> 1/16" from case, 10 sec. max)	-	+230	°C

* JEDEC Registered Values.

2N4212 thru 2N4216 (continued)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms)

Characteristics	Symbol	Min	Max	Unit
Peak Forward Blocking Voltage (Note 1)	V_{FXM}			Volt
2N4212		25*	-	
2N4213		50*	-	
2N4214		100*	-	
2N4215		150*	-	
2N4216		200*		
Peak Reverse Blocking Current (Rated V_{RXM}, T_J = 125°C)	I_{RXM}	-	200*	μA
Peak Forward Blocking Current (Rated V_{FXM}, T_J = 125°C)	I_{FXM}	-	200*	μA
Forward "On" Voltage (I_F = 1.0 Adc peak)	V_F	-	1.5*	Volt
Gate Trigger Current (Note 2) (Anode Voltage = 7.0 V, R_L = 100 ohms)	I_{GT}			μAdc
(T_C = 25°C)		-	100	
(T_C = -65°C)		-	300*	
Gate Trigger Voltage (Anode Voltage = 7.0 V, R_L = 100 ohms, T_C = 25°C)	V_{GT}	-	0.8	Volt
(Anode Voltage = 7.0 V, R_L = 100 ohms, T_C = -65°C)	V_{GT}	-	1.0*	
(Anode Voltage = Rated V_{FXM}, R_L = 100 ohms, T_J = 125°C)	V_{GNT}	0.1*	-	
Holding Current (Anode Voltage = 7.0 V) T_C = 25°C	I_{HX}		3.0	mA
T_C = -65°C			7.0*	
Turn-On Time	t_{on}	Circuit dependent, consult manufacturer		
Turn-Off Time	t_{off}			

* JEDEC Registered Values

Notes: 1. V_{RXM} and V_{FXM} can be applied for all types on a continuous dc basis without incurring damage.

2. R_{GK} current is not included in measurement.

Thyristor devices shall not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

Thyristor devices shall not have a positive bias applied to the gate concurrently with a negative potential applied to the anode.

FIGURE 1 — CASE TEMPERATURE vs CURRENT

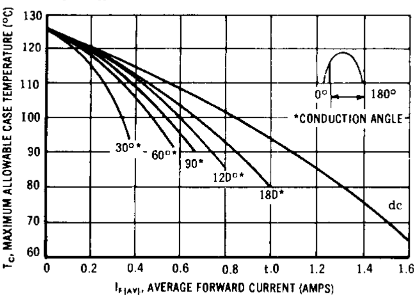
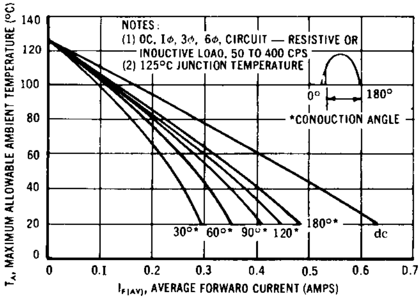
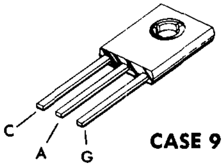


FIGURE 2 — AMBIENT TEMPERATURE vs CURRENT



2N4441 thru 2N4444 (SILICON)

$I_f = 8.0\ A$
$V_{ROM(rep)} = 50\text{-}600\ V$



CASE 90

Plastic thyristors (silicon controlled rectifiers) designed for high-volume consumer phase-control applications such as motor speed, temperature, and light controls and for switching applications in ignition and starting systems, voltage regulators, vending machines, and lamp drivers,etc.

MAXIMUM RATINGS (T_J = 100°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (Note 1) 2N4441 2N4442 2N4443 2N4444	$V_{ROM(rep)}$	50 200 400 600	Volts
Peak Reverse Blocking Voltage (Non-Recurrent, t = 5.0 ms (max) duration) 2N4441 2N4442 2N4443 2N4444	$V_{ROM(non\ rep)}$	75 300 500 700	Volts
Forward Current RMS (All Conduction Angles)	I_f	8.0	Amps
Peak Forward Surge Current (1/2 cycle, 60 Hz, T_J = -40 to +100°C)	$I_{FM(surge)}$	80	Amps
Circuit Fusing Considerations (T_J = -40 to +100°C; t = 1.0 to 8.3 ms)	I^2t	25	A^2s
Peak Gate Power - Forward	P_{GFM}	5.0	Watts
Average Gate Power - Forward	$P_{GF(AV)}$	0.5	Watt
Peak Gate Current - Forward	I_{GFM}	2.0	Amps
Peak Gate Voltage - Forward Reverse	V_{GFM} V_{GRM}	10 10	Volts
Operating Junction Temperature Range	T_J	-40 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C
Mounting Torque (6-32 screw) (Note 2)	-	12	in. lb.

2N4441 thru 2N4444 (continued)

ELECTRICAL CHARACTERISTICS (Tc = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage (T_J = 100°C) Note 1	V_{FOM}				Volts
2N4441		50	-	-	
2N4442		200	-	-	
2N4443		400	-	-	
2N4444		600	-	-	
Peak Forward Blocking Current (Rated V_{FOM} @ T_J = 100°C, gate open)	I_{FOM}	-	-	2.0	mA
Peak Reverse Blocking Current (Rated V_{ROM} @ T_J = 100°C, gate open)	I_{ROM}	-	-	2.0	mA
Forward "On" Voltage (I_F = 5.0 A peak)	V_F	-	1.0	1.5	Volts
(I_F = 15.7 A peak)		-	-	2.5 ‡	
Gate Trigger Current (Continuous dc) (Anode Voltage - 7.0 Vdc, R_L = 100 ohms) T_C = 25°C	I_{GT}	-	10	30	mA
T_C = -40°C		-	-	60 ‡	
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 7.0 Vdc, R_L = 100 ohms) T_C = 25°C	V_{GT}	-	0.7	1.5	Volts
(Anode Voltage = 7.0 Vdc, R_L = 100 ohms) T_C = -40°C	V_{GT}	-	-	2.5 ‡	
(Anode Voltage = Rated V_{FOM}, R_L = 100 ohms) T_J = 100°C	V_{GNT}	0.2 ‡	-	-	
Holding Current (Anode Voltage = 7.0 Vdc, gate open) T_C = 25°C	I_{HO}	-	10	40	mA
T_C = -40°C		-	-	70 ‡	
Turn-On Time (I_F = 5.0 A, I_{GT} = 20 mA)	t_{on}	-	1.0	-	μs
Turn-Off Time (I_F = 5.0 A, I_R = 5.0 A)	t_{off}	-	15	-	μs
(I_F = 5.0 A, I_R = 5.0 A, T_J = 100°C)		-	20	-	
Forward Voltage Application Rate (T_J = 100°C)	dv/dt	-	50	-	V/μs
Thermal Resistance, Junction to Case	θ_{JC}	-	-	2.5	°C/W
Thermal Resistance, Case to Ambient	θ_{CA}	-	40	-	°C/W

‡JEDEC registered, non-production line tests.

FIGURE 1 — CURRENT DERATING — HALF WAVE

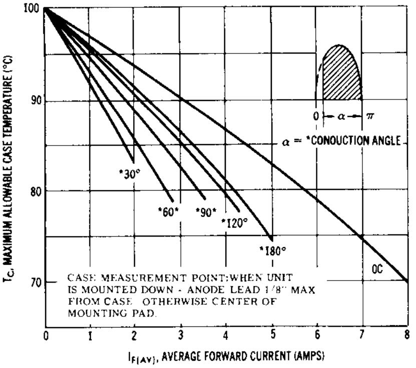
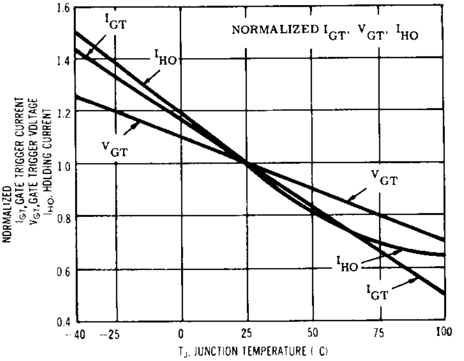
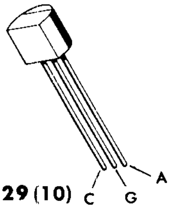


FIGURE 2 — TYPICAL PARAMETER VARIATIONS vs TEMPERATURE



2N5060 thru 2N5063

$I_f = 0.8$ A
$V_{RXM(rep)} = 30\text{-}150$ V



CASE 29 (10)
(TO-92)

PNPN plastic thyristors (silicon controlled rectifiers) designed for operation in low voltage mA/μA switching and detection circuits.

MAXIMUM RATINGS (T_J = 125°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (Note 1) 2N5060 2N5061 2N5062 2N5063	$V_{RXM(rep)}$	30 60 100 150	Volt
Forward Current RMS	I_f	0.8	Amp
Peak Surge Current (One Cycle, 60 Hz) No Repetition until Thermal Equilibrium is Restored	$I_{FM(surge)}$	6.0	Amp
Peak Gate Power - Forward	P_{GFM}	0.1	Watt
Average Gate Power - Forward	$P_{GF(AV)}$	0.01	Watt
Peak Gate Current - Forward (300 μs, 120 PPS)	I_{GFM}	1.0	Amp
Peak Gate Voltage - Forward Reverse	V_{GFM} V_{GRM}	5.0 5.0	Volt
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Solder Temperature (>1/16" from case, 10 sec. max)		+230	°C

2N5060 thru 2N5063 (continued)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms)

Characteristic	Symbol	Min	Max	Unit
Peak Forward Blocking Voltage (Note 1) 2N5060 2N5061 2N5062 2N5063	V_{FXM}	 30* 60* 100* 150*	 - - - -	Volt
Peak Reverse Blocking Current (Rated V_{RXM}, T_J = 125°C)	I_{RXM}	-	50*	μA
Peak Forward Blocking Current (Rated V_{FXM}, T_J = 125°C)	I_{FXM}	-	50*	μA
Forward "On" Voltage (I_F = 1.0 A Peak)	V_F	-	1.7*	Volt
Gate Trigger Current (Note 2) (Anode Voltage = 7.0 V, R_L = 100 ohms) (T_C = 25° C) (T_C = -65°C)	I_{GT}	 -	 200 350*	μAdc
Gate Trigger Voltage (Anode Voltage = 7.0 V, R_L = 100 ohms, T_C = 25°C) (Anode Voltage = 7.0 V, R_L = 100 ohms, T_C = -65°C) (Anode Voltage = Rated V_{FXM}, R_L = 100 ohms, T_J = 125°C)	V_{GT}	 - - 0.1*	 0.8 1.2* -	Volt
Holding Current (Anode Voltage = 7.0 V) T_C = 25°C T_C = -65°C	I_{HX}		5.0 10*	mA
Turn-On Time	t_{on}	Circuit dependent, consult manufacturer		
Turn-Off Time	t_{off}			

*JEDEC Registered Values

Notes: 1. V_{RXM} and V_{FXM} can be applied for all types on a continuous dc basis without incurring damage.
2. R_{GK} current is not included in measurement.

Thyristor devices shall not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

Thyristor devices shall not have a positive bias applied to the gate concurrently with a negative potential applied to the anode.

FIGURE 1 — CURRENT DERATING

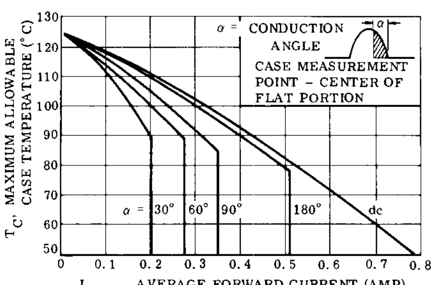
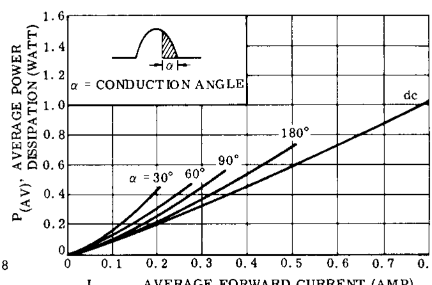
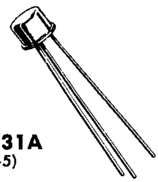


FIGURE 2 — POWER DISSIPATION



MCR1906-1 thru MCR1906-4 (SILICON)

I_f = 1.6 A
$V_{RXM(rep)}$ = 25-200 V



CASE 31A
(TO-5)

Thyristors (silicon controlled rectifiers) designed for applications in control systems and sensing circuits where low level gating and holding characteristics are necessary.

MAXIMUM RATINGS (T_J = 100°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (Note 1) MCR1906-1 MCR1906-2 MCR1906-3 MCR1906-4	$V_{RXM(rep)}$	25 50 100 200	Volt
Forward Current RMS (All Conduction Angles)	I_f	1.6	Amp
Peak Forward Surge Current (One Cycle, 60 Hz, T_J = -40 to +100°C) No Repetition Until Thermal Equilibrium is Restored	$I_{FM(surge)}$	15	Amp
Peak Gate Power Forward	P_{GFM}	0.1	Watt
Average Gate Power Forward	$P_{GF(AV)}$	0.01	Watt
Peak Gate Current Forward	I_{GFM}	0.1	Amp
Peak Gate Voltage - Forward Reverse	V_{GFM} V_{GRM}	6.0 6.0	Volt
Operating Junction Temperature Range	T_J	-65 to +100	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Solder Temperature (> 1/16" From Case, 10 sec. max.)	-	+230	°C

MCR1906-1 thru MCR1906-4 (continued)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms)

Characteristics	Symbol	Min	Max	Unit
Peak Forward Blocking Voltage (Note 1) MCR1906-1 MCR1906-2 MCR1906-3 MCR1906-4	V_{FXM}	 25 50 100 200	 - - - -	Volt
Peak Reverse Blocking Current (Rated V_{RXM}, T_J = 100°C)	I_{RXM}	-	500	μA
Peak Forward Blocking Current (Rated V_{FXM}, T_J = 100°C)	I_{FXM}	-	500	μA
Forward "On" Voltage (I_F = 1.0 Adc peak)	V_F	-	1.75	Volt
Gate Trigger Current (Note 2) (Anode Voltage = 7.0 V, R_L = 100 ohms)	I_{GT}	-	1.0	mAdc
Gate Trigger Voltage (Anode Voltage = 7.0 V, R_L = 100 ohms)	V_{GT}	-	1.0	Volt
(Anode Voltage = Rated V_{FXM}, R_L = 100 ohms, T_J = 100°C	V_{GNT}	0.1	-	
Holding Current (Anode Voltage = 7.0 V)	I_{HX}	-	5.0	mA
Turn-On Time	t_{on}	Circuit dependent, consult manufacturer		
Turn-Off Time	t_{off}			

Notes:

1. V_{RXM} and V_{FXM} can be applied for all types on a continuous dc basis without incurring damage.
2. R_{GK} current is not included in measurement.

Thyristor devices shall not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

Thyristor devices shall not have a positive bias applied to the gate concurrently with a negative potential applied to the anode.

FIGURE 1 — CASE TEMPERATURE vs CURRENT

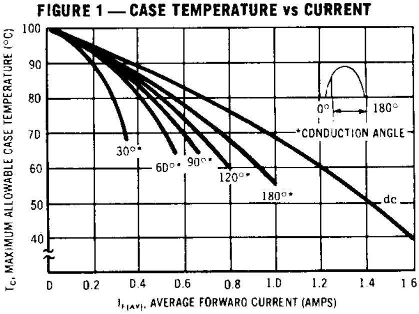
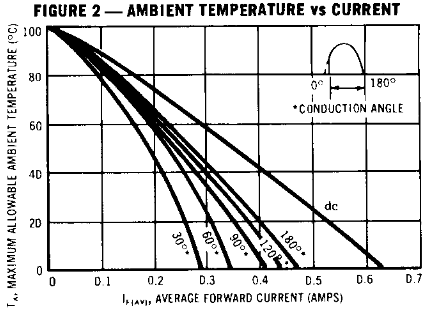


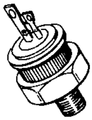
FIGURE 2 — AMBIENT TEMPERATURE vs CURRENT



MCR2818 (SERIES)
MCR2918

$I_f = 20$ A
$V_{ROM(rep)} = 25\text{-}600$ V

CASE 91



CASE 92

PNPN Thyristors (silicon controlled rectifiers) well suited for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls, and protective devices. For reverse polarity add suffix "R".

MAXIMUM RATINGS (T_J = 100°C unless otherwise noted)

Rating	Symbol	Value	Units
Repetitive Peak Reverse Blocking Voltage Ratings apply for zero or negative gate voltage.	$V_{ROM(rep)}$* Do not apply positive gate bias concurrently with negative anode potential.		Volts
MCR2818 / MCR2918 -1		25	
-2		50	
-3		100	
-4		200	
-5		300	
-6		400	
-7		500	
-8		600	
Non-repetitive Peak Reverse Blocking Voltage (t < 5.0 ms)	$V_{ROM(non\text{-}rep)}$		Volts
MCR2818 / MCR2918 -1		35	
-2		75	
-3		150	
-4		300	
-5		400	
-6		500	
-7		600	
-8		700	
Forward Current RMS	I_f	20	Amp
Peak Surge Current (one cycle, 60 Hz) (T_J = -40 to +100°C)	$I_{FM(surge)}$	240	Amp
Circuit Fusing Considerations (T_J = -40 to +100°C) (t = 1.0 to 8.3 ms)	I^2t	235	A^2s
Peak Gate Power	P_{GFM}	5.0	Watt
Average Gate Power	$P_{GF(AV)}$	0.5	Watt
Peak Forward Gate Current	I_{GFM}	2.0	Amp
Peak Gate Voltage			Volts
Forward	V_{GFM}	10	
Reverse	V_{GRM}	10	
Operating Junction Temperature Range	T_J	-40 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C
Stud Torque (MCR2918 Series)	—	30	in. lb.

MCR2818, MCR2918 (continued)

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage* ($T_J = 100°C$) MCR2818, MCR2918 -1	V_{FOM}*	25	-	-	Volts
-2		50	-	-	
-3		100	-	-	
-4		200	-	-	
-5		300	-	-	
-6		400	-	-	
-7		500	-	-	
-8		600	-	-	
Peak Forward Blocking Current (Rated V_{FOM} with gate open, $T_J = 100°C$)	I_{FOM}	-	1.0	5.0	mA
Peak Reverse Blocking Current (Rated V_{ROM}, with gate open, $T_J = 100°C$)	I_{ROM}	-	1.0	5.0	mA
Forward "On" Voltage ($I_F = 20$ A Peak)	V_F	-	1.2	1.5	Volts
Gate Trigger Current (Continuous dc) (Anode Voltage = 7.0 V, $R_L = 100\ \Omega$)	I_{GT}	-	10	40	mA
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 7.0 V, $R_L = 100\ \Omega$)	V_{GT}	-	0.7	1.5	Volts
(Anode Voltage = Rated V_{FOM}, $R_L = 100\ \Omega$, $T_J = 100°C$)	V_{GNT}	0.2	-	-	
Holding Current (Anode Voltage = 7.0 V, gate open)	I_{HO}	-	10	50	mA
Turn-On Time ($t_d + t_r$) ($I_F = 20$ Adc, $I_{GT} = 40$ mAdc)	t_{on}	-	1.0	-	μs
Turn-Off Time ($I_F = 10$ A, $I_R = 10$ A)	t_{off}	-	15	-	μs
($I_F = 10$ A, $I_R = 10$ A, $T_J = 100°C$)		-	25	-	
Forward Voltage Application Rate ($T_J = 100°C$)	dv/dt	-	50	-	V/μs
Thermal Resistance MCR2818	θ_{JC}	-	-	1.5	°C/W
MCR2918		-	-	1.8	

* V_{FOM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage.

SCR devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

FIGURE 1 — CURRENT DERATING

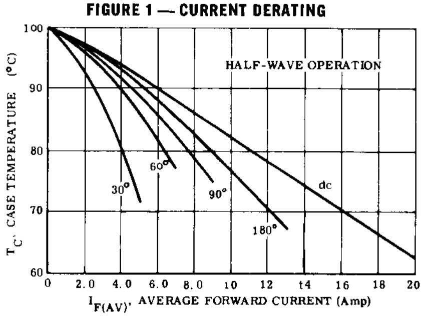
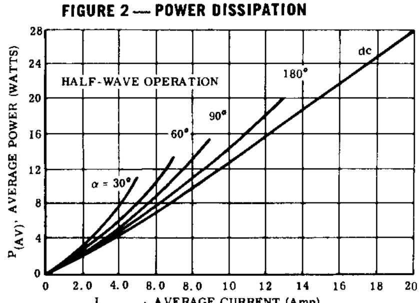


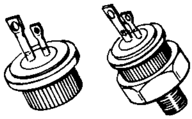
FIGURE 2 — POWER DISSIPATION



MCR2835 (SERIES)
MCR2935

$I_f = 35$ A
$V_{ROM(rep)} = 25\text{-}600$ V

PNPN



CASE 91 CASE 92

Thyristors (silicon controlled rectifiers) well suited for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls, and protective devices.

MAXIMUM RATINGS (T_J = 100° C unless otherwise noted)

Rating	Symbol	Value	Units
Do or repetitive Peak Reverse Blocking Voltage Ratings apply for zero or negative gate voltage.	$V_{ROM(rep)}$*		Volts
MCR2835 / MCR2935 -1	Do not apply positive gate bias concurrently with negative anode potential.	25	
-2		50	
-3		100	
-4		200	
-5		300	
-6		400	
-7		500	
-8		600	
Non-Repetitive Peak Reverse Blocking Voltage (t < 5.0 ms)	$V_{ROM(non\text{-}rep)}$		Volts
MCR2835 / MCR2935 -1		35	
-2		75	
-3		150	
-4		300	
-5		400	
-6		500	
-7		600	
-8		700	
Forward Current RMS	I_f	35	Amp
Peak Surge Current (one cycle, 60 Hz) (T_J = -40 to +100° C)	$I_{FM(surge)}$	325	Amp
Circuit Fusing Considerations (T_J = -40 to +100° C) (t = 1.0 to 8.3 ms)	I^2t	435	A^2s
Peak Gate Power	P_{GFM}	5.0	Watt
Average Gate Power	$P_{GF(AV)}$	0.5	Watt
Peak Forward Gate Current	I_{GFM}	2.0	Amp
Peak Gate Voltage			Volts
Forward	V_{GFM}	10	
Reverse	V_{GRM}	10	
Operating Junction Temperature Range	T_J	-40 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C
Stud Torque (MCR2935 Series)	–	30	in. lb.

MCR2835, MCR2935 (continued)

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage* ($T_J = 100°C$)	V_{FOM}*				Volts
MCR2835 -1		25	-	-	
MCR2835 -2		50	-	-	
MCR2835 -3		100	-	-	
MCR2835 -4		200	-	-	
MCR2935 -5		300	-	-	
MCR2935 -6		400	-	-	
MCR2935 -7		500	-	-	
MCR2935 -8		600	-	-	
Peak Forward Blocking Current (Rated V_{FOM} with gate open, $T_J = 100°C$)	I_{FOM}	-	1.0	5.0	mA
Peak Reverse Blocking Current (Rated V_{ROM}, with gate open, $T_J = 100°C$)	I_{ROM}	-	1.0	5.0	mA
Forward "On" Voltage (I_F = 35 A Peak)	V_F	-	1.2	1.5	Volts
Gate Trigger Current (Continuous dc) (Anode Voltage = 7.0 V, $R_L = 100\ \Omega$)	I_{GT}	-	10	40	mA
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 7.0 V, $R_L = 100\ \Omega$)	V_{GT}	-	0.7	1.5	Volts
(Anode Voltage = Rated V_{FOM}, $R_L = 100\ \Omega$, $T_J = 100°C$)		0.2	-	-	
Holding Current (Anode Voltage = 7.0 V, gate open)	I_{HO}	-	10	50	mA
Turn-On Time ($t_d + t_r$) (I_F = 35 Adc, I_{GT} = 40 mAdc)	t_{on}	-	1.0	-	μs
Turn-Off Time (I_F = 10 A, I_R = 10 A)	t_{off}	-	15	-	μs
(I_F = 10 A, I_R = 10 A, $T_J = 100°C$)		-	25	-	
Forward Voltage Application Rate ($T_J = 100°C$)	dv/dt	-	50	-	V/μs
Thermal Resistance MCR2835	θ_{JC}	-	-	1.2	°C/W
MCR2935		-	-	1.3	

* V_{FOM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. SCR devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

FIGURE 1 — CURRENT DERATING

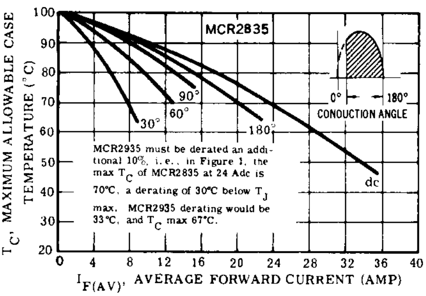
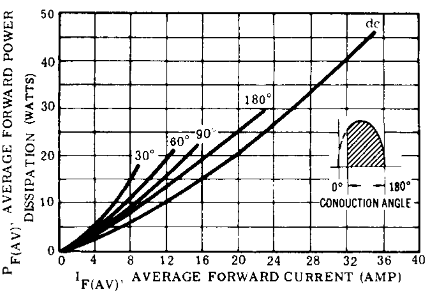
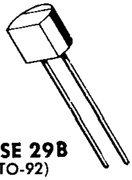


FIGURE 2 — POWER DISSIPATION



MPT28 (SILICON)
MPT32
MPT36

$I_{(BR)12}$ and $I_{(BR)21}$ = 50 μA max
ΔV_{12} and ΔV_{21} = 10 V typ



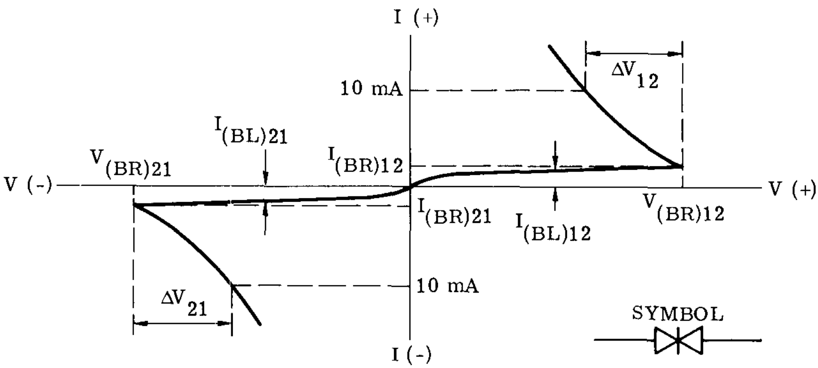
CASE 29B
(TO-92)

Plastic silicon annular 3-layer bilateral triggers, two-terminal devices which exhibit symmetrical negative resistance switching characteristics. These economical, durable devices have been developed for use in thyristor triggering circuits and signal switching and detection circuits.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Pulse Current (30 μs duration, 120 Hz repetition rate)	I_{pulse}	2.0	Amp
Power Dissipation @ T_A = -40 to +25°C Derate above 25°C	P_D	300 4.0	mW mW/°C
Operating Junction Temperature Range	T_J	-40 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

FIGURE 1 — VOLT-AMPERE CHARACTERISTICS



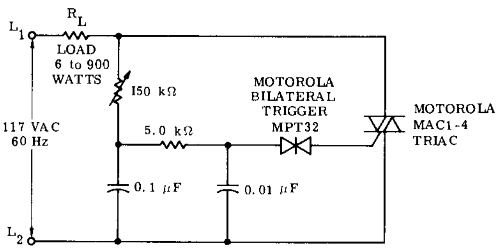
MPT28, 32, 36 (continued)

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Breakover (switching) Voltage – both directions	$V_{(BR)12}$ & $V_{(BR)21}$				Volt
MPT28		24	28	32	
MPT32		28	32	36	
MPT36		32	36	40	
Breakover (switching) Current – both directions	$I_{(BR)12}$ & $I_{(BR)21}$	-	20	50	μAmp
Switchback (delta) Voltage – both directions	ΔV_{12} & ΔV_{21}				Volt
MPT28		5.0	10	-	
MPT32		7.0	10	-	
MPT36		7.0	10	-	
Peak Blocking Current – both directions Voltage Applied ≈ 18 V	$I_{(BL)12}$ & $I_{(BL)21}$	-	0.5	10	μA
Breakover (switching) Voltage Temperature Coefficient, T_A = -40°C to +100°C		-	0.03	-	%/°C

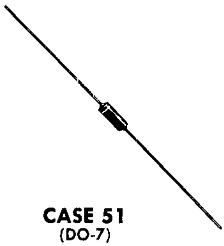
* Plastic trigger devices have symmetrical characteristics and as such the terminat leads are interchangeable. For purposes of symbol clarification, the leads have arbitrarily been designated 1 and 2. A 12 designation indicates that terminal 1 is positive with respect to terminal 2, vice versa for a 21 designation.

FIGURE 2 – TYPICAL CONTROL CIRCUIT



M4L20M-3 thru 50M-28
M4L20-3 thru 50-28
M4L20A thru 50A

$V_{RM(rep)}$ = 10-25 V
I_F = 180 mA
P_D = 200 mW



CASE 51
(DO-7)

PNPN 4-layer diodes – two-terminal, low-leakage, oxide passivated devices used for applications such as pulse generators, alarm circuits, telephone switching circuits, sawtooth oscillator and controlled rectifier trigger circuits.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (125°C)	$V_{RM(rep)}$		Volts
M4L20 Series		10	
M4L30 Series		15	
M4L40 Series		20	
M4L50 Series		25	
Continuous Forward Current	I_F	180	mA
Steady State Power Dissipation (T_A = 50 °C)	P_D	200	mW
Derate above 50° C		2.0	mW/° C
Peak Pulse Current (PW = 50 μs Max)	I_{pulse}	10	Amp
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-65 to +150	°C

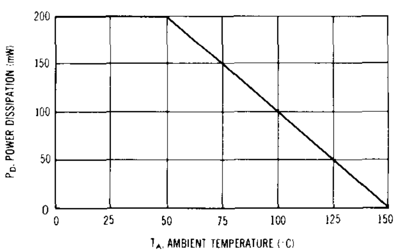
M4L20 SERIES (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Type Number	Forward Breakover Voltage $V_{(BR)F}$	Forward Breakover Voltage @T_A = −60 to +125°C $V_{(BR)F}$	Holding Current I_H mA	Max. Switch. Current $I_{(BR)F}$ @ $V_{(BR)F}$	Fwd. Imp. Test Current I_F	Max. Imp. r_{on}@I_F f = 60 Hz	Max. Forward Voltage @ I_F = 70 mA V_F	Max. Forward Voltage @ I_F = 2.0 A V_F*	Max. Cap. 10 mV AC f = 130 kHz V_R = 0 Vdc	Max. Fwd. & Rev. Leakage Current I_{FM} @ V_{FB}, I_{RM} @ V_{RM}		Max. Rev. Leakage Current @ T_A = 125°C I_{RM} @ V_{RM}	
	Min/Max	Min/Max	Min/Max	µA	mA	Ohms	Volts	Volts	pF	nA	Volts	µA	Volts
M4L20-3	16/24	-	1/6	125	70	2.0	1.2	2.5	40	50	12	-	-
M4L20M-3	16/24	14/25	1/6									125	10
M4L20-8	16/24	-	1/15									-	-
M4L20M-8	16/24	14/25	1/15									125	10
M4L20-28	16/24	-	14/45									-	-
M4L20M-28	16/24	14/25	14/45									125	10
M4L20A	14/26	-	0.5/60		85					100		-	-
M4L30-3	26/34	-	1/6		70				35	50	18	-	-
M4L30M-3	26/34	23/36	1/6									125	15
M4L30-8	28/34	-	1/15									-	-
M4L30M-8	26/34	23/36	1/15									125	15
M4L30-28	26/34	-	14/45									-	-
M4L30M-28	26/34	23/36	14/45									125	15
M4L30A	24/36	-	0.5/60		85					100		-	-
M4L40-3	36/44	-	1/6		70					50	24	-	-
M4L40M-3	36/44	32/46	1/6									125	20
M4L40-8	36/44	-	1/15									-	-
M4L40M-8	36/44	32/46	1/15									125	20
M4L40-28	36/44	-	14/45									-	-
M4L40M-28	36/44	32/46	14/45									125	20
M4L40A	34/46	-	0.5/60		85					100		-	-
M4L50-3	46/54	-	1/6		70				30	50	30	-	-
M4L50M-3	46/54	41/57	1/6									125	25
M4L50-8	46/54	-	1/15									-	-
M4L50M-8	46/54	41/57	1/15									125	25
M4L50-28	46/54	-	14/45									-	-
M4L50M-28	46/54	41/57	14/45									125	25
M4L50A	44/56	-	0.5/60		85					100		-	-

* PW = 300 µs, Duty Cycle ≤ 2%

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



MECHANICAL CHARACTERISTICS

CASE: Hermetically sealed all glass case

DIMENSIONS: JEDEC DO-7 Outline

FINISH: All external surfaces are corrosion resistant with readily solderable leads

POLARITY: Cathode end indicated by color band

WEIGHT: 0.2 grams (approx.)

MOUNTING POSITION: Any

M4L20 SERIES (continued)

TYPICAL DC CHARACTERISTICS vs. TEMPERATURE
(NORMALIZED TO +25°C VALUES)

FIGURE 2 — FORWARD BREAKOVER VOLTAGE

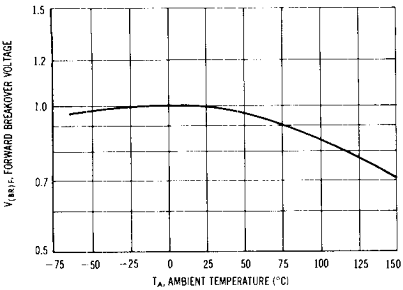


FIGURE 3 — REVERSE BLOCKING VOLTAGE

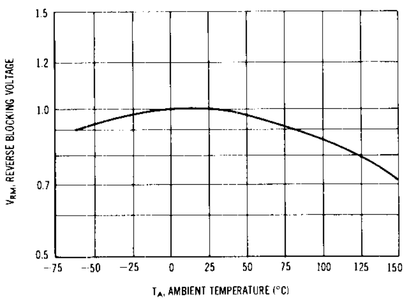


FIGURE 4 — HOLDING CURRENT

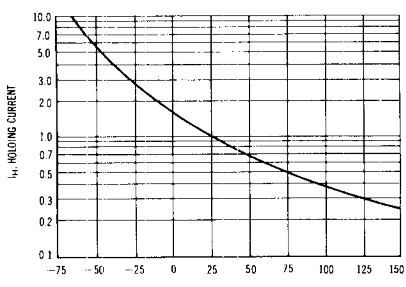
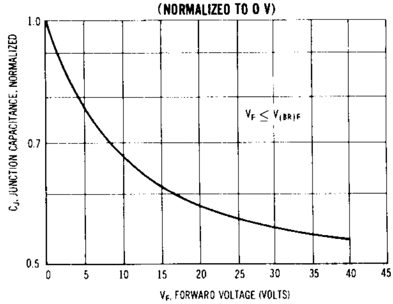


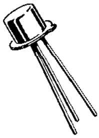
FIGURE 5 — TYPICAL CAPACITANCE (NORMALIZED TO 0 V)



Nominal Switching Voltage $V_{(BR)F}$	Typical Capacitance @ $V_F = 0$
20 V	24 pF
30 V	20 pF
40 V	19 pF
50 V	17 pF

2N2646 (SILICON)
2N2647

$V_{BB} = 35$ V
$I_e = 50$ mA
$P_D = 300$ mW



Silicon annular PN unijunction transistors designed for use in pulse and timing circuits, sensing circuits and thyristor trigger circuits.

CASE 22A

(Lead 3 connected to case)

MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D	300*	mW
RMS Emitter Current	I_e	50	mA
Peak Pulse Emitter Current**	i_e	2**	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage	V_{B2B1}	35	Volts
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

* Derate 3.0 mW/°C increase in ambient temperature. The total power dissipation (available power to Emitter and Base-Two) must be limited by the external circuitry.

** Capacitor discharge — 10 μF or less, 30 volts or less.

2N2646, 2N2647 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio (V_{B2B1} = 10 V) (Note 1)	2N2646 2N2647	η	0.56 0.68	— —	0.75 0.82	—
Interbase Resistance (V_{B2B1} = 3 V, I_E = 0)		R_{BB}	4.7	7.0	9.1	K ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3 V, I_E = 0, T_A = -55°C to +125°C)		αR_{BB}	0.1	—	0.9	%/°C
Emitter Saturation Voltage (V_{B2B1} = 10 V, I_E = 50 mA) (Note 2)		$V_{EB1(sat)}$	—	3.5	—	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)		$I_{B2(mod)}$	—	15	—	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)	2N2646 2N2647	I_{EO}	— —	0.005 0.005	12 0.2	µA
Peak Point Emitter Current (V_{B2B1} = 25 V)	2N2646 2N2647	I_P	— —	1.0 1.0	5.0 2.0	µA
Valley Point Current (V_{B2B1} = 20 V, R_{B2} = 100 ohms) (Note 2)	2N2646 2N2647	I_V	4.0 8.0	6.0 10	— 18	mA
Base-One Peak Pulse Voltage (Note 3, Figure 3)	2N2646 2N2647	V_{OB1}	3.0 6.0	5.0 7.0	— —	Volts

NOTES

1. Intrinsic standoff ratio, η, is defined by equation:

$$\eta = \frac{V_P - V_{(EB1)}}{V_{B2B1}}$$

Where V_P = Peak Point Emitter Voltage
V_{B2B1} = Interbase Voltage
$V_{(EB1)}$ = Emitter to Base-One Junction Diode Drop (≈0.5 V @ 10 µA)

2. Use pulse techniques: PW ≈ 300 µs duty cycle ≤2% to avoid internal heating due to interbase modulation which may result in erroneous readings.

3. Base-One Peak Pulse Voltage is measured in circuit of Figure 3. This specification is used to ensure minimum pulse amplitude for applications in SCR firing circuits and other types of pulse circuits.

FIGURE 1 — UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

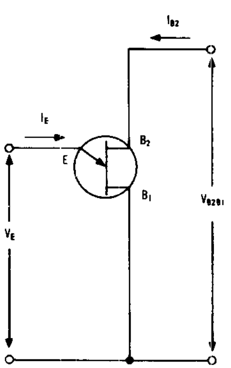


FIGURE 2 — STATIC EMITTER CHARACTERISTIC CURVES
(Exaggerated to Show Details)

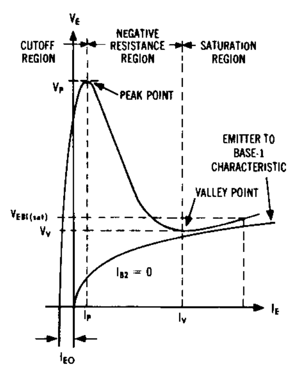
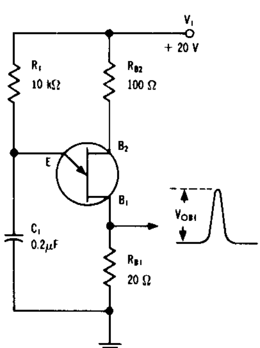
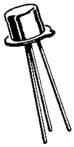


FIGURE 3 — V_{OB1} TEST CIRCUIT
(Typical Relaxation Oscillator)



2N3980

$V_{BB} = 35$ V
$I_e = 50$ mA



CASE 22A

Silicon annular PN unijunction transistor designed for military and industrial use in pulse, timing, sensing, and oscillator circuits.

(Lead 3 connected to case)

MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D	360*	mW
RMS Emitter Current	I_e	50	mA
Peak Pulse Emitter Current**	i_e	1.0**	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage	V_{B2B1}	35	Volts
Storage Temperature Range	T_{stg}	-65 to +200	°C

* Derate 2.4 mW/°C increase in ambient temperature. Total power dissipation (available power to Emitter and Base-Two) must be limited by external circuitry.

**Capacitance discharge current must fall to 0.37 Amp within 3.0 ms and PRR ≤ 10 PPS.

2N3980 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio (V_{B2B1} = 10 V) Note 1	η	0.68	—	0.82	—
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)	R_{BB}	4.0	6.0	8.0	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = -65°C to +100°C)	αR_{BB}	0.4	—	0.9	%/°C
Emitter Saturation Voltage (V_{B2B1} = 10 V, I_E = 50 mA) Note 2	$V_{EB1(sat)}$	—	2.5	3.0	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)	$I_{B2(mod)}$	12	15	—	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)	I_{EO}	—	5.0	10	nA
(V_{B2E} = 30 V, I_{B1} = 0, T_A = 125°C)		—	—	1.0	μA
Peak Point Emitter Current (V_{B2B1} = 25 V)	I_P	—	0.6	2.0	μA
Valley Point Current (V_{B2B1} = 20 V, R_{B2} = 100 ohms) Note 2	I_V	1.0	4.0	10	mA
Base-One Peak Pulse Voltage (Note 3, Figure 3)	V_{OB1}	6.0	8.0	—	Volts
Maximum Oscillation Frequency (Figure 4)	f(max)	1.0	1.25	—	MHz

NOTES

1. Intrinsic standoff ratio, η, is defined by equation:

$$\eta = \frac{V_P - V_{(EB1)}}{V_{B2B1}}$$

Where V_P = Peak Point Emitter Voltage
V_{B2B1} = Interbase Voltage
$V_{(EB1)}$ = Emitter to Base-One Junction Diode Drop ($\approx$0.5 V @ 10 μA)

2. Use pulse techniques: PW $\approx$ 300 μs duty cycle $\leq$2% to avoid internal heating due to interbase modulation which may result in erroneous readings.

3. Base-One Peak Pulse Voltage is measured in circuit of Figure 3. This specification is used to ensure minimum pulse amplitude for applications in SCR firing circuits and other types of pulse circuits.

FIGURE 1 — UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

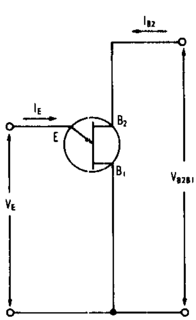


FIGURE 2 — STATIC EMITTER CHARACTERISTICS CURVES

(Exaggerated to Show Details)

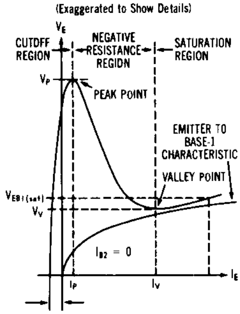


FIGURE 3 — V_{OB1} TEST CIRCUIT

(Typical Relaxation Oscillator)

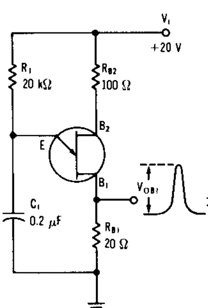
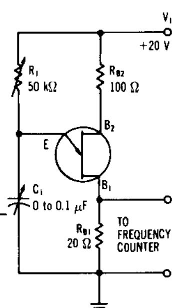
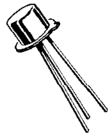


FIGURE 4 — F(max) MAXIMUM FREQUENCY TEST CIRCUIT



2N4851 thru 2N4853 (SILICON)

$V_{BB} = 35$ V
$I_e = 50$ mA RMS



Silicon annular unijunction transistors designed for pulse and timing circuits, sensing circuits, and thyristor trigger circuits.

Lead 3 connected to case

CASE 22A

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D*	300	mW
RMS Emitter Current	I_e	50	mA
Peak-Pulse Emitter Current **	i_e**	1.5	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage †	V_{B2B1}†	35	Volts
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

* Derate 3.0 mW/°C increase in ambient temperature.
** Duty cycle ≤ 1%, PRR = 10 PPS (see figure 6)
† Based upon power dissipation at T_A = 25°C

FIGURE 1 — UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

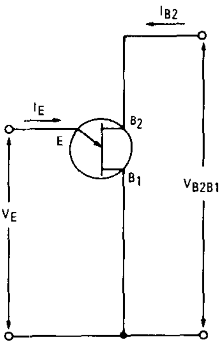


FIGURE 2 — STATIC EMITTER CHARACTERISTICS CURVES

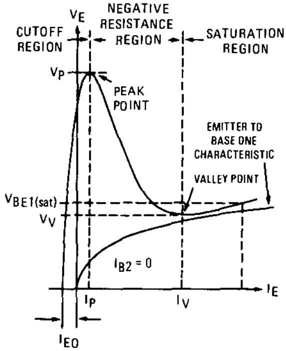
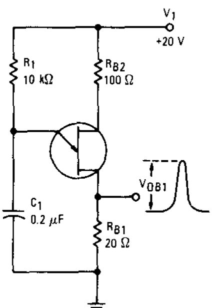


FIGURE 3 — V_{OB1} TEST CIRCUIT



2N4851 thru 2N4853 (continued)

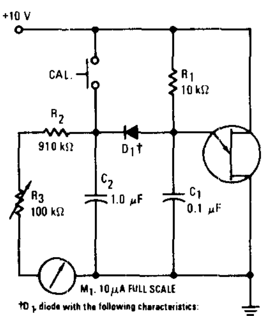
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Figure No.	Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio* (V_{B2B1} = 10 V) 2N4851 2N4852, 2N4853	4, 8	η*	0.56 0.70	— —	0.75 0.85	—
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)	11, 12	R_{BB}	4.7	—	9.1	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = -65 to +125°C)	12	αR_{BB}	0.2	—	0.8	%/°C
Emitter Saturation Voltage** (V_{B2B1} = 10 V, I_E = 50 mA)		$V_{EB1(sat)}$**	—	2.5	—	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)		$I_{B2(mod)}$	—	15	—	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0) 2N4851, 2N4852 2N4853	7	I_{EB2O}	— —	— —	0.1 0.05	µA
Peak-Point Emitter Current (V_{B2B1} = 25 V) 2N4851, 2N4852 2N4853	9, 10	I_P	— —	— —	2.0 0.4	µA
Valley-Point Current** (V_{B2B1} = 20 V, R_{B2} = 100 ohms) 2N4851 2N4852 2N4853	13, 14	I_V**	2.0 4.0 6.0	— — —	— — —	mA
Base-One Peak Pulse Voltage 2N4851 2N4852 2N4853	3, 17	V_{OB1}	3.0 5.0 6.0	— — —	— — —	Volts
Maximum Frequency of Oscillation	5	$f_{(max)}$	1.0	1.25	—	MHz

* η, Intrinsic standoff ratio, is defined in terms of the peak-point voltage, V_P, by means of the equation: $V_P = \eta V_{B2B1} + V_F$, where V_F is about 0.49 volt at 25°C @ I_F = 10 µA and decreases with temperature at about 2.5 mV/°C. The test circuit is shown in Figure 4. Components R_1, C_1, and the UJT form a relaxation oscillator; the remaining circuitry serves as a peak-voltage detector. The forward drop of Diode D_1 compensates for V_F. To use, the "cal" button is pushed, and R_3 is adjusted to make the current meter, M_1, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.0.

** Use pulse techniques: PW ≈ 300 µs, duty cycle ≦ 2.0% to avoid internal heating, which may result in erroneous readings.

FIGURE 4 — η TEST CIRCUIT



†D_1, diode with the following characteristics:
V_F = 0.49 V @ I_F = 10 µA
I_R ≦ 2.0 µA @ V_R = 20 V

FIGURE 5 — $f_{(max)}$ TEST CIRCUIT

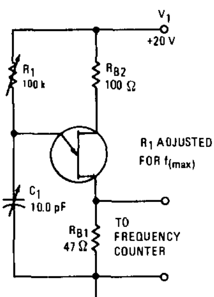
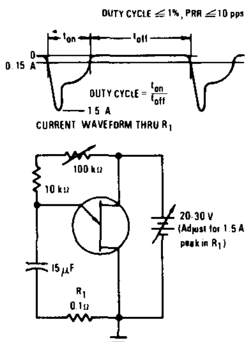


FIGURE 6 — PRR TEST CIRCUIT AND WAVEFORM



2N4851 thru 2N4853 (continued)

TYPICAL CHARACTERISTICS

FIGURE 7 — EMITTER REVERSE CURRENT

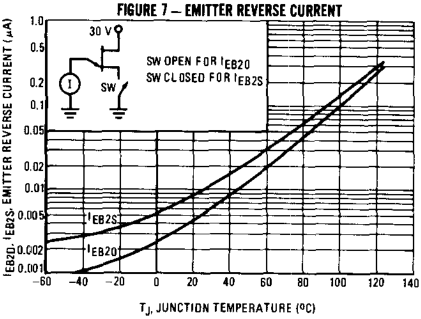
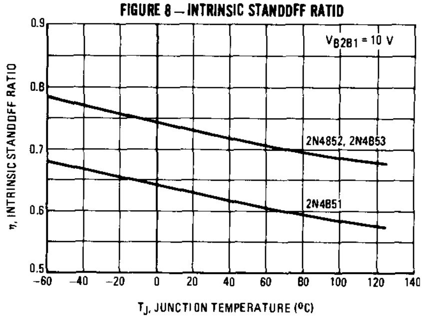


FIGURE 8 — INTRINSIC STANDOFF RATIO



PEAK POINT CURRENT

FIGURE 9 — EFFECT OF VOLTAGE

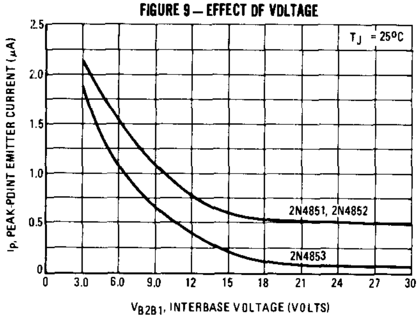
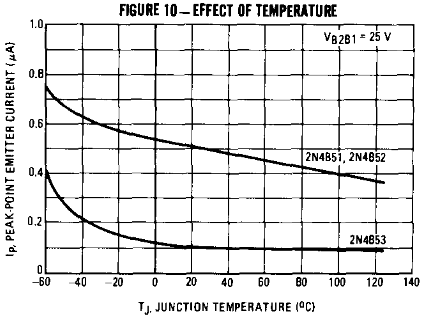


FIGURE 10 — EFFECT OF TEMPERATURE



INTERBASE RESISTANCE

FIGURE 11 — EFFECT OF VOLTAGE

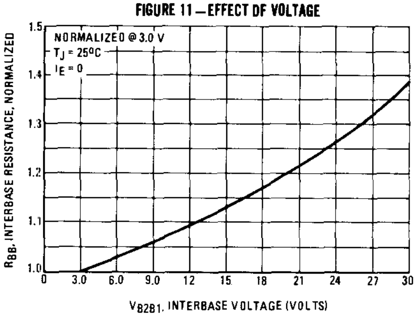
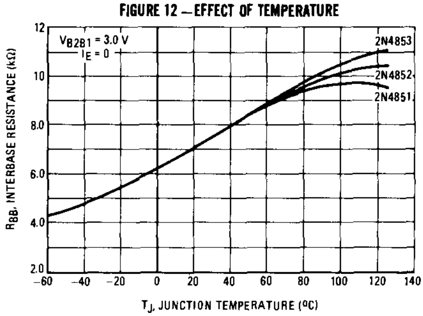


FIGURE 12 — EFFECT OF TEMPERATURE



2N4851 thru 2N4853 (continued)

TYPICAL CHARACTERISTICS

VALLEY CURRENT

FIGURE 13 — EFFECT OF VOLTAGE

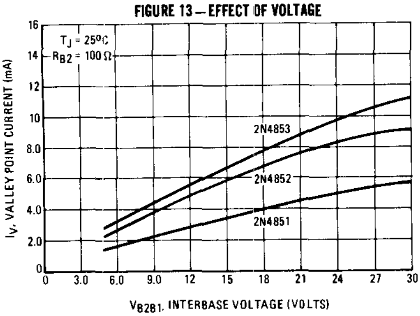
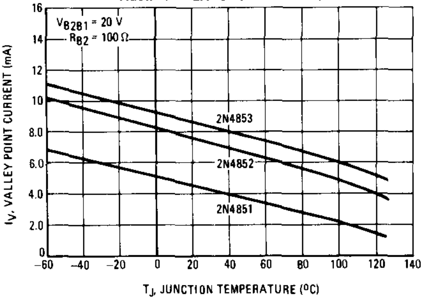


FIGURE 14 — EFFECT OF TEMPERATURE



VALLEY VOLTAGE

FIGURE 15 — EFFECT OF VOLTAGE

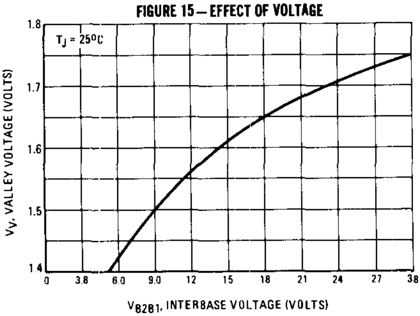


FIGURE 16 — EFFECT OF TEMPERATURE

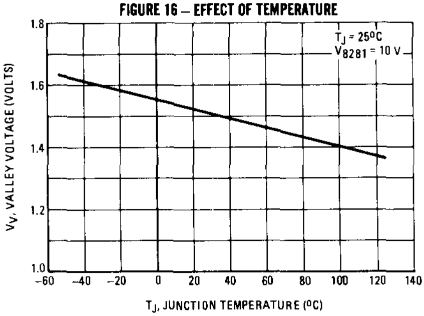
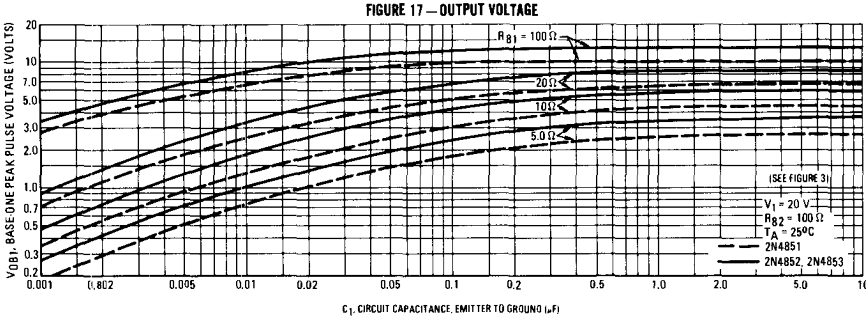
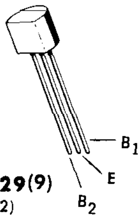


FIGURE 17 — OUTPUT VOLTAGE



2N4870 (SILICON)
2N4871

$V_{BB} = 35$ V
$I_e = 50$ mA RMS



CASE 29(9)
(TO-92)

PN unijunction transistors designed for use in pulse and timing circuits, sensing circuits and thyristor trigger circuits.

MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D	300*	mW
RMS Emitter Current	I_e	50	mA
Peak Pulse Emitter Current**	i_e	2**	Amps
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage	V_{B2B1}	35	Volts
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

* Derate 3.0 mW/°C increase in ambient temperature. The total power dissipation (available power to Emitter and Base-Two) must be limited by the external circuitry.

** Capacitor discharge — 10 μF or less, 30 volts or less.

2N4870, 2N4871 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics		Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio (V_{B2B1} = 10 V) (Note 1)	2N4870 2N4871	η	0.56 0.70	— —	0.75 0.85	—
Interbase Resistance (V_{B2B1} = 3 V, I_E = 0)		R_{BBO}	4.0	6.0	9.1	K ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3 V, I_E = 0, T_A = -55°C to +125°C)		α_{RBBO}	0.10	—	0.90	%/°C
Emitter Saturation Voltage (V_{B2B1} = 10 V, I_E = 50 mA) (Note 2)		$V_{EB1\ (sat)}$	—	2.5	—	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)		$I_{B2\ (mod)}$	—	15	—	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)		I_{EB2O}	—	0.05	1.0	μA
Peak Point Emitter Current (V_{B2B1} = 25 V)		I_P	—	1.0	5.0	μA
Valley Point Current (V_{B2B1} = 20 V, R_{B2} = 100 ohms) (Note 2)	2N4870 2N4871	I_V	2.0 4.0	5.0 7.0	— —	mA
Base-One Peak Pulse Voltage (Note 3, Figure 3)	2N4870 2N4871	V_{OB1}	3.0 5.0	6.0 8.0	— —	Volts

NOTES:

1. The intrinsic standoff ratio, η, is essentially constant with interbase voltage. η is defined by the equation:

$$\eta = \frac{V_P - V_{F(EB1)}}{V_{B2B1}}$$

Where: V_P = Peak Point Emitter Voltage

V_{B2B1} = Interbase Voltage

$V_{F(EB1)}$ = Emitter to Base-One Junction Diode Drop ($\approx$ 0.5V)

2. When Testing for Emitter Saturation Voltage ($V_{EB1\ (sat)}$) and Valley Point Current (I_V), the Emitter Current should be limited to avoid internal heating resulting in erroneous readings.

3. The Base-One Peak Pulse Voltage is measured in the circuit of Figure 3. This specification is used to ensure a minimum pulse amplitude for applications in SCR firing circuits and other types of pulse circuits.

FIGURE 1 — UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

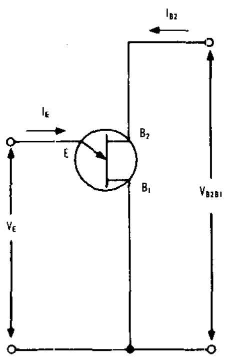


FIGURE 2 — STATIC EMITTER CHARACTERISTICS CURVES

(Exaggerated to Show Details)

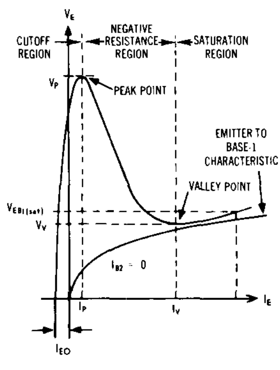
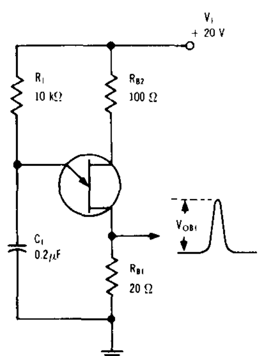


FIGURE 3 — V_{OB1} TEST CIRCUIT

(Typical Relaxation Oscillator)



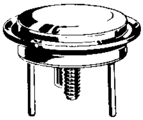
POWER TRANSISTORS

THE FOLLOWING POWER TRANSISTORS ARE INCLUDED IN THIS SECTION

2N4048	2N4399
2N4049	2N4898
2N4050	2N4899
2N4051	2N4900
2N4052	2N4910
2N4053	2N4911
2N4276	2N4912
2N4277	2N4918
2N4278	2N4919
2N4279	2N4920
2N4280	2N4921
2N4281	2N4922
2N4282	2N4923
2N4283	MP800
2N4398	MP801

2N4048 thru 2N4053

V_{CEO} = 30-60 V
I_C = 60 A
P_D = 170 W



CASE 7
(TO-36)

PNP germanium power transistors designed for high-current applications requiring high gain and extremely low saturation voltage.

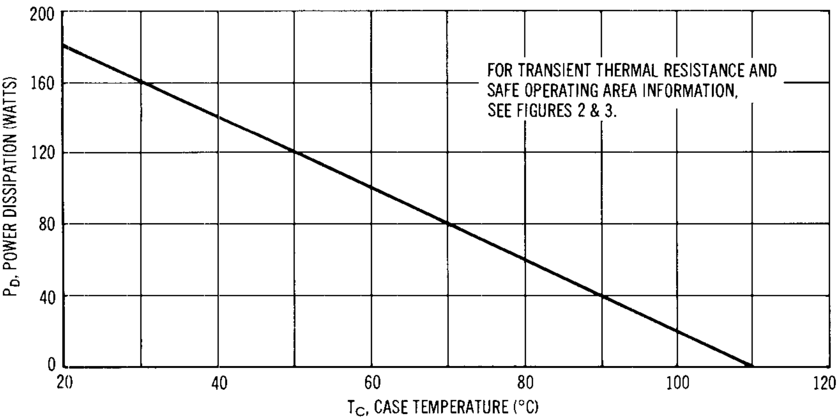
MAXIMUM RATINGS

Rating	Symbol	2N4048 2N4051	2N4049 2N4052	2N4050 2N4053	Unit
Collector-Emitter Voltage	V_{CEO}	30	45	60	Vdc
Collector-Emitter Voltage	V_{CES}	45	60	75	Vdc
Collector-Base Voltage	V_{CB}	45	60	75	Vdc
Emitter-Base Voltage	V_{EB}	25	30	40	Vdc
Collector Current — Continuous	I_C*	← 60 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 170 → ← 2.0 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +110 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.5	°C/W

FIGURE 1 — AVERAGE POWER-TEMPERATURE DERATING CURVE



* JEDEC Registered Values, For True Capability See Figure 3

2N4048 thru 2N4053 (continued)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage†		BV_{CEO}†			Vdc
(I_C = 1.0 Adc, I_B = 0)	2N4048, 2N4051		30	-	
	2N4049, 2N4052		45	-	
	2N4050, 2N4053		60	-	
Collector-Emitter Breakdown Voltage		BV_{CES}			Vdc
(I_C = 300 mAdc, V_{BE} = 0)	2N4048, 2N4051		45	-	
	2N4049, 2N4052		60	-	
	2N4050, 2N4053		75	-	
Floating Potential		V_{EBF}			Vdc
(V_{CB} = 45 Vdc, I_E = 0)	2N4048, 2N4051		-	0.5	
(V_{CB} = 60 Vdc, I_E = 0)	2N4049, 2N4052		-	0.5	
(V_{CB} = 75 Vdc, I_E = 0)	2N4050, 2N4053		-	0.5	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 30 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_C = +71°C)	2N4048, 2N4051		-	15	
(V_{CE} = 45 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_C = +71°C)	2N4049, 2N4052		-	15	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_C = +71°C)	2N4050, 2N4053		-	15	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 2.0 Vdc, I_E = 0)	All Types		-	0.2	
(V_{CB} = 45 Vdc, I_E = 0)	2N4048, 2N4051		-	4.0	
(V_{CB} = 60 Vdc, I_E = 0)	2N4049, 2N4052		-	4.0	
(V_{CB} = 75 Vdc, I_E = 0)	2N4050, 2N4053		-	4.0	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 25 Vdc, I_C = 0)	2N4048, 2N4051		-	4.0	
(V_{BE} = 25 Vdc, I_C = 0, T_C = +71°C)			-	15	
(V_{BE} = 30 Vdc, I_C = 0)	2N4049, 2N4052		-	4.0	
(V_{BE} = 30 Vdc, I_C = 0, T_C = +71°C)			-	15	
(V_{BE} = 40 Vdc, I_C = 0)	2N4050, 2N4053		-	4.0	
(V_{BE} = 40 Vdc, I_C = 0, T_C = +71°C)			-	15	
ON CHARACTERISTICS					
DC Current Gain†		h_{FE}†			-
(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N4048, 2N4049, 2N4050		60	120	
	2N4051, 2N4052, 2N4053		80	180	
(I_C = 60 Adc, V_{CE} = 2.0 Vdc)			15	-	
Collector-Emitter Saturation Voltage†		$V_{CE(sat)}$†			Vdc
(I_C = 15 Adc, I_B = 1.0 Adc)			-	0.15	
(I_C = 60 Adc, I_B = 6.0 Adc)			-	0.3	
Base-Emitter Saturation Voltage†		$V_{BE(sat)}$†			Vdc
(I_C = 15 Adc, I_B = 1.0 Adc)			-	0.6	
(I_C = 60 Adc, I_B = 6.0 Adc)			-	1.0	
SMALL SIGNAL CHARACTERISTICS					
Common-Emitter Cutoff Frequency		$f_{\alpha e}$			kHz
(I_C = 15 Adc, V_{CE} = 2.0 Vdc)			2.0	-	

† To avoid excessive heating of the collector junction, perform test with pulse method.

The switching performance of this transistor is determined primarily by the gain-bandwidth product, f_T*, and the behavior of the base-spreading resistance, r_B'.

In the case of rise time, the base-spreading resistance plays a small part, and the test circuit delivers a constant current step of turn-on current to the transistor (I_{B1}). Therefore, the curve of t_r on Figure 6 follows theory closely, i.e.:

$$t_r \doteq 0.8 \frac{I_C}{I_{B1}} \cdot \frac{1}{2\pi f_T}$$

From the curve, it can be seen that f_T is roughly constant with current; using the equation, its large signal value can be calculated to be approximately 120 kHz at the 20-Amp level. A lower supply voltage will increase rise time slightly.

Turn-off time is slow because of conductivity modulation which occurs in the base region. When the transistor is held "on" in saturation, the base region becomes filled with excess charge; i.e., charge in excess of that necessary to sustain the circuit limited value of I_C. As a result, the base resistivity and consequently r_B' become very low. During turn off, as the excess charge is reduced, the accompanying increase in resistivity causes a marked reduction in the turn-off current, i_{B2}, as can be seen from the waveforms of Figure 5. During fall time, the i_{B2} current is very low causing an extended fall time.

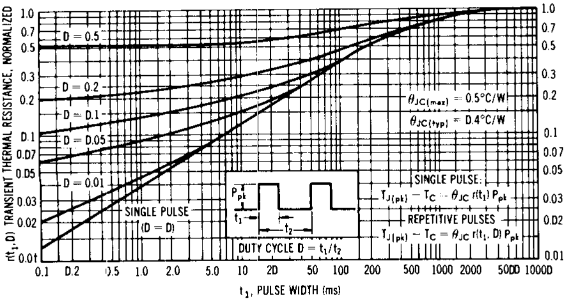
Only a slight improvement in turn-off performance is achieved with a "speed-up" capacitor placed across R_B. This unusual behavior occurs because r_B' limits the amount of reverse current which can be achieved. Also, it seems evident that r_B' increases with applied reverse current, so that efforts to speed up the turn-off behavior are somewhat futile.

In most applications, switching time will be close to the values shown on Figure 6. Delay time is not shown as it is negligible in comparison to the other times.

* $f_T \approx f_{\alpha e} \times h_{fe}$

2N4048 thru 2N4053 (continued)

FIGURE 2 – TRANSIENT THERMAL RESISTANCE



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e. the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 110°C$; T_C is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} < 110°C$. $T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 3 – ACTIVE REGION SAFE-OPERATING AREA

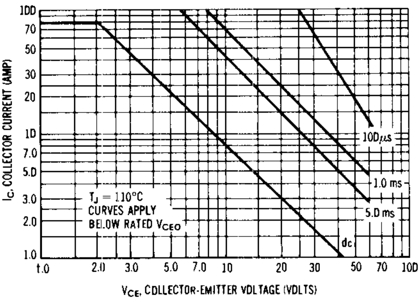


FIGURE 4 – SAFE OPERATING AREA TEST CIRCUIT

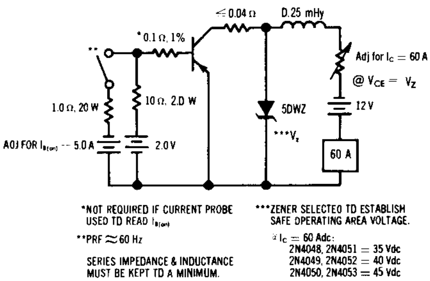


FIGURE 5 – SWITCHING TEST CIRCUIT

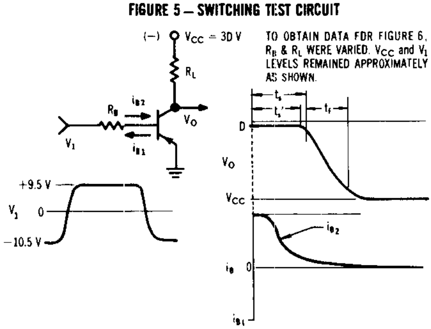
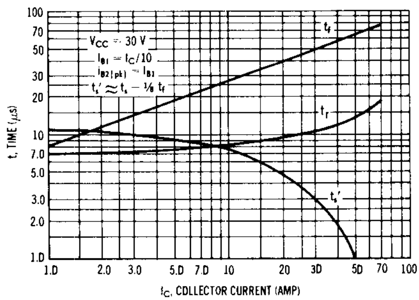


FIGURE 6 – SWITCHING TIMES



2N4048 thru 2N4053 (continued)

TYPICAL DC CHARACTERISTICS

FIGURE 7 — DC CURRENT GAIN

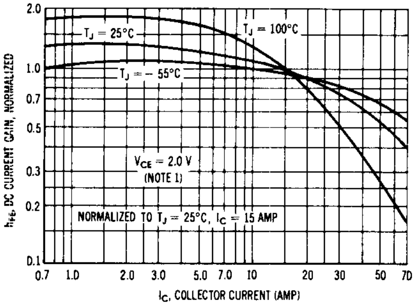


FIGURE 8 — COLLECTOR SATURATION REGION

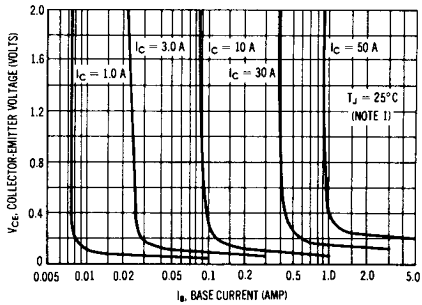


FIGURE 9 — EFFECTS OF BASE-EMITTER RESISTANCE

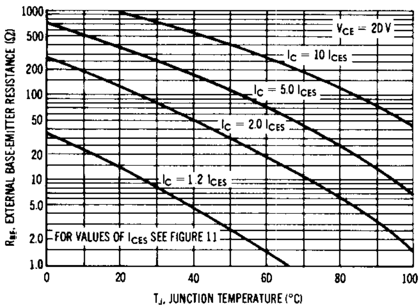


FIGURE 10 — "ON" VOLTAGES

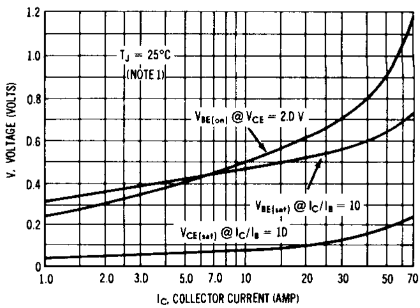


FIGURE 11 — COLLECTOR CUTOFF REGION

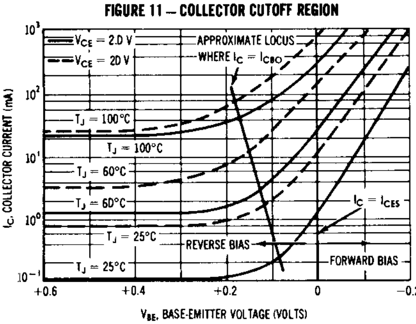
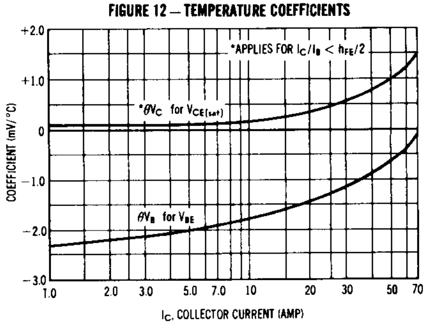


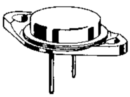
FIGURE 12 — TEMPERATURE COEFFICIENTS



NOTE 1: Data is obtained from pulse tests and adjusted to nullify the effect of I_{CBO}.

2N4276 thru 2N4283

V_{CEO} = 20-60 V
I_C = 60 A
P_D = 170 W



CASE 3A
(TO-3)

PNP germanium power transistors designed for high-current applications requiring high gain and extremely low saturation voltage.

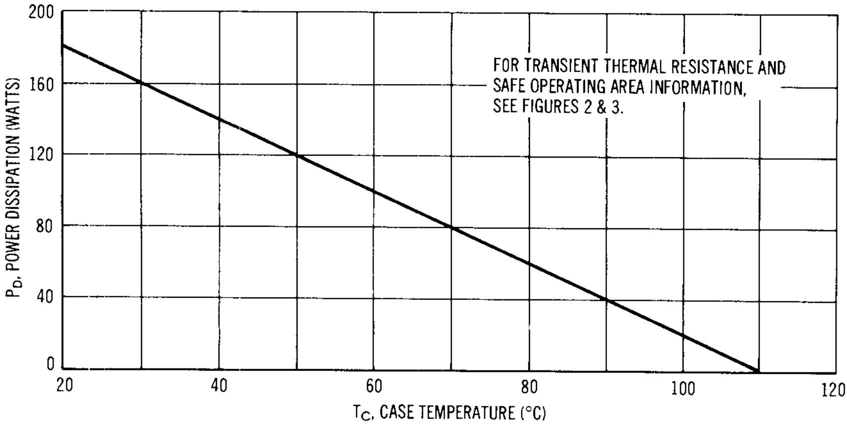
MAXIMUM RATINGS

Rating	Symbol	2N4276 2N4277	2N4278 2N4279	2N4280 2N4281	2N4282 2N4283	Unit
Collector-Emitter Voltage	V_{CEO}	20	30	45	60	Vdc
Collector-Emitter Voltage	V_{CES}	30	45	60	75	Vdc
Collector-Base Voltage	V_{CB}	30	45	60	75	Vdc
Emitter-Base Voltage	V_{EB}	20	25	30	40	Vdc
Collector Current — Continuous *	I_C*	← 60 →				Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 170 → ← 2.0 →				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +110 →				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.5	°C/W

FIGURE 1 — AVERAGE POWER-TEMPERATURE DERATING CURVE



* JEDEC Registered Values, For True Capability See Figure 3.

2N4276 thru 2N4283 (continued)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage† (I_C = 1.0 Adc, I_B = 0)	2N4276, 2N4277	BV_{CEO}†	20	-	Vdc
	2N4278, 2N4279		30	-	
	2N4280, 2N4281		45	-	
	2N4282, 2N4283		60	-	
Collector-Emitter Breakdown Voltage (I_C = 300 mAdc, V_{BE} = 0)	2N4276, 2N4277	BV_{CES}	30	-	Vdc
	2N4278, 2N4279		45	-	
	2N4280, 2N4281		60	-	
	2N4282, 2N4283		75	-	
Floating Potential (V_{CB} = 30 Vdc, I_E = 0)	2N4276, 2N4277	V_{EBF}	-	0.5	Vdc
(V_{CB} = 45 Vdc, I_E = 0)	2N4278, 2N4279		-	0.5	
(V_{CB} = 60 Vdc, I_E = 0)	2N4280, 2N4281		-	0.5	
(V_{CB} = 75 Vdc, I_E = 0)	2N4282, 2N4283		-	0.5	
Collector Cutoff Current (V_{CE} = 20 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_C = +71°C)	2N4276, 2N4277	I_{CEX}	-	15	mAdc
(V_{CE} = 30 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_C = +71°C)	2N4278, 2N4279		-	15	
(V_{CE} = 45 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_C = +71°C)	2N4280, 2N4281		-	15	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_C = +71°C)	2N4282, 2N4283		-	15	
Collector Cutoff Current (V_{CB} = 2.0 Vdc, I_E = 0)	All Types	I_{CBO}	-	0.2	mAdc
(V_{CB} = 30 Vdc, I_E = 0)	2N4276, 2N4277		-	4.0	
(V_{CB} = 45 Vdc, I_E = 0)	2N4278, 2N4279		-	4.0	
(V_{CB} = 60 Vdc, I_E = 0)	2N4280, 2N4281		-	4.0	
(V_{CB} = 75 Vdc, I_E = 0)	2N4282, 2N4283		-	4.0	
Emitter Cutoff Current (V_{BE} = 20 Vdc, I_C = 0)	2N4276, 2N4277	I_{EBO}	-	4.0	mAdc
(V_{BE} = 20 Vdc, I_C = 0, T_C = +71°C)			-	15	
(V_{BE} = 25 Vdc, I_C = 0)	2N4278, 2N4279		-	4.0	
(V_{BE} = 25 Vdc, I_C = 0, T_C = +71°C)			-	15	
(V_{BE} = 30 Vdc, I_C = 0)	2N4280, 2N4281		-	4.0	
(V_{BE} = 30 Vdc, I_C = 0, T_C = +71°C)			-	15	
(V_{BE} = 40 Vdc, I_C = 0)	2N4282, 2N4283		-	4.0	
(V_{BE} = 40 Vdc, I_C = 0, T_C = +71°C)			-	15	
ON CHARACTERISTICS					
DC Current Gain† (I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N4276, 2N4278, 2N4280, 2N4282	h_{FE}†	60	120	-
	2N4277, 2N4279, 2N4281, 2N4283		80	180	
(I_C = 60 Adc, V_{CE} = 2.0 Vdc)			15	-	
Collector-Emitter Saturation Voltage† (I_C = 15 Adc, I_B = 1.0 Adc)		$V_{CE(sat)}$†	-	0.15	Vdc
(I_C = 60 Adc, I_B = 8.0 Adc)			-	0.3	
Base-Emitter Saturation Voltage† (I_C = 15 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$†	-	0.6	Vdc
(I_C = 60 Adc, I_B = 6.0 Adc)			-	1.0	
SMALL SIGNAL CHARACTERISTICS					
Common-Emitter Cutoff Frequency (I_C = 15 Adc, V_{CE} = 2.0 Vdc)		$f_{\alpha e}$	2.0	-	kHz

† To avoid excessive heating of the collector junction, perform test with pulse method.

2N4276 thru 2N4283 (continued)

FIGURE 2 — TRANSIENT THERMAL RESISTANCE

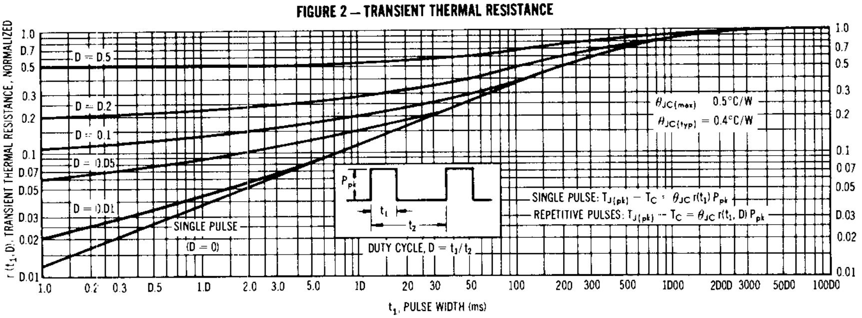
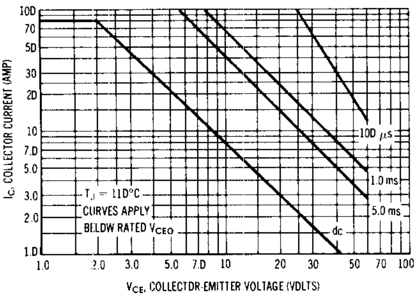


FIGURE 3 — ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e. the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)} = 110°C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} < 110°C$. $T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 4 — SWITCHING TEST CIRCUIT

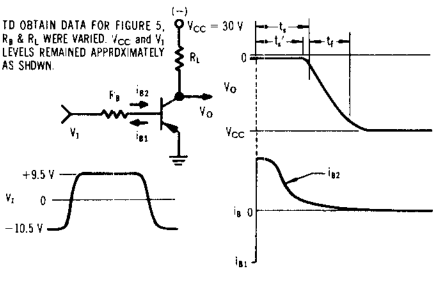
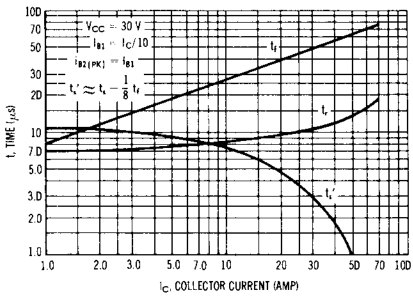


FIGURE 5 — SWITCHING TIMES



The switching performance of this transistor is determined primarily by the gain-bandwidth product, f_T*, and the behavior of the base-spreading resistance, r_B'.

In the case of rise time, the base-spreading resistance plays a small part, and the test circuit delivers a constant current step of turn-on current to the transistor (I_{B1}). Therefore, the curve of t_r on Figure 5 follows theory closely, i.e.:

$$t_r \approx 0.8 \frac{I_C}{I_{B1}} \cdot \frac{1}{2\pi f_T}$$

From the curve, it can be seen that f_T is roughly constant with current; using the equation, its large signal value can be calculated to be approximately 120 kHz at the 20-Amp level. A lower supply voltage will increase rise time slightly.

Turn-off time is slow because of conductivity modulation which occurs in the base region. When the transistor is held "on" in saturation, the base region becomes filled with excess charge; i.e., charge in excess of that necessary to sustain the circuit limited value of I_C. As a result, the base resistivity and consequently r_B' become very low. During turn off, as the excess charge is reduced, the accompanying increase in resistivity causes a marked reduction in the turn-off current, i_{B2}, as can be seen from the waveforms of Figure 4. During fall time, the i_{B2} current is very low causing an extended fall time.

Only a slight improvement in turn-off performance is achieved with a "speed-up" capacitor placed across R_B. This unusual behavior occurs because r_B' limits the amount of reverse current which can be achieved. Also, it seems evident that r_B' increases with applied reverse current, so that efforts to speed up the turn-off behavior are somewhat futile.

In most applications, switching time will be close to the values shown on Figure 5. Delay time is not shown as it is negligible in comparison to the other times.

* $f_T = f_{\alpha e} \times h_{fe}$

2N4276-2N4283 (continued)

TYPICAL DC CHARACTERISTICS

FIGURE 6 — DC CURRENT GAIN

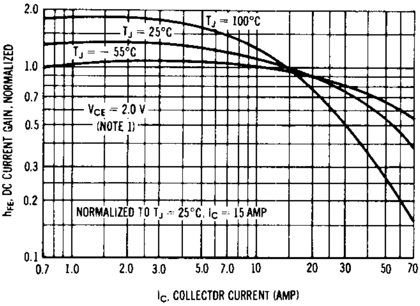


FIGURE 7 — COLLECTOR SATURATION REGION

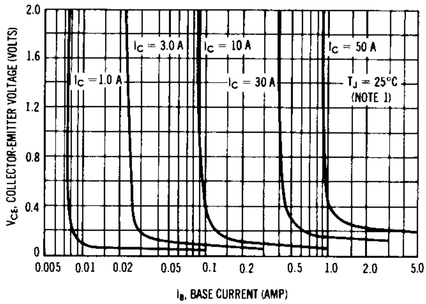


FIGURE 8 — EFFECTS OF BASE-EMITTER RESISTANCE

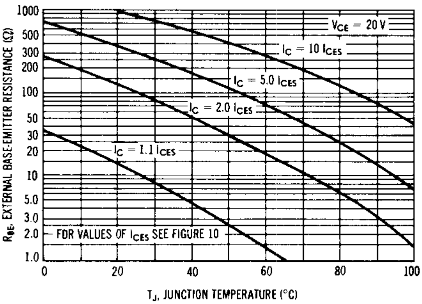


FIGURE 9 — "ON" VOLTAGES

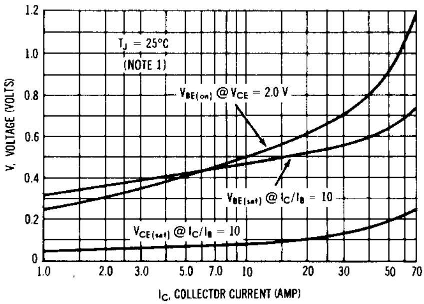
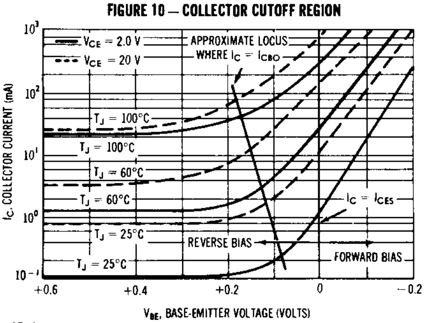
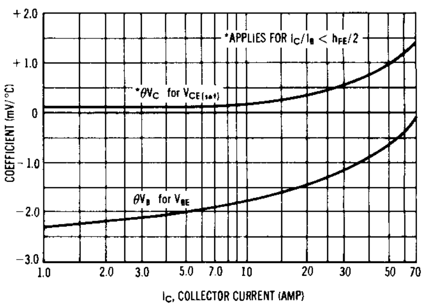


FIGURE 10 — COLLECTOR CUTOFF REGION



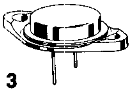
NOTE 1: Data is obtained from pulse tests and adjusted to nullify the effect of I_{CBO}.

FIGURE 11 — TEMPERATURE COEFFICIENTS



2N4398 (SILICON)
2N4399

V_{CEO} = 40-60 V
I_C = 30 A
P_D = 200 W



CASE 3
(TO-3)

High-power PNP silicon transistors for use in power amplifier and switching circuits; serves as direct replacements for germanium high-power devices.

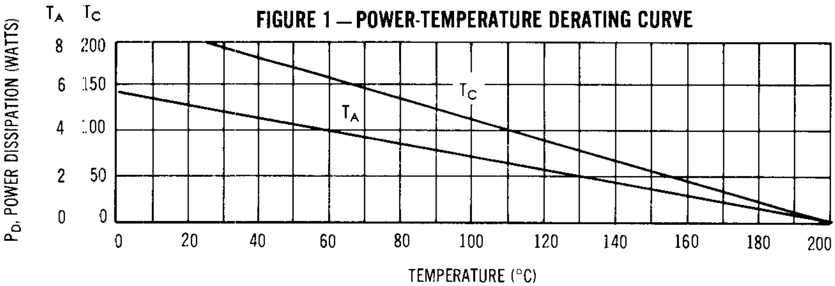
MAXIMUM RATINGS

Rating	Symbol	2N4398	2N4399	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	Vdc
Collector-Base Voltage	V_{CB}	40	60	Vdc
Emitter-Base Voltage	V_{EB}	5		Vdc
Collector Current-Continuous	I_C	30		Adc
Peak		50		
Base Current	I_B	7.5		Adc
Total Device Dissipation @ T_A = 25°C	P_D	5.0		Watts
Total Device Dissipation @ T_C = 25°C	P_D	200		Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W
Thermal Resistance, Case to Ambient	θ_{CA}	34	°C/W

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 13. All limits are applicable and must be observed.

2N4398, 2N4399 (continued)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage* (I_C = 200 mAdc, I_B = 0)	2N4398 2N4399	13	$BV_{CEO(sus)}$*	40 60	— —	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0)	2N4398 2N4399		I_{CEO}	— —	5.0 5.0	mAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 68 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	 2N4398 2N4399	7, 8	I_{CEX}	— — —	10 5.0 5.0	mAdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0)	2N4398 2N4399	7, 8	I_{CBO}	— —	1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)			I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS						
DC Current Gain* (I_C = 1.0 Adc, V_{CE} = 2.8 Vdc) (I_C = 15 Adc, V_{CE} = 2.0 Vdc) (I_C = 30 Adc, V_{CE} = 4.0 Vdc)		8	h_{FE}*	40 15 5.0	— 60 —	—
Collector-Emitter Saturation Voltage* (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 15 Adc, I_B = 1.5 Adc) (I_C = 20 Adc, I_B = 2.0 Adc)		10, 11, 12	$V_{CE(sat)}$*	— — —	0.75 1.0 2.0	Vdc
Base-Emitter Saturation Voltage* (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 15 Adc, I_B = 1.5 Adc) (I_C = 20 Adc, I_B = 2.0 Adc)		11, 12	$V_{BE(sat)}$*	— — —	1.6 1.85 2.5	Vdc
Base-Emitter On Voltage* (I_C = 15 Adc, V_{CE} = 2.0 Vdc) (I_C = 30 Adc, V_{CE} = 4.0 Vdc)		11, 12	$V_{BE(on)}$*	— —	1.7 3.0	Vdc
DYNAMIC CHARACTERISTICS						
Current Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)			f_T	4.0	—	MHz
Small Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)			h_{fe}	40	—	—
Rise Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	2, 5	t_r	—	0.4	μs
Storage Time		2, 3, 6	t_s	—	1.5	μs
Fall Time		2, 3, 6	t_f	—	0.8	μs

* Pulse Test: PW ≤ 300 μs, Duty Cycle ≤ 2.0%

SWITCHING TIME EQUIVALENT TEST CIRCUITS

FIGURE 2 — TURN-ON TIME

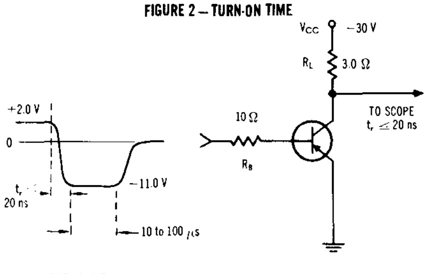
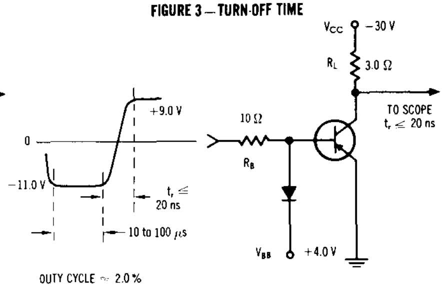


FIGURE 3 — TURN-OFF TIME



FOR CURVES OF FIGURES 5 & 6, R_B, R_L, & V_{CC} ARE VARIED. INPUT LEVELS ARE APPROXIMATELY AS SHOWN.

2N4398, 2N4399 (continued)

TYPICAL TRANSIENT CHARACTERISTICS

FIGURE 4 — CAPACITANCES

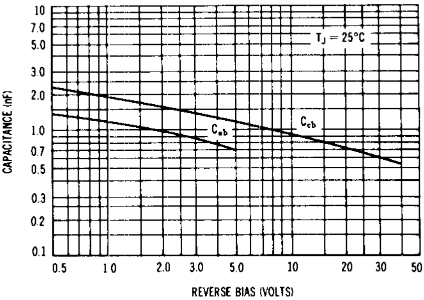


FIGURE 5 — TURN-ON TIME

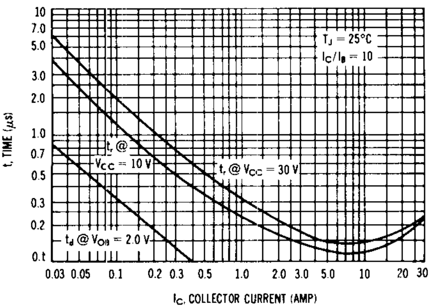
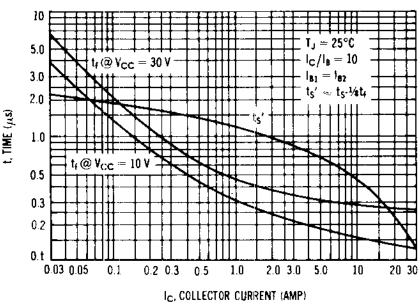


FIGURE 6 — TURN-OFF TIME



TYPICAL "OFF" REGION CHARACTERISTICS

FIGURE 7 — TRANSCONDUCTANCE

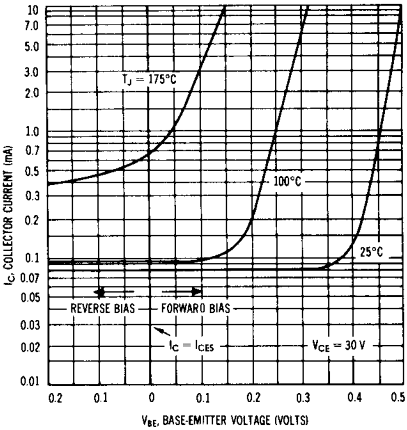
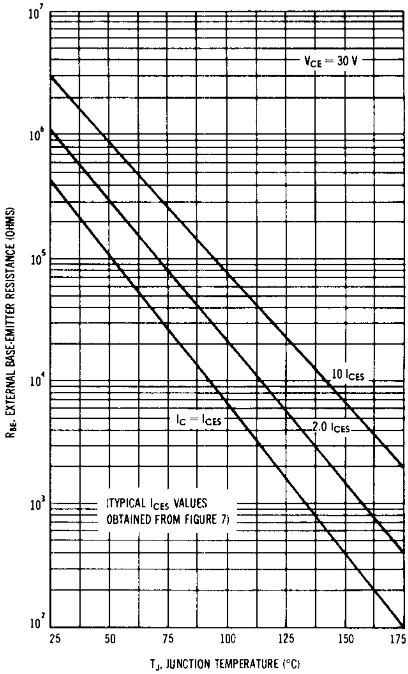


FIGURE 8 — EFFECT OF BASE-EMITTER RESISTANCE



2N4398, 2N4399 (continued)

TYPICAL "ON" REGION CHARACTERISTICS

FIGURE 9 — NORMALIZED DC CURRENT GAIN

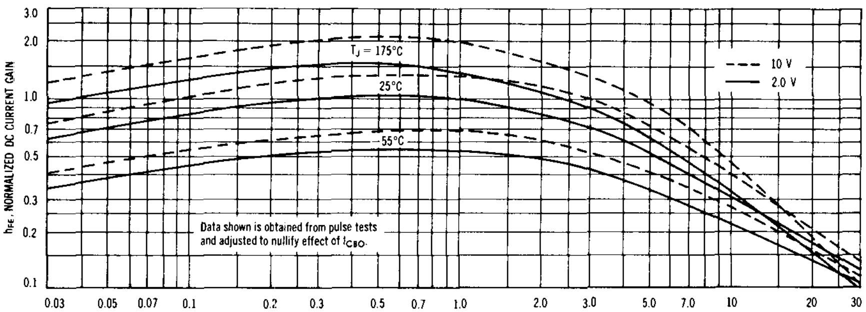


FIGURE 10 — COLLECTOR SATURATION REGION

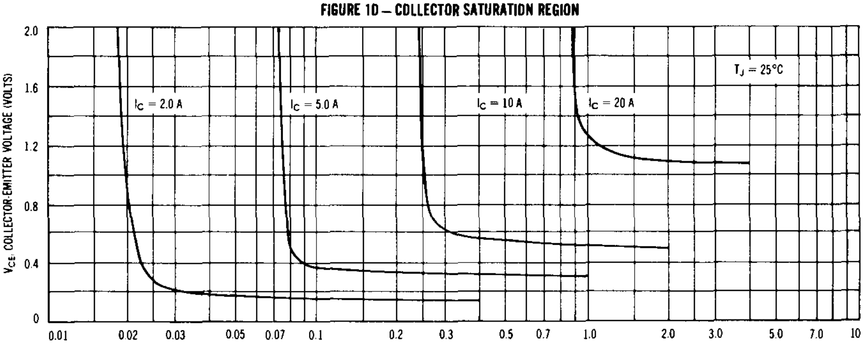


FIGURE 11 — "ON" VOLTAGES

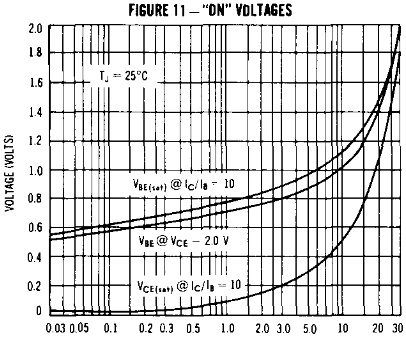
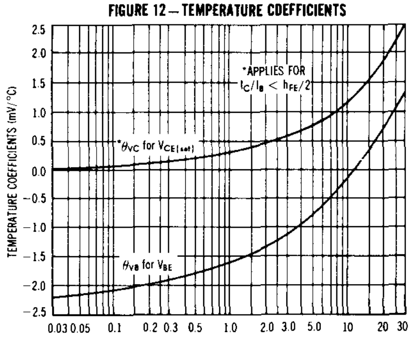


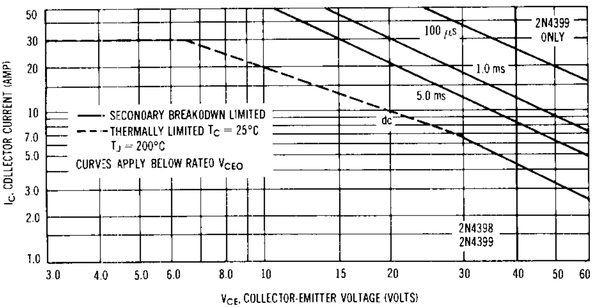
FIGURE 12 — TEMPERATURE COEFFICIENTS



2N4398, 2N4399 (continued)

RATINGS AND THERMAL DATA

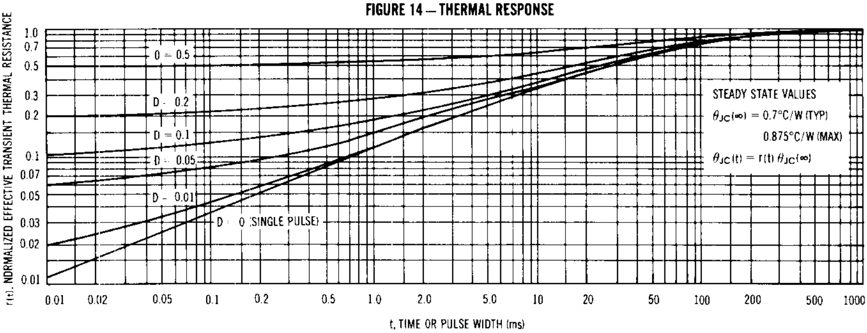
FIGURE 13 — ACTIVE-REGION SAFE OPERATING AREA



The safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

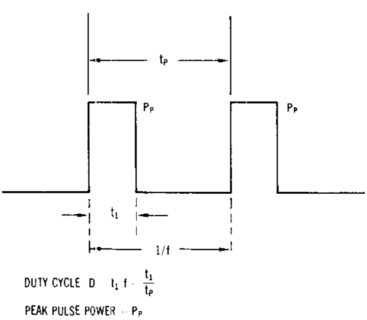
The data of Figure 13 is based upon $T_{J(pk)}$ = 200°C; T_C is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 14. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by the secondary breakdown.

FIGURE 14 — THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

FIGURE A



A train of periodical power pulses can be represented by the model as shown in Figure A. Using the model and the device thermal reponse, the normalized effective transient thermal resistance of Figure 14 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 14 by the steady state value $\theta_{JC}(\infty)$.

Example:
The 2N4398 is dissipating 100 watts under the following conditions:
t_1 = 1.0 ms, t_P = 5.0 ms. (D = 0.2)

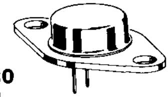
Using Figure 14, at a pulse width of 1.0 ms and D = 0.2, the reading of r (t) is 0.28.

The peak rise in junction temperature is therefore

$$\Delta T = r(t) \times P_P \times \theta_{JC}(\infty) = 0.28 \times 100 \times 0.875 = 24.5°C$$

2N4898 thru 2N4900 (SILICON)

V_{CEO} = 40-80 V
I_C = 4 A
P_D = 25 W



CASE 80
(TO-66)

Medium-power PNP silicon transistors designed for driver circuits, switching, and amplifier applications.

MAXIMUM RATINGS

Rating	Symbol	2N4898	2N4899	2N4900	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous *	I_C*	← 1.0 →			Adc
		← 4.0 →			
Base Current	I_B	← 1.0 →			Adc
Total Device Dissipation T_C = 25°C	P_D	← 25 →			Watts
Derate above 25°C		← 0.143 →			W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

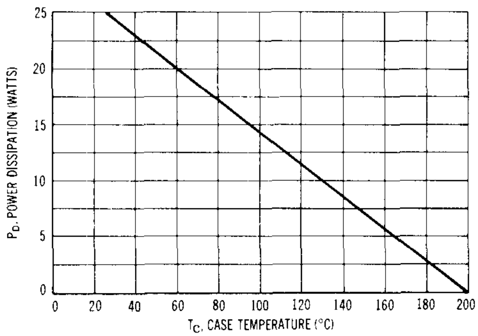
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	7.0	°C/W

* The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements.

The 4.0 Amp maximum value is based upon actual current-handling capability of the device (see Figure 5).

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



2N4898 thru 2N4900 (continued)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0) 2N4898	-	$BV_{CEO(sus)}$*	40	-	Vdc
2N4899			60	-	
2N4900			80	-	
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) 2N4898		I_{CEO}	-	0.5	mAdc
(V_{CE} = 30 Vdc, I_B = 0) 2N4899			-	0.5	
(V_{CE} = 40 Vdc, I_B = 0) 2N4900			-	0.5	
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc)	12	I_{CEX}	-	0.1	mAdc
(V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			-	1.0	
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	-	I_{CBO}	-	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	-	I_{EBO}	-	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain* (I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	8	h_{FE}*	40	-	-
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			20	100	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)			10	-	
Collector-Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)	9, 11, 13	$V_{CE(sat)}$*	-	0.6	Vdc
Base-Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)	11, 13	$V_{BE(sat)}$*	-	1.3	Vdc
Base-Emitter On Voltage* (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	11, 13	$V_{BE(on)}$*	-	1.3	Vdc
SMALL SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C - 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	-	f_T	3.0	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	-	C_{ob}	-	100	pF
Small-Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	-	h_{fe}	25	-	-

* Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%

FIGURE 2 — SWITCHING TIME EQUIVALENT CIRCUIT

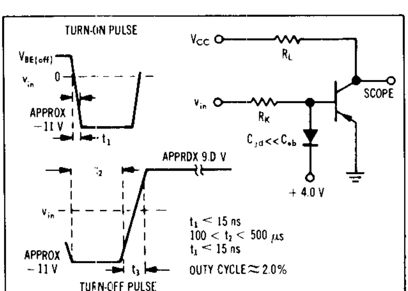
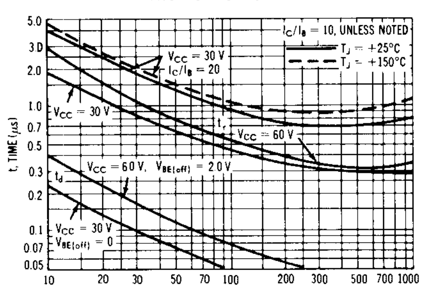


FIGURE 3 — TURN-ON TIME



2N4898 thru 2N4900 (continued)

FIGURE 4 — THERMAL RESPONSE

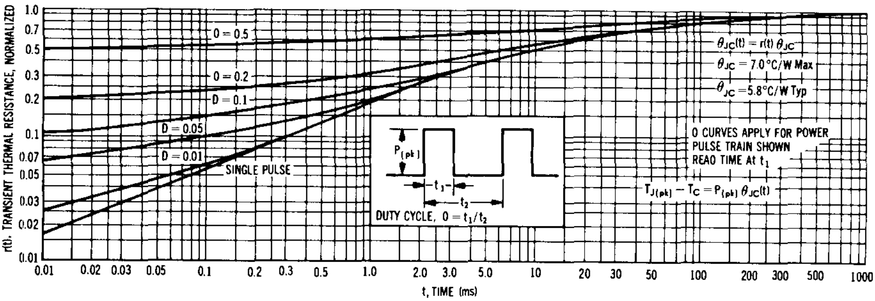
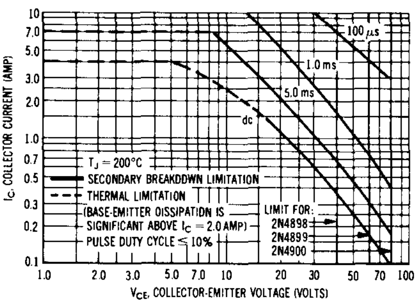


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



The safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor which must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 5 is based upon $T_{J(pk)} = 200°C$; T_C is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power which can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 — STORAGE TIME

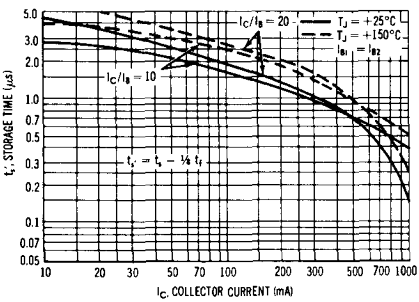
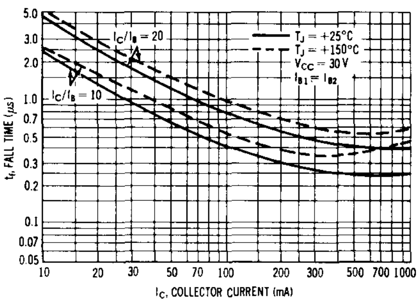


FIGURE 7 — FALL TIME



2N4898 thru 2N4900 (continued)

FIGURE 8 — CURRENT GAIN

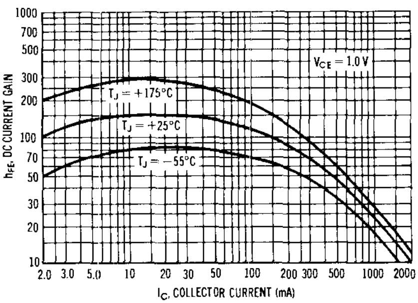


FIGURE 9 — COLLECTOR SATURATION REGION

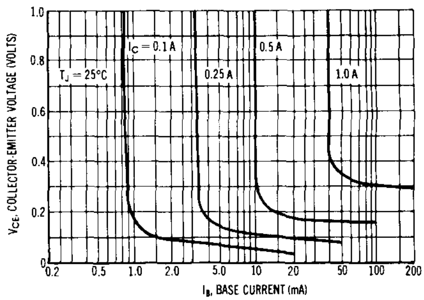


FIGURE 10 — EFFECTS OF BASE-EMITTER RESISTANCE

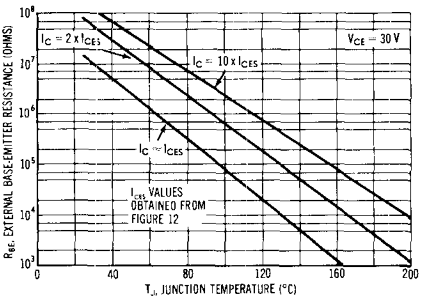


FIGURE 11 — "ON" VOLTAGE

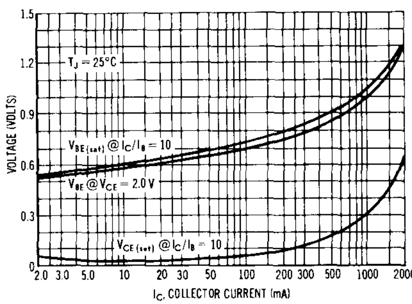


FIGURE 12 — COLLECTOR CUTOFF REGION

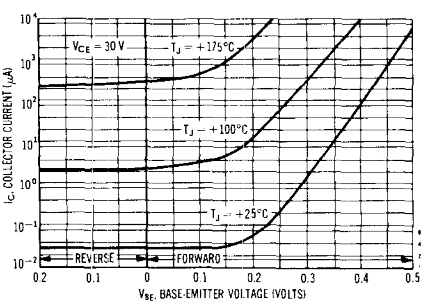
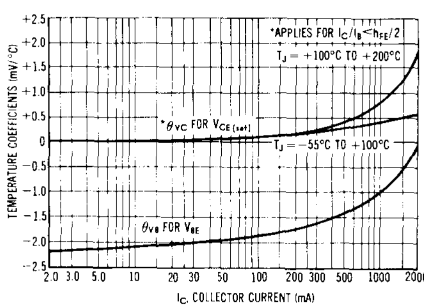
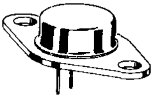


FIGURE 13 — TEMPERATURE COEFFICIENTS



2N4910 thru 2N4912 (SILICON)

V_{CEO} = 40-80 V
I_C = 4 A
P_D = 25 W



CASE 80
(TO-66)

Medium-power NPN silicon transistors designed for driver circuits, switching, and amplifier applications.

MAXIMUM RATINGS

Rating	Symbol	2N4910	2N4911	2N4912	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous*	I_C*	← 1.0 → ← 4.0 →			Adc
Base Current — Continuous	I_B	← 1.0 →			Adc
Total Device Dissipation T_C = 25°C	P_D	← 25 →			Watts
Derate above 25°C		← 0.143 →			mW/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

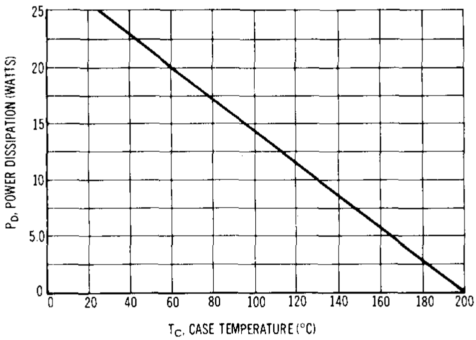
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	7.0	°C/W

* The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements.

The 4.0 Amp maximum value is based upon actual current-handling capability of the device (see Figure 5).

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

2N4910 thru 2N4912 (continued)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0) 2N4910 / 2N4911 / 2N4912	-	$BV_{CEO(sus)}$*	40 / 60 / 80	- / - / -	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) 2N4910 / (V_{CE} = 30 Vdc, I_B = 0) 2N4911 / (V_{CE} = 40 Vdc, I_B = 0) 2N4912	-	I_{CEO}	- / - / -	0.5 / 0.5 / 0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc) / (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	12	I_{CEX}	- / -	0.1 / 1.0	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	-	I_{CBO}	-	0.1	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	-	I_{EBO}	-	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain * (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) / (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) / (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	8	h_{FE}*	40 / 20 / 10	- / 100 / -	-
Collector-Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)	9, 11, 13	$V_{CE(sat)}$*	-	0.6	Vdc
Base-Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)	11, 13	$V_{BE(sat)}$*	-	1.3	Vdc
Base-Emitter On Voltage* (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	11, 13	$V_{BE(on)}$*	-	1.3	Vdc
SMALL SIGNAL CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	-	f_T	3.0	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	-	C_{ob}	-	100	pF
Small-Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	-	h_{fe}	25	-	-

* Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%

FIGURE 2 -- SWITCHING TIME EQUIVALENT CIRCUIT

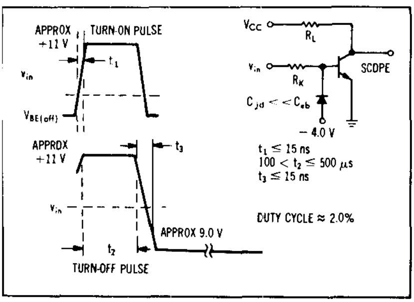
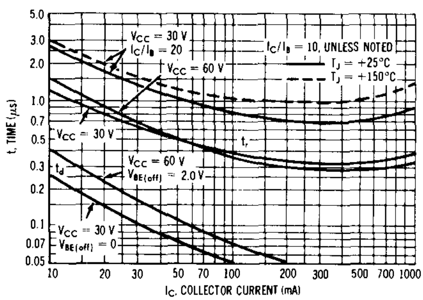


FIGURE 3 — TURN-ON TIME



2N4910 thru 2N4912 (continued)

FIGURE 4 — THERMAL RESPONSE

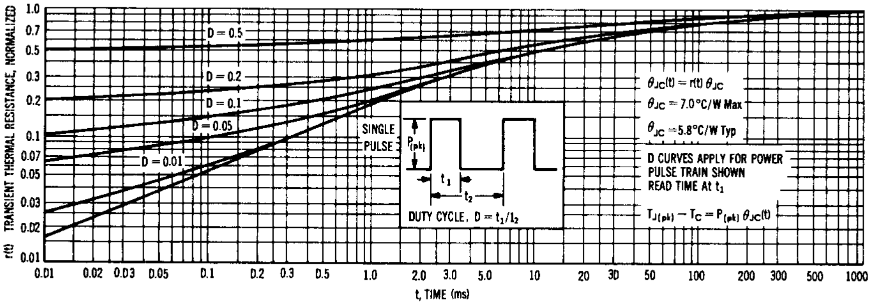
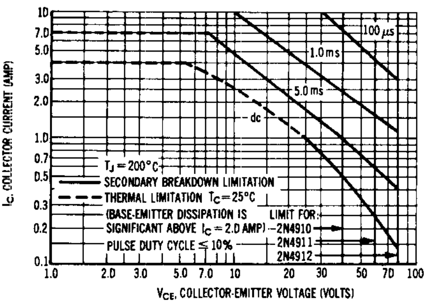


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 — STORAGE TIME

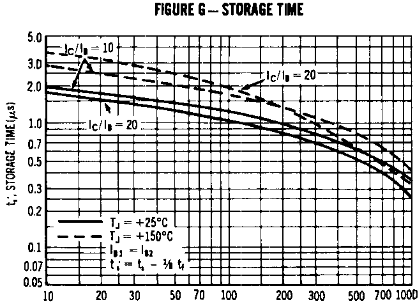
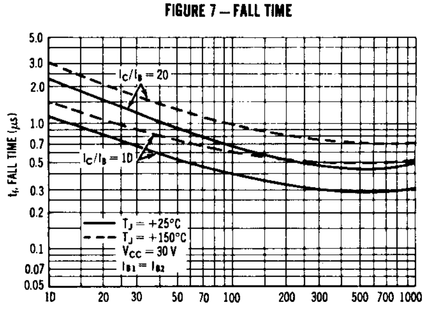


FIGURE 7 — FALL TIME



2N4910 thru 2N4912 (continued)

TYPICAL DC CHARACTERISTICS

FIGURE 8 — CURRENT GAIN

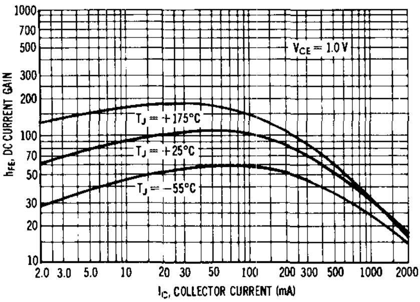


FIGURE 9 — COLLECTOR SATURATION REGION

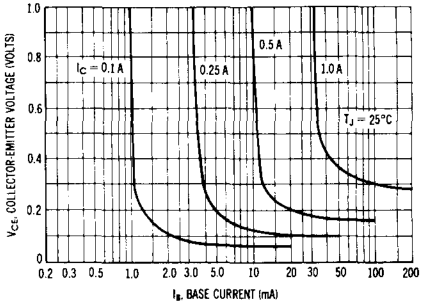


FIGURE 10 — EFFECTS 8F BASE-EMITTER RESISTANCE

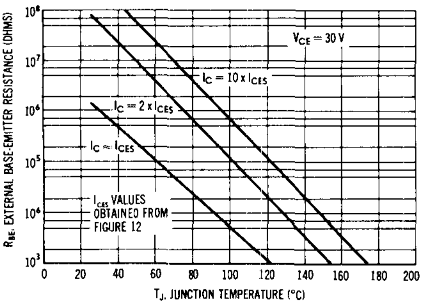


FIGURE 11 — "ON" VOLTAGE

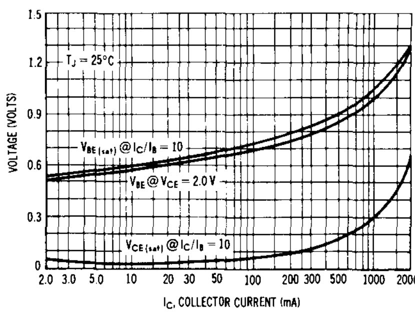


FIGURE 12 — COLLECTOR CUTOFF REGION

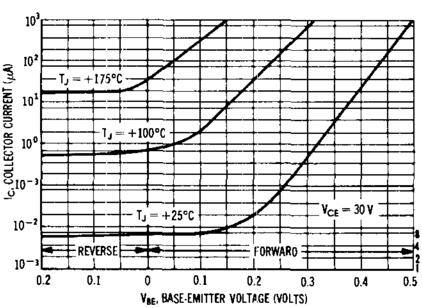
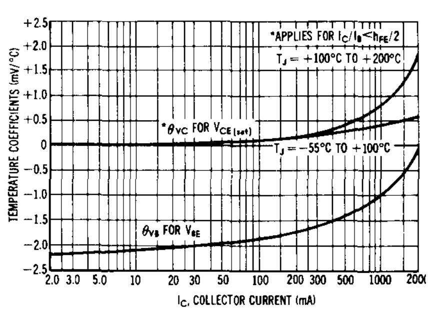


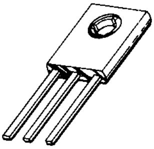
FIGURE 13 — TEMPERATURE COEFFICIENTS



2N4918 thru 2N4920 (SILICON)

V_{CEO} = 40-80 V
I_C = 3 A
P_D = 30 W

CASE 77



Medium-power plastic PNP silicon transistors designed for driver circuits, switching, and amplifier applications.

MAXIMUM RATINGS

Rating	Symbol	2N4918	2N4919	2N4920	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current -- Continuous*	I_C*	← 1.0 → ← 3.0 →			Adc
Base Current	I_B	← 1.0 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 30 → ← 0.24 →			Watts W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

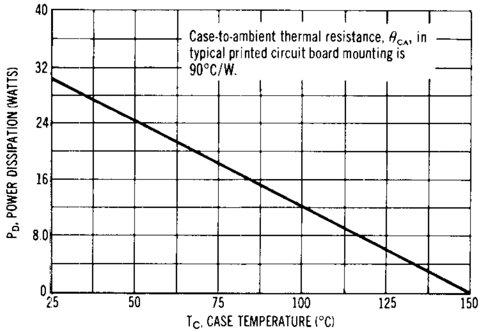
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

* The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements.

The 3.0 Amp maximum value is based upon actual current-handling capability of the device (see Figure 5).

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

2N4918 thru 2N4920 (continued)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0) 2N4918 / 2N4919 / 2N4920	-	$BV_{CEO(sus)}$*	40 / 60 / 80	- / - / -	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	-	I_{CEO}	- / - / -	0.5 / 0.5 / 0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	t2	I_{CEX}	- / -	0.1 / 0.5	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	-	I_{CBO}	-	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	-	I_{EBO}	-	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain* (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	8	h_{FE}*	40 / 20 / 10	- / 100 / -	-
Collector-Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)	9, 11, 13	$V_{CE(sat)}$*	-	0.6	Vdc
Base-Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)	11, 13	$V_{BE(sat)}$*	-	1.3	Vdc
Base-Emitter On Voltage* (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	11, 13	$V_{BE(on)}$*	-	1.3	Vdc
SMALL SIGNAL CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	-	f_T	3.0	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	-	C_{ob}	-	100	pF
Small-Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	-	h_{fe}	25	-	-

* Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%

FIGURE 2 — SWITCHING TIME EQUIVALENT CIRCUIT

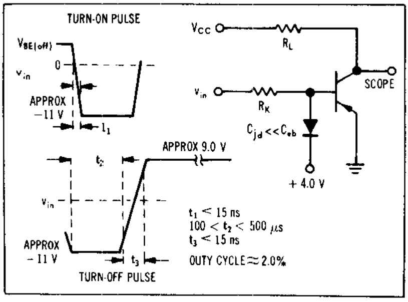
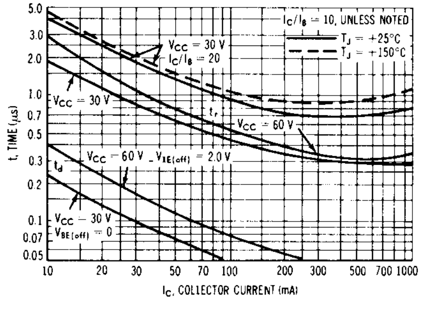


FIGURE 3 — TURN-ON TIME



2N4918 thru 2N4920 (continued)

FIGURE 4 — THERMAL RESPONSE

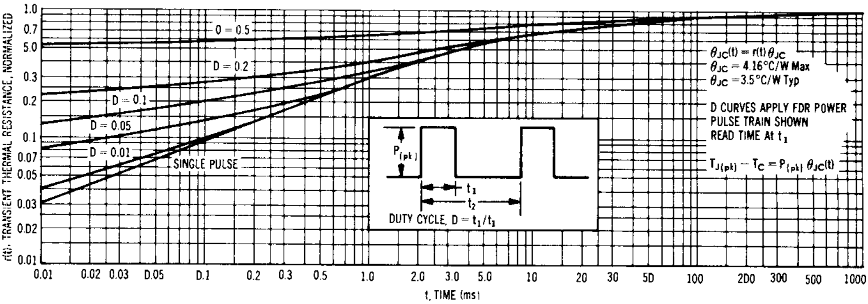
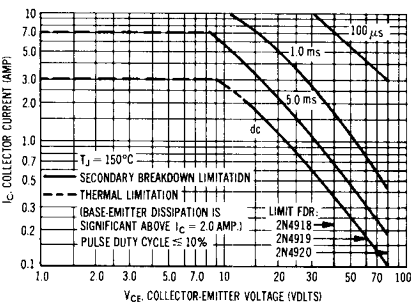


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



The safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor which must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 5 is based upon $T_{J(pk)} = 150°C$; T_C is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power which can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 — STORAGE TIME

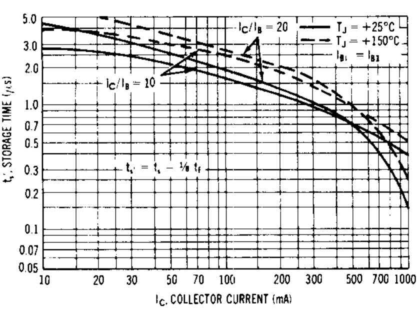
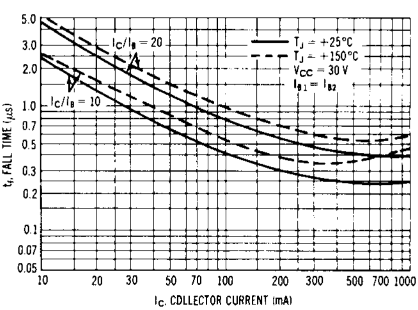


FIGURE 7 — FALL TIME



2N4918 thru 2N4920 (continued)

TYPICAL DC CHARACTERISTICS

FIGURE 8 — CURRENT GAIN

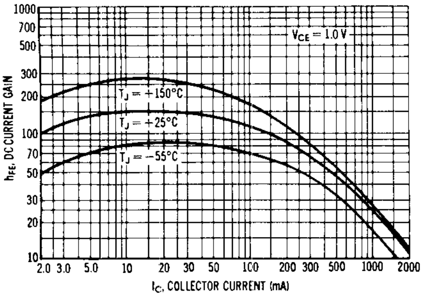


FIGURE 9 — COLLECTOR SATURATION REGION

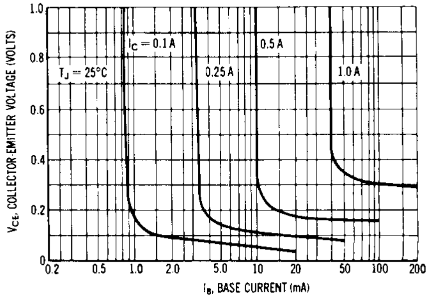


FIGURE 10 — EFFECTS OF BASE-EMITTER RESISTANCE

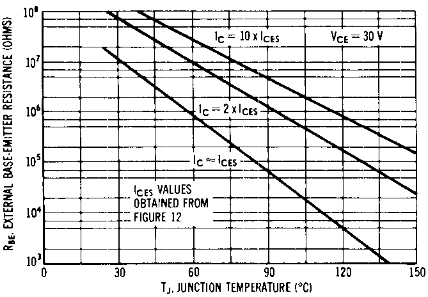


FIGURE 11 — "ON" V8LTAGE

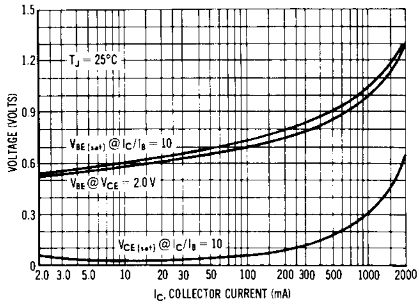


FIGURE 12 — COLLECTOR CUTOFF REGION

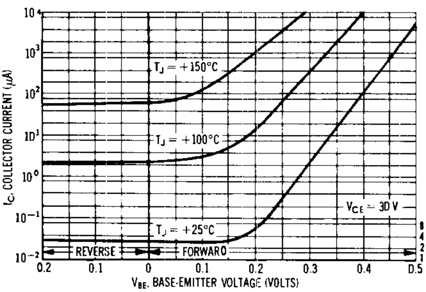
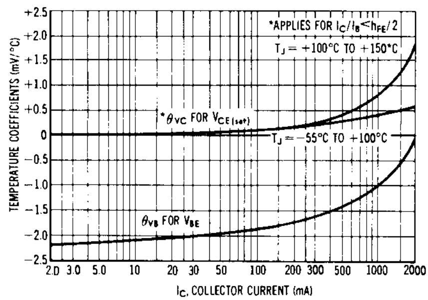


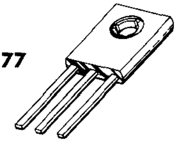
FIGURE 13 — TEMPERATURE COEFFICIENTS



2N4921 thru 2N4923 (SILICON)

V_{CEO} = 40-80 V
I_C = 3 A
P_D = 30 W

CASE 77



Medium-power plastic NPN silicon transistors designed for driver circuits, switching, and amplifier applications.

MAXIMUM RATINGS

Rating	Symbol	2N4921	2N4922	2N4923	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current — Continuous*	I_C*	← 1.0 → ← 3.0 →			Adc
Base Current — Continuous	I_B	← 1.0 →			Adc
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	← 30 → ← 0.24 →			Watts W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

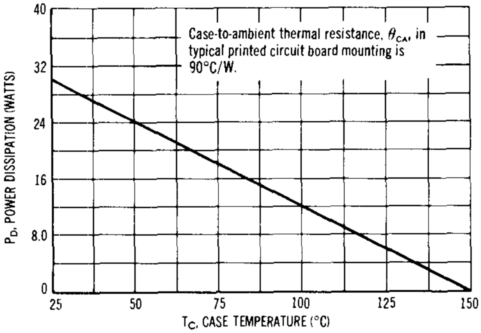
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

* The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements.

The 3.0 Amp maximum value is based upon actual current-handling capability of the device (see Figure 5).

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

2N4921 thru 2N4923 (continued)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Figure No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0) 2N4921 / 2N4922 / 2N4923	-	$BV_{CEO(sus)}$*	40 / 60 / 80	- / - / -	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) 2N4921; (V_{CE} = 30 Vdc, I_B = 0) 2N4922; (V_{CE} = 40 Vdc, I_B = 0) 2N4923	-	I_{CEO}	- / - / -	0.5 / 0.5 / 0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc); (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	12	I_{CEX}	- / -	0.1 / 0.5	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	-	I_{CBO}	-	0.1	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	-	I_{EBO}	-	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain* (I_C = 50 mAdc, V_{CE} = 1.0 Vdc); (I_C = 500 mAdc, V_{CE} = 1.0 Vdc); (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	8	h_{FE}*	40 / 20 / 10	- / 100 / -	-
Collector-Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)	9, 11, 13	$V_{CE(sat)}$*	-	0.6	Vdc
Base-Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)	11, 13	$V_{BE(sat)}$*	-	1.3	Vdc
Base-Emitter On Voltage* (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	11, 13	$V_{BE(on)}$*	-	1.3	Vdc
SMALL SIGNAL CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	-	f_T	3.0	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	-	C_{ob}	-	100	pF
Small-Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	-	h_{fe}	25	-	-

* Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%.

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

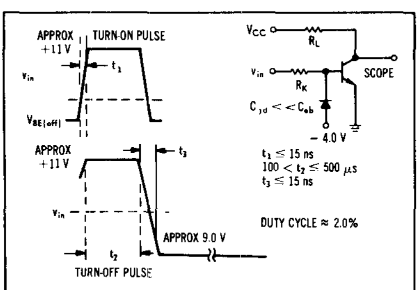
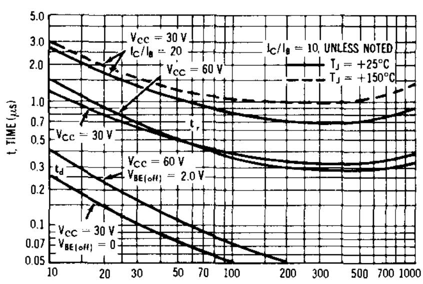


FIGURE 3 – TURN-ON TIME



2N4921 thru 2N4923 (continued)

FIGURE 4 — THERMAL RESPONSE

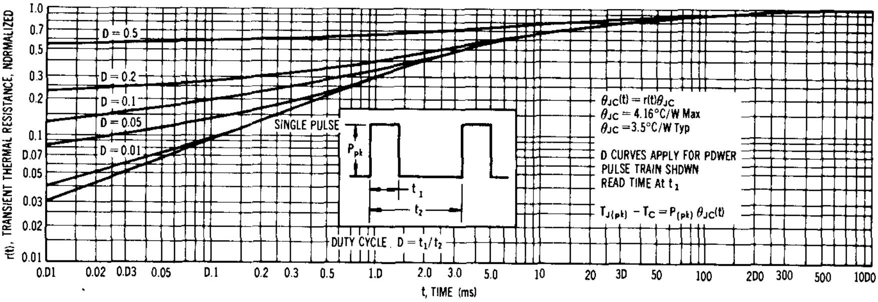
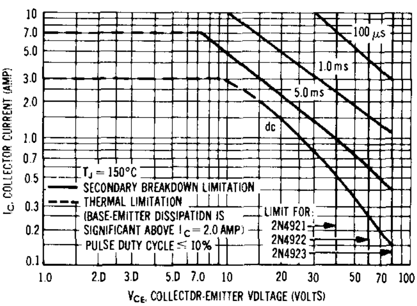


FIGURE 5 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 — STORAGE TIME

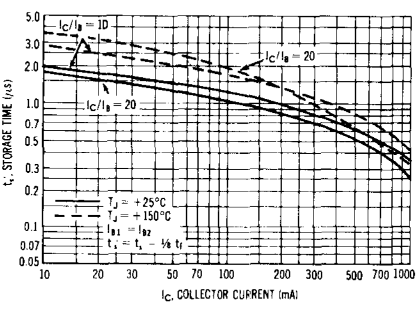
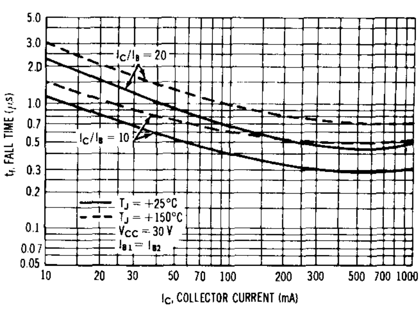


FIGURE 7 — FALL TIME



2N4921 thru 2N4923 (continued)

FIGURE 8 — CURRENT GAIN

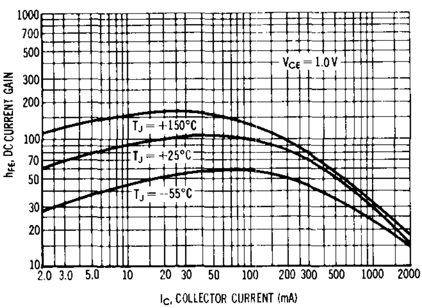


FIGURE 9 — COLLECTOR SATURATION REGION

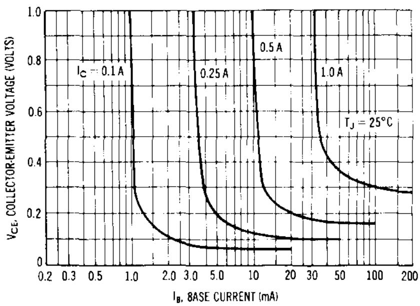


FIGURE 10 — EFFECTS OF BASE-EMITTER RESISTANCE

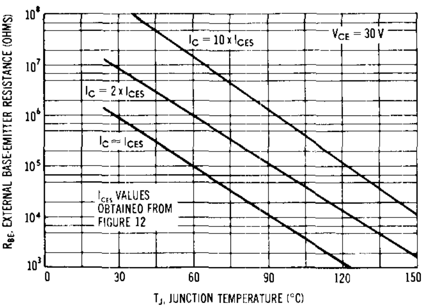


FIGURE 11 — "ON" VOLTAGE

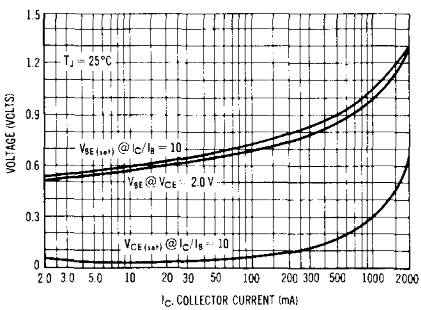


FIGURE 12 — COLLECTOR CUTOFF REGION

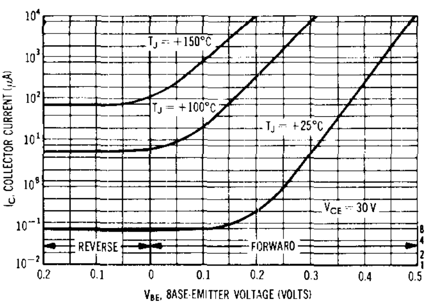
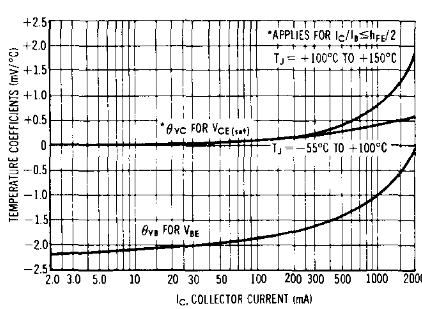
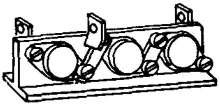


FIGURE 13 — TEMPERATURE COEFFICIENTS



MP800 (GERMANIUM)
MP801

V_{CEO} = 45-60 V
I_C = 150 A
P_D = 250 W



CASE 118

PNP germanium power transistor designed for ultra-high current applications requiring high gain and extremely low saturation voltage.

MAXIMUM RATINGS

Rating	Symbol	MP800/MP801		Unit
Collector-Emitter Voltage	V_{CEO}	60	45	Vdc
Collector-Emitter Voltage	V_{CES}	75	60	Vdc
Emitter-Base Voltage	V_{EB}	20		Vdc
Collector Current*	I_C*	150		Amp
Total Device Dissipation @ T_C = 25°C	P_D	250		Watts
Operating Junction Temperature Range	T_J	-65 to +110		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.33	°C/W

ELECTRICAL CHARACTERISTICS

** For Epoxy Encapsulated unit, add "A" to device type, i.e. MP800A

(T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 Adc, I_B = 0)	MP800	BV_{CEO}	60	-	Vdc
	MP801		45	-	
Collector Cutoff Current (V_{CB} = 75 Vdc, I_E = 0)	MP800	I_{CBO}	-	12	mAdc
(V_{CB} = 60 Vdc, I_E = 0)	MP801		-	12	
ON CHARACTERISTICS					
DC Current Gain (I_C = 150 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	15	-	-
Collector-Emitter Saturation Voltage (I_C = 150 Adc, I_B = 15 Adc)		$V_{CE(sat)}$	-	0.30	Vdc
Base-Emitter Saturation Voltage (I_C = 150 Adc, I_B = 15 Adc)		$V_{BE(sat)}$	-	1.0	Vdc
Safe Operating Area (Figure 1) 100% Test - Clamped V_{CE}	MP800	SOA	-	45	Volts
	MP801		-	40	

* For currents above 150 Amp, contact your local Motorola representative.

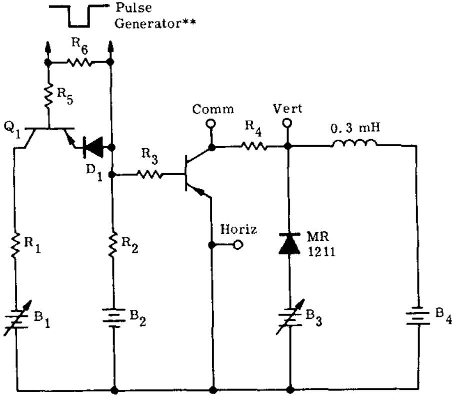
MP800, MP801 (continued)

FIGURE 1 — SAFE OPERATING AREA TEST CURRENT

R_1 = 1.0Ω, 200 W
R_2 = 10Ω, 2.0 W
R_3 = 0.1Ω, 1%, 20 W
R_4 = 0.001Ω
R_5 = 10Ω, 2.0 W
R_6 = 50Ω, 1.0 W
Q_1 = 2N2832
D_1 = 1N1183

B_1 = Adj for $I_{B(on)}$ = 15 A
B_2 = 6.0 V
B_3 = Adj for clamped V_{CE}
B_4 = 20 V

** Adj P. W. to obtain I_C = 150 A



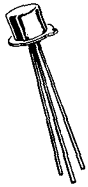
SWITCHING AND GENERAL PURPOSE TRANSISTORS

THE FOLLOWING TRANSISTORS ARE INCLUDED IN THIS SECTION

JAN2N559-1	2N2845	2N4890
JAN2N559-2	2N2846	2N4924
JAN2N559-3	2N2847	2N4925
2N699	2N2848	2N4926
2N702	2N3009	2N4927
2N703	2N3010	2N4928
JAN2N703	2N3011	2N4929
2N709	2N3013	2N4930
2N721	2N3014	2N4931
2N731	2N3015	2N5086
2N743	2N3053	2N5087
2N1708	2N3210	2N5088
2N1959	2N3211	2N5089
2N1990	2N3299	AF239
2N2224	2N3300	MM4000
2N2242	2N3301	MM4001
2N2410	2N3302	MM4002
2N2476	2N4123	MM4003
2N2477	2N4124	MM5000
JAN2N2709	2N4125	MM5001
2N2710	2N4126	MM5002
		MPS2369

JAN 2N559-1
JAN 2N559-2
JAN 2N559-3*

$V_{CES} = 15\ V$
$I_C = 50\ mA$
$P_D = 150\ mW$



CASE 22
(TO-18)

PNP germanium mesa transistors designed for military and industrial high-reliability, high-speed switching applications.

Collector connected to case

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CES}	15	Vdc
Collector-Base Voltage	V_{CB}	15	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current	I_C	50	mAdc
Base Current	I_B	50	mAdc
Emitter Current	I_E	50	mAdc
Total Device Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	150 2.0	mW mW/^oC
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	300 4.0	mW mW/^oC
Operating Junction Temperature Range	T_J	-65 to +100	^oC
Storage Temperature Range	T_{stg}	-65 to +150	^oC

* Level 3 reliability data shown for information only. Qualification tests will be initiated upon established customer requirements.

JAN 2N559-1, -2, -3 (Continued)

RELIABILITY RATINGS†

Reliability Level Indicator	QUALITY LEVELS (LTPD) Group A Subgroups		QUALITY LEVELS (LTPD) Group B Subgroups		RELIABILITY LEVELS Maximum failure rate (λ) during first 1000 hours with 90% confidence. Operation Life $P_D = 150$ mW, $I_E = 50$ mA, $T_A = 25°C$		Storage Life $T_A = 100°C$		Storage Life $T_A = 150°C$		Est. Max Failure Rate in Conservatively Designed Equipment %/1000 Hrs
	Major Defect	Minor Defect	Major Defect	Minor Defect	Major Defect	Minor Defect	Major Defect	Minor Defect	Major Defect	Minor Defect	
-1	3.0	5.0	10	20	10	20	10	20	20	—	0.1
-2	1.5	3.0	5	15	5	15	1.5	3	7	20	0.01
-3*	1.0	2.0	3	7	2	5	0.2	0.5	1	3	0.001

† This table relates the statistical sampling requirements in the specification to the reliability levels for the transistor.

* Level 3 reliability data shown for information only. Qualification tests will be initiated upon established customer requirements.

TABLE I – GROUP A INSPECTION**

Examination or Test	MIL-STD-750 Method	LTPD for Respective Reliability Level Minor -1	Minor -2	Minor -3	Major -1	Major -2	Major -3	Symbol	Limit Minor Min	Limit Minor Max	Limit Major Min	Limit Major Max	Unit
SUBGROUP 1													
Visual and Mechaniral Examination	2071	10	7	5	7	5	3	-	-	-	-	-	
SUBGROUP 2		5	3	2	3	1.5	1.0						
Emittrr-Base Cutoff Current (V_{EB} = -1 Vdr)	3061 Condition D							I_{EBO}	-	5	-	10	µAdc
Collector-Base Cutoff Current (V_{CB} = -5 Vdc)	3036 Condition D							I_{CBO}	-	3	-	5.0	µAdc
Emitter-Base Breakdown Voltage (I_E = -200 µAdc)	3026 Condition O							BV_{EBD}	5	-	3.5	-	Vdr
Collector-Emitter Breakdown Voltage (I_C = -100 µAdc)	3011 Condition C							BV_{CES}	15	-	12	-	Vdc
SUBGROUP 3		5	3	2	3	1.5	1.0						
Collector-Emitter Saturation Voltage (I_C = -50 mAdc, I_B = -1.5 mAdc)	3071							$V_{CE(sat)}$	-	1	-	1.2	Vdc
(I_C = -10 mAdc, I_B = -0.4 mAdc)									-	0.3	-	0.35	
Base-Emitter Saturation Voltage (I_C = -10 mAdc, I_B = -0.4 mAdc)	3066 Condition A							$V_{BE(sat)}$	0.32	0.44	0.30	0.50	Vdc
DC Current Gain (I_C = -10 mAdc, V_{CE} = -0.5 Vdr)	3076							h_{FE}	25	150	20	200	-
SUBGROUP 4		5	3	2	3	1.5	1.0						
Rise Time (V_{CC} = -3.5 Vdc, $V_{BE(off)}$ = 0.5 Vdc, I_{B1} = -0.55 mAdc, R_C = 300 ohms, C_{CE} = 150 pF, $C_{CB} = 2^{+0.5}_{-0}$ pF)	3251 Condition A							t_r	-	95	-	115	ns
Storage Time (V_{CC} = -3.5 Vdc, I_{B1} = -1 mAdr, I_{B2} = 0.25 mAdc, R_C = 300 ohms)	3251 Condition A							t_s	-	95	-	115	ns
Fall Time (V_{CC} = -3.5 Vdc, I_{B1} = -1 mAdr, I_{B2} = 0.25 mAdc, R_C = 300 ohms, $C_{CB} = 2^{+0.5}_{-0}$ pF)	3251 Condition A							t_f	-	100	-	120	ns

**These tests are cnnsidered non-destructive.

JAN 2N559-1, -2, -3 (Continued)

TABLE II – GROUP B INSPECTION

Examination or Test	MIL-STD-750 Method	LTPD for Respective Reliability Level						Symbol	Limit				Unit
		Minor			Major				Minor		Major		
		-1	-2	-3	-1	-2	-3		Min	Max	Min	Max	
SUBGROUP 1													
Physical Dimensions	2066	20	15	7	-	-	-	-	-	-	-	-	-
SUBGROUP 2													
Tension	2036 Condition A	20	15	7	10	5	3	-	-	-	-	-	-
Solderability, Omit Aging	2036							-	-	-	-	-	-
Temperature Cycling (5 cycles) $T_{(high)} = 100 ^{+5}_{-0}$ °C 2N559-1; $T_{(high)}$ = :5 °C 2N559-2, 2N559-3	1051 Condition F							-	-	-	-	-	-
Thermal Shock (Glass Strain)	1056 Condition A							-	-	-	-	-	-
Moisture Resistance (No initial conditioning; one cycle; only steps 1 to 6)	1021							-	-	-	-	-	-
End-Point Tests:													
Emitter-Base Cutoff Current (V_{EB} = -1 Vdc)	3061 Condition D							I_{EBO}	-	10	-	20	μAdc
Collector-Base Cutoff Current (V_{CB} = -5 Vdc)	3036 Condition D							I_{CBO}	-	5	-	10	μAdc
DC Current Gain (I_C = -10 mAdc, V_{CE} = -0.5 Vdc)	3076							h_{FE}	20	200	15	250	-
SUBGROUP 3		20	15	7	10	5	3						
Shock (Non-operating; 5 blows: 1500 G, 0.5 ms Orientations X_1, Y_1, Y_2, and Z_1 (total = 20 blows)	2016							-	-	-	-	-	-
Constant Acceleration (20,000 G, Orientations X_1, Y_1, Y_2, and Z_1)	2006							-	-	-	-	-	-
Vibration, Variable Frequency (1 cycle each in Orientations X_1, Y_1, and Z_1)	2056							-	-	-	-	-	-
End-Point Tests: Same as Subgroup 2													
SUBGROUP 4		20	15	7	-	-	-						
Terminal Strength - Lead Fatigue ①	2036 Condition E							-	-	-	-	-	-
SUBGROUP 5		20	15	3	10	7	1						
High-Temperature Life (Non-operating) ($T_{stg} = 150 ^{+0}_{-0}$ °C)	1031							-	-	-	-	-	-
End-Point Tests: Same as Subgroup 2													
SUBGROUP 6		20	15	5	10	5	2						
Steady-State Operation Life ($I_E = 50 ^{+0}_{-5}$ mAdc, $P_D = 150 ^{+0}_{-15}$ mW, T_A = 25 +3°C)	1026							-	-	-	-	-	-
End-Point Tests: Same as Subgroup 2													

NOTE: ① Rejects from prior electrical-test samples from the same lot may be used for this test.

JAN 2N559-1, -2, -3 (Continued)

TABLE III – GROUP C INSPECTION*

Examination or Test	MIL-STD-750 Method	LTPD for Respective Reliability Level						Symbol	Limit				Unit
		Minor			Major				Minor		Major		
		-1	-2	-3	-1	-2	-3		Min	Max	Min	Max	
SUBGROUP 1		10	7	5	5	3	2						
Output Capacitance (V_{CB} = -5 Vdc, I_E = 0, f = 100 kHz)	3236							C_{ob}	-	6	-	10	pF
Current-Gain — Bandwidth Product (I_E = 10 mAdc, V_C = -1 Vdc, f = 100 MHz)	3261							f_T	300	1000	250	1000	MHz
Delay Plus Rise Time (V_{CC} = -3.5 Vdc, $V_{BE(off)}$ = 0.5 Vdc, I_{B1} = -1 mAdc, R_C = 300 ohms, C_{CB} = $2^{+0.5}_{-0}$ pF, C_{BE} = 2 ± 0.5 pF	3251 Condition A							$t_d + t_r$	-	50		75	ns
SUBGROUP 2		10	7	5	5	3	2						
Collector-Emitter Cutoff Current (V_{CE} = 5 Vdc, T_A = + 55°C)	3041 Condition C							I_{CES}	-	40	-	50	μAdc
DC Current Gain (I_C = -10 mAdc, V_{CE} = -0.5 Vdc, T_A = -55°C)	3076							h_{FE}	10	-	8.0	-	-
SUBGROUP 3		20	15	7	-	-	-						
Salt Atmosphere (Corrosion)	1041							-	-	-	-	-	-
End-Point Tests: Same as Group B, Subgroup 2													
SUBGROUP 4		-	20	10	-	10	5						
High-Temperature Life (Non-operating) (T_{stg} = 100^{+0}_{-5} °C)	1031							-	-	-	-	-	-
End-Point Tests:													
Emitter-Base Breakdown Voltage (I_E = -300 μAdc)	3026 Condition D							BV_{EBO}	5	-	3.5	-	Vdc
Collector-Emitter Breakdown Voltage (I_C = -100 μAdc)	3011 Condition C							BV_{CES}	12	-	8.0	-	Vdc
Collector-Emitter Saturation Voltage (I_C = -10 mAdc, I_B = -0.5 mAdc)	3071							$V_{CE(sat)}$	-	0.3	-	0.6	Vdc
Base-Emitter Saturation Voltage (I_C = -10 mAdc, I_B = -0.4 mAdc)	3066 Condition A							$V_{BE(sat)}$	0.31	0.47	0.25	0.55	Vdc
Delay Time (V_{CC} = -3.5 Vdc, $V_{BE(off)}$ = 0.5 Vdc, I_{B1} = -0.55 mAdc, R_C = 300 ohms, C_{CE} = 150 pF, C_{CB} = $2^{+0.5}_{-0}$ pF, C_{BE} = 2 ± 0.5 pF)	3251 Condition A							t_d	10	35	10	45	ns
Rise Time (V_{CC} = -3.5 Vdc, $V_{BE(off)}$ = 0.5 Vdc, I_{B1} = -0.55 mAdc, R_C = 300 ohms, C_{CE} = 150 pF, C_{CB} = $2^{+0.5}_{-0}$ pF)	3251 Condition A							t_r	15	105	15	125	ns
Storage Time (V_{CC} = -3.5 Vdc, I_{B1} = -1 mAdc, I_{B2} = 0.25 mAdc, R_C = 300 ohms)	3251 Condition A							t_s	15	105	15	125	ns

* Group C is to be performed on the first lot and every 6 months thereafter.

2N699 (SILICON)

V_{CB} = 120 V
f_T = 50 MHz (min)
P_D = 0.6 W

NPN silicon annular transistor designed for medium-current switching and amplifier applications.

CASE 79
(TO-39)

Collector connected to case

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CER}	80	Vdc
Collector-Base Voltage	V_{CB}	120	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	0.6 4.0	Watt mW/°C
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	2.0 13.3	Watts mW/°C
Operating Junction Temperature Range	T_J	175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	75	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	250	°C/W

2N699 (continued)

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage* (I_C = 100 mAdc, $R_{BE} \leq 10$ ohms)	BV_{CER}*	80	-	Vdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0)	I_{CBO}	-	2.0	μAdc
(V_{CB} = 60 Vdc, I_E = 0, T_A = 150°C)		-	200	
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, I_C = 0)	I_{EBO}	-	100	μAdc
ON CHARACTERISTICS				
DC Current Gain* (I_C = 150 mAdc, V_{CE} = 10 Vdc)	h_{FE}*	40	120	-
Collector-Emitter Saturation Voltage* (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{CE(sat)}$*	-	5.0	Vdc
Base-Emitter Saturation Voltage* (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{BE(sat)}$*	-	1.3	Vdc
SMALL SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)	f_T	50	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	-	20	pF
Input Impedance (I_C = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz)	h_{ib}	20	30	ohms
(I_C = 5.0 mAdc, V_{CB} = 10 Vdc, f = 1.0 kHz)		-	10	
Voltage Feedback Ratio (I_C = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz)	h_{rb}	-	2.5	$X\ 10^{-4}$
(I_C = 5.0 mAdc, V_{CB} = 10 Vdc, f = 1.0 kHz)		-	3.0	
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	h_{fe}	35	100	-
(I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		45	-	
Output Admittance (I_C = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz)	h_{ob}	0.1	0.5	μmhos
(I_C = 5.0 mAdc, V_{CB} = 10 Vdc, f = 1.0 kHz)		-	1.0	

* Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2%.

2N702 (SILICON) 2N703 (JAN 2N703 ALSO AVAILABLE)

V_{CEO} = 25 V
I_C = 50 mA
P_D = 300 mW

NPN silicon annular transistor designed for low-level, high-speed switching applications.

CASE 22
(TO-18)

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Collector-Base Voltage	V_{CB}	25	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	50	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 2.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	600 4.0	mW mW/°C
Operating and Storage Junction Temperature Range	T_{stg}	-65 to +175	°C

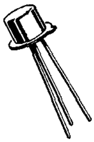
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 2.0 mAdc, I_B = 0)	BV_{CEO}	25	-	-	Vdc
Collector-Base Breakdown Voltage (I_C = 5.0 μAdc, I_E = 0)	BV_{CBO}	25	-	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0	-	-	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0)	I_{CEO}	-	-	10	μAdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0) (V_{CB} = 10 Vdc, I_E = 0, T_A = +150°C)	I_{CBO}	 - -	 - -	 0.5 50	μAdc
ON CHARACTERISTICS					
DC Current Gain* (I_C = 10 mAdc, V_{CE} = 5.0 Vdc) 2N702 2N703 (I_C = 10 mAdc, V_{CE} = 5.0 Vdc, T_A = -55°C) 2N702 2N703	h_{FE}*	 20 40 12 20	 - - - -	 60 100 - -	-
Collector-Emitter Saturation Voltage* (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$*	-	-	0.5	Vdc
Base-Emitter On Voltage* (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$*	0.7	-	0.95	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_E = 10 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	70	150		MHz
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	-	3.0	6.0	pF

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

2N709 (SILICON)

$V_{CEO} = 6\ V$
$I_C = 100\ mA$
$P_D = 300\ mW$



CASE 22
(TO-18)

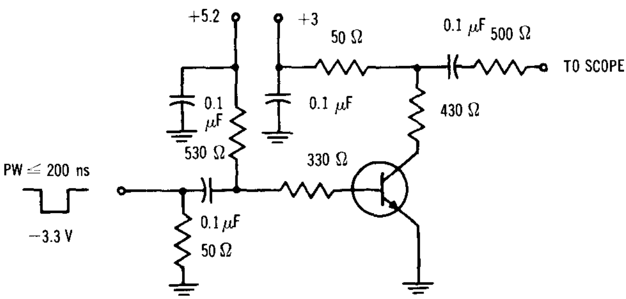
Collector connected to case

NPN silicon annular transistor designed for ultra-high speed switching applications.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	6	Vdc
Collector-Base Voltage	V_{CB}	15	Vdc
Emitter-Base Voltage	V_{EB}	4	Vdc
Collector Current	I_C	100	mAdc
Total Device Dissipation $T_A = 25^oC$ Derate above 25^oC	P_D	300 1.71	mWatts $mW/^oC$
Total Device Dissipation $T_C = 100^oC$ Derate above 100^oC	P_D	500 2.0	mWatts $mW/^oC$
Operating & Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC
Lead Temperature (Soldering, 10 second time limit)	-	300	^oC

FIGURE 1 – STORAGE TIME CONSTANT TEST CIRCUIT



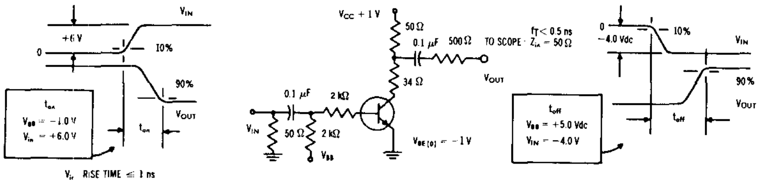
2N709 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage* (I_C = 10 mAdc, I_B = 0)	$BV_{CEO(sus)}$*	6	-	-	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BV_{CBO}	15	-	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	4	-	-	Vdc
Collector Cutoff Current (V_{CB} = 5 Vdc, I_E = 0) (V_{CB} = 5 Vdc, I_E = 0, T_A = 125°C)	I_{CBO}	- -	0.002 0.5	0.05 5.0	μAdc
ON CHARACTERISTICS					
DC Current Gain* (I_C = 10 mAdc, V_{CE} = 0.5 Vdc) (I_C = 10 mAdc, V_{CE} = 0.5 Vdc, T_A = -55°C) (I_C = 30 mAdc, V_{CE} = 1 Vdc)	h_{FE}*	20 10 15	- - -	120 - -	-
Collector-Emitter Saturation Voltage (I_C = 3 mAdc, I_B = 0.15 mAdc)	$V_{CE(sat)}$	-	0.2	0.3	Vdc
Base-Emitter Saturation Voltage (I_C = 3 mAdc, I_B = 0.15 mAdc)	$V_{BE(sat)}$	0.70	-	0.85	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 5 mAdc, V_{CE} = 4 Vdc, f = 100 MHz)	f_T	600	-	-	MHz
Output Capacitance (V_{CB} = 5 Vdc, I_E = 0)	C_{ob}	-	-	3	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0)	C_{ib}	-	-	2	pF
Turn-On Time, Figure 2 (V_{CC} = 1 Vdc, V_{EB} (off) = 1 Vdc, I_C = 10 mAdc, I_{B1} = 2 mAdc, I_{B2} = 1.0 mA)	t_{on}	-	8	15	ns
Turn-Off Time, Figure 2 (V_{CC} = 1 Vdc, I_C = 10 mAdc, I_{B1} = I_{B2} = 1 mAdc)	t_{off}	-	6	15	ns
Storage Time, Figure 1 (I_C = 5 mAdc, I_{B1} = I_{B2} = 5 mAdc)	t_s	-	-	6	ns

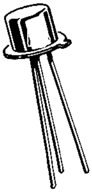
*Pulse Test: Pulse Width = 300 μs; Duty Cycle = 2%

FIGURE 2 — TURN-ON & TURN-OFF TIME TEST CIRCUIT



2N721 (SILICON)

V_{CB} = 50 V
f_T = 50 MHz min



CASE 22
(TO-18)

PNP silicon annular transistor for high-frequency general-purpose amplifier applications.

Collector connected to case

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	35	Vdc
Collector-Emitter Voltage	V_{CER}	50	Vdc
Collector - Base Voltage	V_{CB}	50	Vdc
Emitter - Base Voltage	V_{EB}	5.0	Vdc
Total Device Dissipation @ T_A=25°C (Derate above 25°C)	P_D	0.40 2.67	Watts mW/°C
Total Device Dissipation @ T_C=25°C T_C=100°C (Derate above 25°C)	P_D	1.5 0.75 10	Watts mW/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

2N721 (continued)

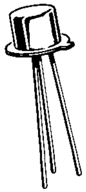
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage* (I_C = 100 mAdc, I_B = 0)	$BV_{CEO(sus)}$*	35	-	Vdc
Collector-Emitter Sustaining Voltage* (I_C = 100 mAdc, $R_{BE} \leq$ 100 ohms)	$BV_{CER(sus)}$*	50	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	50	-	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_A = 150°C)	I_{CBO}	- -	1.0 100	μAdc
Emitter Cutoff Current (V_{BE} = 2.0 Vdc, I_C = 0)	I_{EBO}	-	100	μAdc
ON CHARACTERISTICS				
DC Current Gain* (I_C = 150 mAdc, V_{CE} = 10 Vdc) (I_C = 5.0 mAdc, V_{CE} = 10 Vdc)	h_{FE}*	20 15	45 -	-
Collector-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{CE(sat)}$	-	1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{BE(sat)}$	-	1.3	Vdc
SMALL SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)	f_T	50	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	-	45	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0)	C_{ib}	-	100	pF
Input Impedance (I_C = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz) (I_C = 5.0 mAdc, V_{CB} = 10 Vdc, f = 1.0 kHz)	h_{ib}	25 -	35 10	ohms
Voltage Feedback Ratio (I_C = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz) (I_C = 5.0 mAdc, V_{CB} = 10 Vdc, f = 1.0 kHz)	h_{rb}	- -	8.0 8.0	$X10^{-4}$
Small Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz) (I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	15 20	50 -	
Output Admittance (I_C = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz) (I_C = 5.0 mAdc, V_{CB} = 10 Vdc, f = 1.0 kHz)	h_{ob}	- -	1.0 5.0	μmhos

* Pulse Test: Pulse Width = 300 μs; Duty Cycle = 1.0%

2N731 (SILICON)

V_{CER} = 40 V
I_C = 1.0 A
P_D = 0.5 W



CASE 22
(TO-18)

Collector electrically connected to case

NPN silicon transistor designed primarily for large-signal, medium power audio frequency applications in industrial service.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage (R_{BE} = ≦ 10 ohms)	V_{CER}	40	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	1.0	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.5 3.33	Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 10	Watts mW/°C
Operating Junction Temperature Range	T_J	+175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

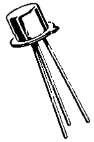
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage* (I_C = 100 mAdc, R_{BE} = 10 ohms)	BV_{CER}*	40	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	60	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	5.0	-	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_A = 150°C)	I_{CBO}	 - -	 1.0 100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 150 mAdc, V_{CE} = 10 Vdc)	h_{FE}	40	120	-
Collector-Emitter Saturation Voltage* (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{CE(sat)}$*	-	1.5	Vdc
Base-Emitter Saturation Voltage* (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{BE(sat)}$*	-	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)	f_T	25	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	-	35	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{ib}	-	80	pF

* Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

2N743

V_{CEO} = 12 V
I_C = 200 mA
f_T = 282 MHz min



CASE 22
(TO-18)

NPN silicon annular transistor designed for high-speed, low-current, saturated switching operations.

Collector connected to case

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	12	Vdc
Collector-Base Voltage	V_{CB}	20	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current - Continuous	I_C	200	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 1.71	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

SWITCHING TEST CIRCUITS

FIGURE 1 — TURN-ON AND TURN-OFF TIME TEST CIRCUIT

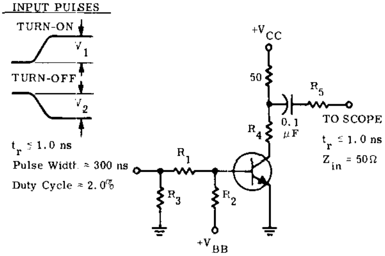
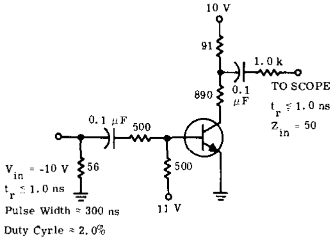


FIGURE 2 — CHARGE-STORAGE TIME TEST CIRCUIT



CIRCUIT CONDITIONS									
	(VOLTS)					(OHMS)			
	t_{on}		t_{off}						
Condition	V_1	V_{BB}	V_2	V_{BB}	V_{CC}	$R_1 = R_2$	R_3	R_4	R_5
1	15	-3.0	-15	+12	3.0	3.3 k	50	220	-
2	20	-4.5	-20	+15.3*	6.0	330	56	-	1.0 k

* V_{BB} is pulsed for 1.5 s at less than 10% Duty Cycle to maintain $T_C < 30°C$.

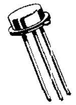
2N743 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	12	-	Vdc
Collector-Cutoff Current (V_{CE} = 20 Vdc, V_{BE} = 0)	I_{CES}	-	1.0	μAdc
(V_{CE} = 20 Vdc, V_{BE} = 0, T_A = 170°C)		-	100	
Collector Cutoff Current (V_{CE} = 10 Vdc, $V_{EB(off)}$ = 0.35 Vdc, T_A = 100°C)	I_{CEX}	-	30	μAdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	-	1.0	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	-	10	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 1.0 mAdc, V_{CE} = 0.25 Vdc)	h_{FE}	10	-	-
(I_C = 10 mAdc, V_{CE} = 0.35 Vdc)		20	60	
(I_C = 10 mAdc, V_{CE} = 0.35 Vdc, T_A = -55°C)		10	-	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)		10	-	
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc, T_A = 170°C)	$V_{CE(sat)}$	-	0.35	Vdc
(I_C = 100 mAdc, I_B = 10 mAdc, T_A = 170°C)		-	1.0	
(I_C = 10 mAdc, I_B = 1.0 mAdc, T_A = -55°C)		-	1.1	
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$	0.65	0.85	Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc, T_A = -55°C)		-	1.1	
(I_C = 100 mAdc, I_B = 10 mAdc)		-	1.5	
(I_C = 100 mAdc, I_B = 10 mAdc, T_A = -55°C)		-	1.6	
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	282	-	MHz
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	-	5.0	pF
Turn-On Time (V_{CC} = 3.0 Vdc, $V_{BE(off)}$ = 1.5 Vdc, I_C = 10 mAdc, I_{B1} = 3.0 mAdc, Condition 1)	t_{on}	-	16	ns
(V_{CC} = 6.0 Vdc, $V_{BE(off)}$ = 2.4 Vdc, I_C = 100 mAdc, I_{B1} = 40 mAdc, Figure 1, Condition 2)		-	12	
Turn-Off Time (V_{CC} = 3.0 Vdc, I_C = 10 mAdc, I_{B1} = 3.0 mAdc, I_{B2} = 1.5 mAdc, Condition 1)	t_{off}	-	24	ns
(V_{CC} = 6.0 Vdc, I_C = 100 mAdc, I_{B1} ≈ 40 mAdc, I_{B2} ≈ 20 mAdc, Figure 1, Condition 2)		-	40	
Storage Time (I_C = 10 mAdc, I_{B1} = I_{B2} = 10 mAdc, V_{CC} = 10 Vdc, Figure 2)	t_s	-	14	ns

2N1708 (SILICON)

V_{CEO} = 12 V
I_C = 200 mA
P_D = 300 mW



CASE 26
(TO-46)

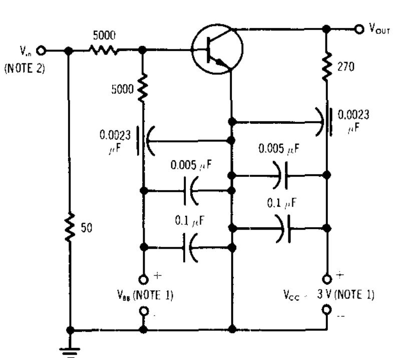
Collector electrically connected to case

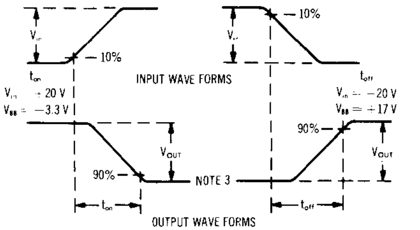
NPN silicon transistor designed for very-high-speed, low-power saturated switching applications for computers in military and industrial service.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	12	Vdc
Collector-Base Voltage	V_{CB}	25	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current	I_C	200	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 2.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.0 6.67	Watt mW/°C
Operating Junction Temperature Range	T_J	+175	°C
Storage Temperature Range	T_{stg}	-65 to +300	°C
Lead Temperature 1/16" ± 1/32" from case, 10 s	T_L	+235	°C

FIGURE 1 — TURN-ON AND TURN-OFF TIME TEST CIRCUIT





NOTE 1: With certain types of power supplies, it may be necessary to connect 25 μF decoupling capacitors across the power-supply terminals for V_{CC} and V_{BB}.

NOTE 2: Input voltage (V_{in}) obtained from a pulse generator having an output impedance of 50 ohms, V_{in} rise time ≤ 1.0 ns, pulse duration ≈ 300 ns, and duty factor ≤ 2.0%.

NOTE 3: Input and output waveforms, shown above, monitored by means of an oscilloscope having a rise time ≤ 0.5 ns, input capacitance of probe ≤ 2.5 pF with shunt resistance ≥ 3000 ohms.

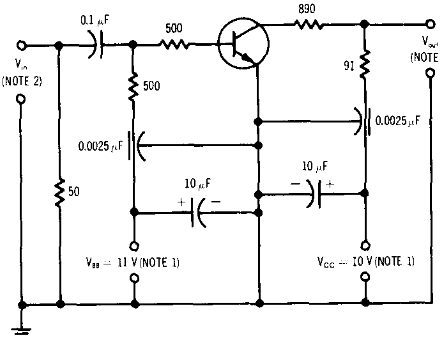
2N1708 (continued)

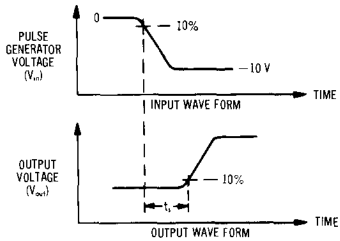
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage* (I_C = 10 mAdc, I_B = 0)	$BV_{CEO(sus)}$*	12	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	25	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	3.0	-	Vdc
Collector-Cutoff Current (V_{CE} = 10 Vdc, V_{BE} = 0.25 Vdc, T_A = 100°C)	I_{CEX}	-	15	μAdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	-	0.025	μAdc
(V_{CB} = 15 Vdc, I_E = 0, T_A = 150°C)		-	15	
ON CHARACTERISTICS				
DC Current Gain* (I_C = 10 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	20	-	-
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	-	0.22	Vdc
(I_C = 50 mAdc, I_B = 5.0 mAdc)		-	0.35	
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$	0.7	0.9	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	200	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 140 kHz)	C_{ob}	-	6.0	pF
Turn-On Time (Figure 1) (I_C = 10 mAdc, I_{B1} = 3.0 mAdc, I_{B2} = 1.0 mAdc)	t_{on}	-	40	ns
Turn-Off Time (Figure 1) (V_{CC} = 3.0 Vdc, I_C = 10 mAdc, I_{B1} = 3.0 mAdc, I_{B2} = 1.0 mAdc)	t_{off}	-	75	ns
Storage Time (Figure 2) (I_C = 10 mAdc, I_{B1} = I_{B2} = 10 mAdc)	t_s	-	25	ns

* Pulse Test: Pulse Length ≤ 6.0 ms, Duty Cycle ≤ 30%.

FIGURE 2 — STORAGE TIME TEST CIRCUIT



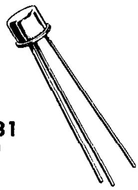


NOTE 1: Input voltage (V_{in}) obtained from pulse generator having an output impedance of 50 ohms. V_{in} rise time < 1 ns, pulse duration ≈ 300 ns, and duty factor ≤ 2.0%.

NOTE 2: Input and output wave forms monitored by means of an oscilloscope having a rise time ≤ 0.5 ns; input capacitance of probe < 2.5 pF with shunt resistance ≥ 1000 ohms.

2N1959 (SILICON)

V_{CER} = 40 V
I_C = 500 mA
P_D = 600 mW



CASE 31
(TO-5)

Collector connected to case

NPN silicon annular transistor designed for high-speed, medium-power saturated switching applications.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage R_{BE} = 10 ohms	V_{CER}	40	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current	I_C	500	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	600 4.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	2.0 1.3	Watts mW/°C
Operating Junction Temperature Range	T_J	-65to + 175	°C
Storage Temperature Range	T_{stg}	-65 to + 300	°C

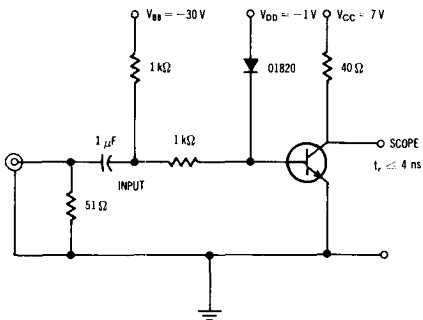
2N1959 (continued)

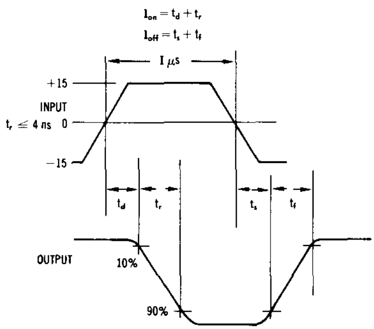
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 50 μAdc, R_{BE} = 10 ohms)		BV_{CER}	40	—	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)		BV_{CBO}	60	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0	—	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_A = 150°C)		I_{CBO}	— —	0.5 300	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 150 mAdc, V_{CE} = 10 Vdc)		h_{FE}	40	120	—
Collector-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)		$V_{CE(sat)}$	—	0.45	Vdc
Base-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)		$V_{BE(sat)}$	—	1.3	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 25 mAdc, V_{CB} = 10 Vdc, f = 100 MHz)		f_T	100	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}	—	18	pF
Turn-On Time	Figure 1 (V_{CC} = 7 Vdc, I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc,	t_{on}	—	65	ns
Turn-Off Time		t_{off}	—	45	ns
Storage Time		t_s	—	25	ns

*t_{on}, t_{off}, and t_s measured from 50% point of input pulse.

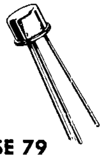
FIGURE 1 — SWITCHING TIME TEST CIRCUIT





2N1990 (SILICON)

$V_{CB} = 100$ V
$I_C = 1.0$ A
$P_D = 0.6$ W



CASE 79
(TO-39)

. . . NPN silicon transistor designed for driving neon display tubes.

Collector connected to case

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current-Continuous	I_C	1.0	Adc
Total Device Dissipation $T_A = 25°C$ Derate above 25°C	P_D	0.6 4.8	W mW/°C
Total Device Dissipation $T_C = 2.5°C$ @ $T_C = 100°C$	P_D	2.0 1.0	W
Operating & Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

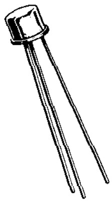
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	62.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	208	°C/W

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector Cutoff Current ($V_{CE} = 75$ Vdc, $I_B = 10$ μAdc) ($V_{CE} = 75$ Vdc, $I_B = 250$ μAdc, $T_A = 150°C$	I_{CEX}	 - -	 10 250	μAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 30$ mAdc, $V_{CE} = 10$ Vdc)	h_{FE}	 20	 -	-
Collector-Emitter Saturation Voltage ($I_C = 2.0$ mAdc, $I_B = 0.2$ mAdc)	$V_{CE(sat)}$	 -	 0.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 2.0$ mAdc, $I_B = 0.2$ mAdc)	$V_{BE(sat)}$	 -	 1.0	Vdc

2N2224 (SILICON)

V_{CEO} = 40 V
I_C = 0.5 A
P_D = 800 mW



. . . NPN silicon annular transistor designed primarily for high speed switching applications.

CASE 31
(TO-5)

Collector connected to case

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	65	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current-Continuous	I_C	0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.8 5.33	W mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	3.0 20	Watts mW/°C
Operating Junction Temperature Range	T_J	+175	°C
Storage Temperature Range	T_{stg}	-65 to +300	°C

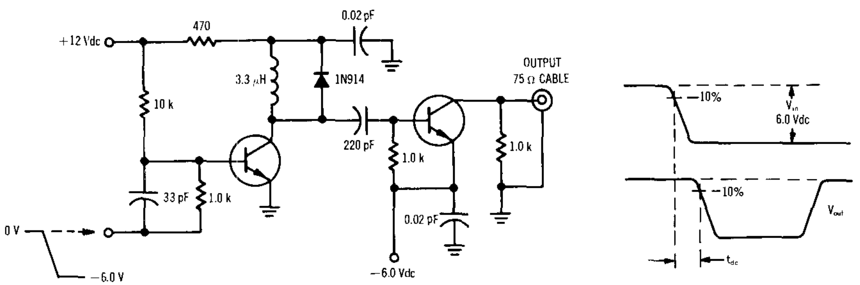
2N2224 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	40	-	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BV_{CBO}	65	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0	-	Vdc
Collector-Cutoff Current (V_{CB} = 50 Vdc, I_E = 0) (V_{CB} = 50 Vdc, I_E = 0, T_A = +150°C)	I_{CBO}	- -	0.01 10	μAdc
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	-	1.0	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 0.1 mAdc, V_{CE} = 10 Vdc) (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 100 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	 20 25 35 40	 - - 115 120	-
Collector-Emitter Saturation Voltage* (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{CE(sat)}$*	-	0.4	Vdc
Base-Emitter Saturation Voltage* (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{BE(sat)}$*	-	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz) (I_C = 80 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	 250 160	 - -	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0)	C_{ob}	-	8.0	pF
Circuit Delay (Figure 1) (T_A = 25°C)	t_{dc}	-	15	ns
Circuit Delay - Total Change (Figure 1) (T_A = +10°C to T_A = +25°C)	Δt_{dc}	-	15	ns

*Pulse Test: PW ≤ 300 μs, Duty Cycle ≤ 2.0%

FIGURE 1



2N2242 (SILICON)

V_{CB} = 40 V (max)
I_C = 225 mA
C_{ob} = 6.0 pF (max)
f_T = 250 MHz (min)

CASE 22
(TO-18)

. . . designed for high-speed, low power saturated switching applications.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	225	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	360 2.0	mWatts mW/°C
Junction Temperature — Operating	T_J	-65 to +205	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

FIGURE 1 — SWITCHING TIME TEST CIRCUIT

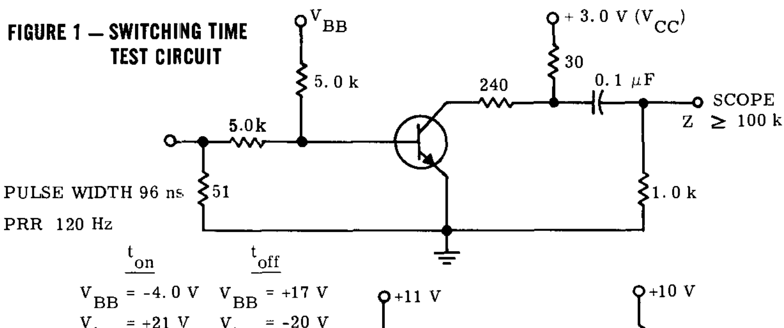
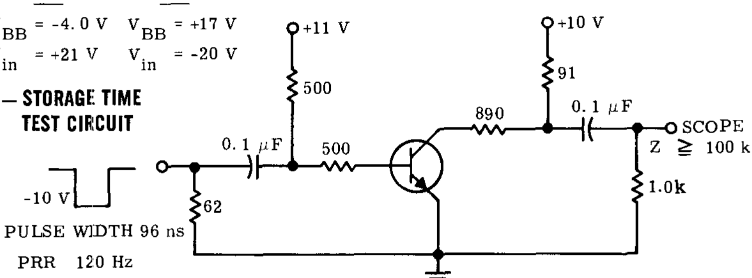


FIGURE 2 — STORAGE TIME TEST CIRCUIT



2N2242 (continued)

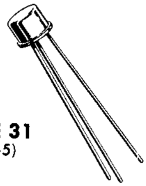
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collertor-Emitter Breakdown Voltage* (I_C = 30 mAdc, I_E = 0)	BV_{CEO}*	15	-	Vdc
Collector-Emitter Breakdown Voltage* (I_C = 30 mAdc, R_{BE} = ≤ 10 ohms)	BV_{CER}*	20	-	Vdc
Collector-Base Breakdown Voltage (I_C = 1.0 μAdc, I_E = 0)	BV_{CBO}	40	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0	-	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, $V_{EB(off)}$ = 0.25 Vdc, T_A = 125°C)	I_{CEX}	-	10	μAdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0) (V_{CB} = 20 Vdc, I_E = 0, T_A = 150°C)	I_{CBO}	- -	0.1 15	μAdc
Emitter Cutoff Current ($V_{EB(off)}$ = 4.0 Vdc, I_C = 0)	I_{EBO}	-	0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain* (I_C = 10 mAdc, V_{CE} = 1.0 Vdc) (I_C = 10 mAdc, V_{CE} = 1.0 Vdc, T_A = -55°C)	h_{FE}*	40 20	120 -	-
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc) (I_C = 10 mAdc, I_B = 1.0 mAdc, T_A = -55 to +125°C)	$V_{CE(sat)}$	- -	0.7 0.3	Vdc
Base-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc) (I_C = 10 mAdc, I_B = 1.0 mAdc, T_A = 125°C)	$V_{BE(sat)}$	- -	1.5 0.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain--Bandwidth Product (I_C = 20 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	250	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	-	6.0	pF
Turn-On Time (Figure 1) (V_{CC} = 3.0 Vdc, $V_{BE(off)}$ = +2.0 Vdc, I_{B1} = 3.0 mAdc, I_C = 10 mAdc)	t_{on}	-	30	ns
Turn-Off Time (Figure 1) (V_{CC} = 3.0 Vdc, I_C = 10 mAdc, I_{B1} = 3.0 mAdc, I_{B2} = 1.0 mAdc)	t_{off}	-	50	ns
Storage Time (Figure 2) (I_C = 10 mAdc, I_{B1} = I_{B2} = 10 mAdc)	t_s	-	25	ns

* Pulse Test: Pulse Wdith = 300 μS; Duty Cycle = ≤ 2%

2N2410 (SILICON)

$V_{CEO} = 30$ V
$I_C = 800$ mA
$P_D = 800$ mW



CASE 31
(TO-5)

Collector connected to case

NPN silicon annular transistor designed for high-speed, medium-power saturated switching applications.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Emitter Voltage R_{BE} = 10 ohms	V_{CER}	40	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current	I_C	800	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	800 4.57	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	2.5 14.3	Watts mW/°C
Operating Junction Temperature Range	T_J	200	°C
Storage Temperature Range	T_{stg}	-65 to + 300	°C

2N2410 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage* (I_C = 30 mAdc, I_B = 0)	$BV_{CEO\ (sus)}$*	30	—	Vdc
Collector-Emitter Breakdown Voltage* (I_C = 30 mAdc, R_{BE} = 10 ohms)	BV_{CER}*	40	—	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	BV_{CBO}	60	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	BV_{EBO}	5.0	—	Vdc
Collector-Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0) (V_{CE} = 30 Vdc, V_{BE} = 0, T_A = 150°C)	I_{CES}	— —	0.3 350	µAdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	0.3	µAdc
Emitter Cutoff Current (V_{BE} = 4 Vdc, I_C = 0)	I_{EBO}	—	0.3	µVdc
ON CHARACTERISTICS				
DC Current Gain* (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 150 mAdc, V_{CE} = 1 Vdc) (I_C = 150 mAdc, V_{CE} = 10 Vdc) (I_C = 500 mAdc, V_{CE} = 10 Vdc)	h_{FE}*	30 15 30 25	120 — 120 100	—
Collector-Emitter Saturation Voltage* (I_C = 150 mAdc, I_B = 15 mAdc) (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{CE(sat)}$*	— —	0.45 1.3	Vdc
Base-Emitter Saturation Voltage* (I_C = 150 mAdc, I_B = 15 mAdc) (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{BE\ (sat)}$*	— —	1.2 1.6	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	200	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	11	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 1 MHz)	C_{ib}	—	50	pF
Turn-On Time (t_d + t_r) (I_C = 150 mAdc, Figure 1) (I_C = 500 mAdc, Figure 2)	t_{on}	— —	65 65	ns
Turn-Off Time (t_s + t_f) (I_C = 150 mAdc, Figure 1) (I_C = 500 mAdc, Figure 2)	t_{off}	— —	55 65	ns
Storage Time (I_C = 150 mAdc, Figure 1)	t_s	—	40	ns
Fall Time (I_C = 150 mAdc, Figure 1)	t_f	—	30	ns

*Pulse Test: Pulse Width = 300 µs; Duty Cycle = 2%

SWITCHING TIME EQUIVALENT TEST CIRCUITS

FIGURE 1 — I_C = 150 mA

$t_r \leq$ 1 ns, PULSE WIDTH ~ 300 ns

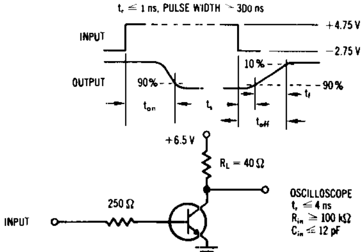
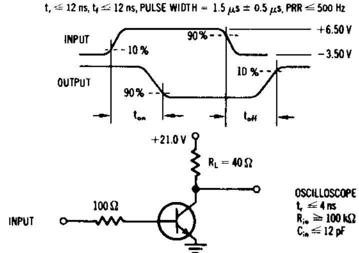


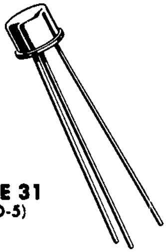
FIGURE 2 — I_C = 500mA

$t_r \leq$ 12 ns, $t_f \leq$ 12 ns, PULSE WIDTH = 1.5 µs ± 0.5 µs, PRR ≤ 500 Hz



2N2476 (SILICON)
2N2477

V_{CEO} = 20 V
f_T = 250 MHz
P_D = 600 mW



CASE 31
(TO-5)

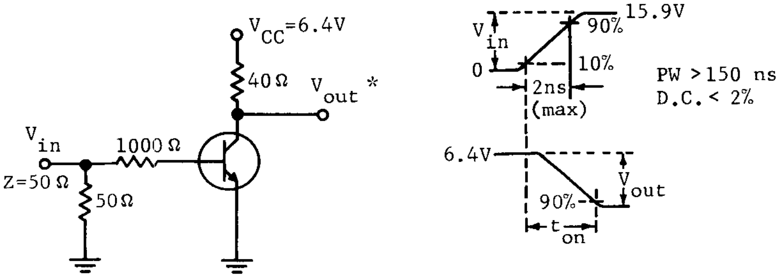
NPN silicon annular transistors designed for high-speed, low-power saturated switching applications.

Collector connected to case

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.6 3.4	Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	2.0 11.4	Watts mW/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

FIGURE 1 — TURN-ON TIME TEST CIRCUIT



*Input and output waveforms monitored by means of an oscilloscope or other indicating device having a rise time<0.5 ns; input capacitance of probe < 2.5 pF with shunt resistance ≥1 megohm.

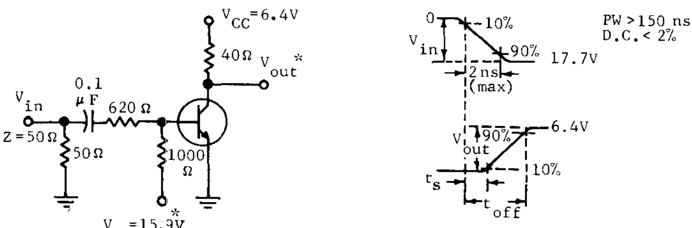
2N2476, 2N2477 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 50 mAdc, I_B = 0)		BV_{CEO}*	20	-	Vdc
Collector-Base Breakdown Voltage (I_C = 10 µAdc, I_E = 0)		BV_{CBO}	60	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 µAdc, I_C = 0)		BV_{EBO}	5.0	-	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)		I_{CBO}	-	0.2	µAdc
(V_{CB} = 30 Vdc, I_E = 0, T_A = 150°C)			-	200	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	-	100	µAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 150 mAdc, V_{CE} = 0.4 Vdc)	2N2476	h_{FE}	20	-	-
	2N2477		40	-	
Collector-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 7.5 mAdc)	2N2476	$V_{CE(sat)}$	-	0.4	Vdc
(I_C = 150 mAdc, I_B = 3.75 mAdc)	2N2477		-	0.4	
(I_C = 500 mAdc, I_B = 50 mAdc)	2N2476		-	0.75	
	2N2477		-	0.65	
Base-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 7.5 mAdc)	2N2476	$V_{BE(sat)}$	-	1.0	Vdc
(I_C = 150 mAdc, I_B = 3.75 mAdc)	2N2477		-	0.95	
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)		f_T	250	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 140 kHz)		C_{ob}	-	10	pF
Turn-On Time (Figure 1) (V_{CC} = 6.4 Vdc, I_C = 150 mAdc, I_{B1} = 15 mAdc)		t_{on}	-	25	ns
Turn-Off Time (Figure 2) (V_{CC} = 6.4 Vdc, I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc)		t_{off}	-	45	ns
Storage Time (Figure 2) (I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc)		t_s	-	25	ns

* Pulse Test: pulse width ≤ 400 µs, duty cycle ≤ 3%.

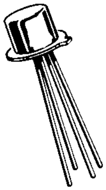
FIGURE 2 — TURN-OFF TIME TEST CIRCUIT



*Input and output waveforms monitored by means of an oscilloscope or other indicating device having a rise time<0.5 ns; input capacitance of probe<2.5 pF with shunt resistance ≥1 megohm.

JAN 2N2708 (SILICON)

V_{CEO} = 20 V
I_C = 50 mA
NF = 7.5 dB



CASE 20
(TO-72)

NPN silicon annular transistor designed for low power IF and RF use in VHF/UHF amplifier, mixer and oscillator applications, and qualified to meet the requirements of MIL-S-19500/302 EL.

Active Elements Isolated From Case

MAXIMUM RATINGS (T_A = 25° ± 3°C — unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Base Voltage	V_{CB}	35	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current	I_C	50	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.2 1.14	Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	0.3 1.72	Watt mW/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C
Lead Temperature (Not less than 1/16" from Seating Surface, No Time Limit)	T_L	+230	°C

JAN 2N2708 (continued)

TABLE I – GROUP A INSPECTION (T_A = 25°C ± 3°C – unless otherwise noted)

The fourth lead (case) shall be floating except for the following tests: G_{pe}, $r_b'C_c$, and NF.

Examination or Test	MIL-STD-750 Method	Symbol	Limits Min	Limits Max	Unit	LTPD
SUBGROUP 1						
Visual and Mechanical Examination	2071	-	-	-	-	10
SUBGROUP 2						5
Collector-Base Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	3036 Condition D	I_{CBO}	-	10	nAdc	
Collector-Base Breakdown Voltage (I_C = 1.0 μAdc, I_E = 0)	3001 Condition D	BV_{CBO}	35	-	Vdc	
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	3026 Condition D	BV_{EBO}	3.0	-	Vdc	
Collector-Emitter Breakdown Voltage (I_C = 3.0 mAdc, I_B = 0, Pulsed, Note 1)	3011 Condition D	BV_{CEO}	20	-	Vdc	
Forward-Current Transfer Ratio (V_{CE} = 2.0 Vdc, I_C = 2.0 mAdc)	3076	h_{FE}	30	200	-	
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	3066	$V_{BE(sat)}$	-	1.0	Vdc	
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	3071	$V_{CE(sat)}$	-	0.4	Vdc	
SUBGROUP 3						10
Forward-Current Transfer Ratio (V_{CE} = 15 Vdc, I_C = 2.0 mAdc, f = 1.0 kHz)	3206	h_{fe}	30	160	-	
Output Capacitance (V_{CB} = 15 Vdc, I_E = 0, f ≥ 0.1 MHz and ≤ 1.0 MHz)	3236	C_{ob}	-	1.5	pF	
SUBGROUP 4						10
Forward Current Transfer Ratio (V_{CE} = 15 Vdc, I_C = 2.0 mAdc, f = 100 MHz)	3306	h_{fe}	7.0	12	-	
Amplifier Power Gain (Neutralized) (V_{CE} = 15 Vdc, I_C = 2.0 mAdc, f = 200 MHz)	(See Figure 1)	G_{pe}	15	22	dB	
Collector-Base Time Constant (V_{CB} = 15 Vdc, I_C = 2.0 mAdc, f = 31.9 MHz)		$r_b'C_c$	9.0	33	ps	
Noise Figure (V_{CE} = 15 Vdc, I_C = 2.0 mAdc, R_G = 50 ohms, f = 200 MHz)		NF	-	7.5	dB	
SUBGROUP 5						10
High Temperature Operation: T_A = +150°C min						
Collector-Base Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	3036 (Notes 2 & 3)	I_{CBO}	-	1.0	μAdc	
Low-Temperature Operation: T_A = -55° +0 -3°C						
Forward Current Transfer Ratio (V_{CE} = 2.0 Vdc, I_C = 2.0 mAdc)	3076 (Notes 2 & 3)	h_{FE}	10	-	-	

Note 1. Pulse Test: Pulse Width ≤ 300 μs: Duty Cycle ≤ 2.0%

Note 2. Units shall be allowed to return to and be stabilized at 25°C prior to Low-Temperature Operational Test.

Note 3. Test measurement shall be made after thermal equilibrium has been reached at the temperature specified.

JAN 2N2708 (continued)

TABLE II – GROUP B INSPECTION (T_A = 25°C ± 3°C – unless otherwise noted)

Examination or Test	MIL-STD-750 Method	Symbol	Limits Min	Limits Max	Unit	LTPD
SUBGROUP 1						
Physical Dimensions	2066	-	-	-	-	20
SUBGROUP 2						10
Soldering Heat, 1 cycle	2031	-	-	-	-	
Temperature Cycling	1051 Condition C	-	-	-	-	
Thermal Shock (glass strain)	1056 Condition A	-	-	-	-	
Moisture Resistance, (No initial conditioning)	1021	-	-	-	-	
End Point Tests: (Note 4)						
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	3036 Condition D	I_{CBO}	-	20	nAdc	
Forward-Current Transfer Ratio (V_{CE} = 2.0 Vdc, I_C = 2.0 mAdc)	3076	h_{FE}	30	-	-	
SUBGROUP 3						10
Shock (1500 G, 5 blows of approx. 0.5 ms each in orientations X1, Y1, Y2, Z1, total = 20 blows)	2016 non-operating	-	-	-	-	
Vibration, variable frequency	2056	-	-	-	-	
Vibration Fatigue, 20 G	2046 non-operating	-	-	-	-	
Constant Acceleration (centrifuge) Orientations X1, Y1, Y2, Z1 20,000 G	2006	-	-	-	-	
End Point Tests: (Note 4)						
Same as for Subgroup 2						
SUBGROUP 4						15
Lead Fatigue	2036 Condition E					
End Point Tests: (Note 4)						
Seal		-	-	$5x10^{-7}$	atm cc/s	
Per Method 112, MIL-STD-202.	Condition C Procedure IIIa Test Cond. A for Gross Leaks					
SUBGROUP 5						20
Salt atmosphere	1041	-	-	-	-	
There shall be no evidence of flaking, pitting, or other visible signs of corrosion on sample units after test subjection.						
End Point Tests: (Note 4)						
Same as for Subgroup 2						
SUBGROUP 6						λ = 15
High-Temperature Life T_{stg} = +200°C min	1031 non-operating	-	-	-	-	
End Point Tests: (Note 4)						
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	3036 Condition D	I_{CBO}	-	50	nAdc	
Forward Current Transfer Ratio (V_{CE} = 2.0 Vdc, I_C = 2.0 mAdc)	3076	h_{FE}	22.5	-	-	
SUBGROUP 7						λ = 15
Steady-State Operation Life (I_C = 20 mAdc, P_T = 200 mW)	1026	-	-	-	-	
End Point Tests: (Note 4)						
Same as for Subgroup 6						

Note 4. End-point test measurements shall be made within 4 hours.

JAN 2N2708 (continued)

TABLE III – GROUP C INSPECTION (T_A = 25°C ± 3° – unless otherwise noted)

Examination or Test	MIL-STD-750 Method	Symbol	Limits Min	Limits Max	Unit	LTPD
SUBGROUP 1						
Barometric pressure, reduced (altitude operation) Normal mounting t = 60 s	1001 Condition D	-	-	-	-	15
Collector-Base Cutoff Current (V_{CB} = 35 Vdc, I_E = 0)	3036 Condition D (Note 5)	I_{CBO}	-	1.0	μAdc	

Note 5. This test to be performed and measurement made during subjection of the sample units to the reduced barometric pressure specified.

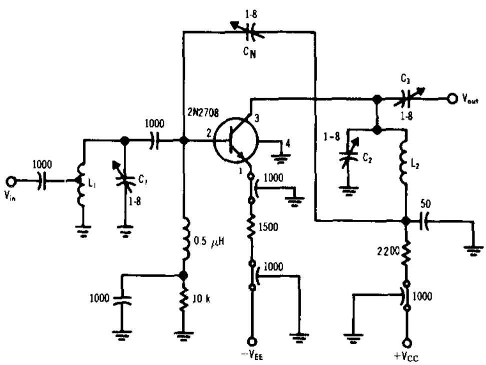


FIGURE 1 – TEST CIRCUIT FOR POWER GAIN AND NOISE FIGURE

Capacitance values in pF

L1 – 2½ turns #18 AWG wire, ⅜" ID by ½" lg.
L2 – 3 turns #22 AWG wire, ⅜" ID by ¾" lg.

Neutralization Procedure:

(A) Connect 200-MHz signal generator (with Z_{out} = 50 ohms) to input terminals of amplifier.

(B) Connect 50-ohm RF voltmeter across output terminals of amplifier.

(C) Apply V_{EE} and V_{CC}, and with signal generator adjusted for 1.0 mV output from amplifier, tune C_1, C_2, and C_3 for maximum output.

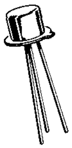
(D) Interchange connections to signal generator and output indicator.

(E) With sufficient signal applied to output terminals of amplifier, adjust C_N for minimum indication at input.

(F) Repeat steps (A), (B), and (C) to determine if retuning is necessary.

2N2710 (SILICON)

V_{CEO} = 20 V
I_C = 500 mA
T_S = 15 ns max



CASE 22
(TO-18)

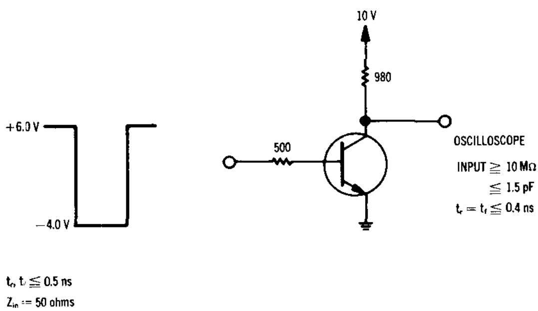
. . . NPN silicon transistor primarily designed for high-speed, low-power saturated switching applications for industrial service.

Collector connected to case

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Emitter Voltage	V_{CES}	30	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current-Continuous	I_C	500	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.36 2.1	W mW/°C
Total Device Dissipation @ T_C = 25°C	P_D	1.2	W
Operating Junction Temperature Range	T_J	+200	°C
Storage Temperature Range	T_{stg}	-65 to +300	°C

FIGURE 1 — STORAGE TIME TEST CIRCUIT

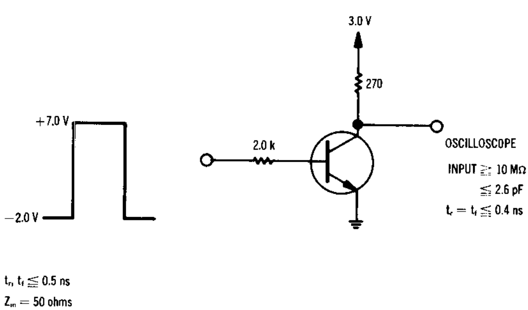


2N2710 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

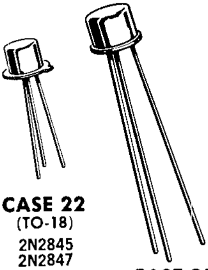
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	20	-	Vdc
Collector-Emitter Breakdown Voltage (I_C = 10 μAdc, V_{BE} = 0)	BV_{CES}	30	-	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BV_{CBO}	40	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0	-	Vdc
Collector-Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	-	30	nAdc
(V_{CB} = 20 VDC, I_E = 0, T_A = +150°C)		-	30	μAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}	-	1.0	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 10 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	40	-	-
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)		40	-	
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	-	0.25	Vdc
(I_C = 50 mAdc, I_B = 5.0 mAdc)		-	0.4	
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$	-	0.9	Vdc
(I_C = 50 mAdc, I_B = 5.0 mAdc)		-	1.3	
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	500	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 4.0 MHz)	C_{ob}	-	4.0	pF
Turn-On Time (Figure 2) (V_{CC} = 3.0 Vdc, $V_{BE(off)}$ = -2.0 Vdc, I_C = 10 mAdc, I_{B1} = 3.0 mAdc)	t_{on}	-	20	ns
Turn-Off Time (Figure 2) (V_{CC} = 3.0 Vdc, I_C = 10 mAdc, I_{B1} = 3.0 mAdc, I_{B2} = 1.0 mAdc)	t_{off}	-	35	ns
Charge-Storage Time (Figure 1) (V_{CC} = 10 Vdc, I_C = I_{B1} = I_{B2} = 10 mAdc)	t_s	-	15	ns

FIGURE 2 — TURN ON AND TURN OFF TIME TEST CIRCUIT



2N2845 thru 2N2848 (SILICON)

V_{CEO} = 20-30 V
P_D = 360-800 mW



CASE 22
(TO-18)
2N2845
2N2847

CASE 31
(TO-5)
2N2846
2N2848

NPN silicon annular transistors designed for high-speed, medium-power saturated switching applications.

MAXIMUM RATINGS

Rating	Symbol	2N2845	2N2846	2N2847	2N2848	Unit
Collector-Emitter Voltage*	V_{CEO}*	30	30	20	20	Vdc
Collector-Base Voltage	V_{CB}	60	60	60	60	Vdc
Emitter-Base Voltage	V_{EB}	5	5	5	5	Vdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	360 2.1	800 4.6	360 2.1	800 4.6	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.2 6.9	3.0 17.2	1.2 6.9	3.0 17.2	Watts mW/°C
Operating Junction Temperature Range	T_J	-65 to 200				°C
Storage Temperature Range	T_{stg}	-65 to +300				°C
Lead Temperature (Soldering, no time limit)	—	300				°C

*Applicable from 1 mA to 30 mA (Pulsed)

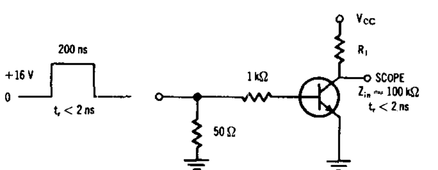
2N2845 thru 2N2848 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage*		$BV_{CEO(sus)}$*			Vdc
(I_C = 30 mAdc, I_B = 0)	2N2845, 2N2846		30	—	
(I_C = 30 mAdc, I_B = 0)	2N2647, 2N2848		20	—	
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)		BV_{CBO}	80	—	Vdc
Emttter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)		BV_{EBO}	5.0	—	Vdc
Collector-Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0)		I_{CES}	—	0.2	μAdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0, T_A = 150°C)		I_{CBO}	—	200	μAdc
Base Leakage Current (V_{CE} = 30 Vdc, V_{BE} = 0)		I_{BL}	—	0.2	μAdc
ON CHARACTERISTICS					
DC Current Gain*		h_{FE}*			—
(I_C = 150 mAdc, V_{CE} = 10 Vdc)	2N2845, 2N2846		30	120	
	2N2847, 2N2848		40	140	
(I_C = 500 mAdc, V_{CE} = 10 Vdc)	2N2845, 2N2846		20	—	
	2N2847, 2N2848		30	—	
(I_C = 500 mAdc, V_{CE} = 1 Vdc)	All Types		10	—	
Collector-Emitter Saturation Voltage*		$V_{CE(sat)}$*			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)	All Types		—	0.4	
(I_C = 500 mAdc, I_B = 50 mAdc)	2N2845, 2N2846		—	1.0	
	2N2847, 2N2848		—	0.75	
Base-Emitter Saturation Voltage*		$V_{BE(sat)}$*			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)			—	1.2	
(I_C = 500 mAdc, I_B = 50 mAdc)			—	1.8	
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)		f_T	250	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 140 kHz)		C_{ob}	—	8.0	pF
Turn-On Time (Figure 1)		t_{on}			ns
(V_{CC} = 10 Vdc, I_C ≈ 150 mAdc, I_{B1} ≈ 15 mAdc)	2N2845, 2N2846		—	40	
(V_{CC} = 8 Vdc, I_C ≈ 150 mAdc, I_{B1} ≈ 15 mAdc)	2N2847, 2N2848		—	25	
Turn-Off Time (Figure 2)		t_{off}			ns
(V_{CC} = 10 Vdc, I_C ≈ 150 mAdc, I_{B1} ≈ I_{B2} ≈ 15 mAdc)	2N2845, 2N2846		—	40	
(V_{CC} = 8 Vdc, I_C ≈ 150 mAdc, I_{B1} ≈ I_{B2} ≈ 15 mAdc)	2N2847, 2N2848		—	40	

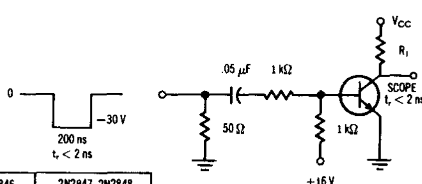
*Pulse Test: Pulse Width = 300 μs; Duty Cycle = ≤ 2%

FIGURE 1 — TURN-ON TIME TEST CIRCUIT



	2N2845, 2N2846	2N2847, 2N2848
V_{CC}	10 V	6 V
R_1	62 Ω	39 Ω

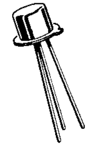
FIGURE 2 — TURN-OFF TIME TEST CIRCUIT



2N3009 (SILICON)
2N3013
2N3014

BV_{CBO} = 40 V (min)
f_T = 350 MHz (min)

NPN silicon epitaxial switching transistor designed for high-speed, medium-power saturated switching applications



Collector connected to case

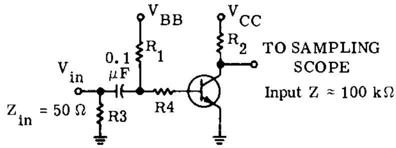
CASE 27
(TO-52)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage* 2N3009, 2N3013 / 2N3014	V_{CEO}*	15 / 20	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage 2N3009 / 2N3013, 2N3014	V_{EB}	4.0 / 5.0	Vdc
Collector Current — Continuous / (10 μs pulse) Peak	I_C	200 / 500	mAdc
Total Device Dissipation @T_A = 25°C / Derate above 25°C	P_D	0.36 / 2.06	Watt / mW/°C
Total Device Dissipation @T_C = 25°C / @T_C = 100°C / Derate above 25°C	P_D	1.20 / 0.68 / 6.85	Watts / Watt / mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C
Lead Temperature (Soldering, 60 second time limit)	—	300	°C

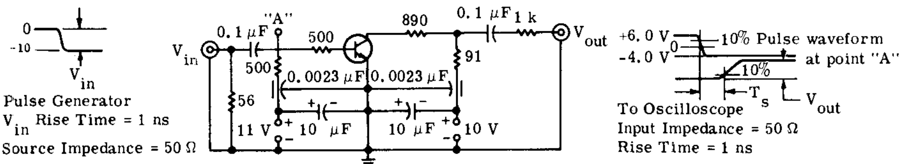
* Applicable from 0.01 mA to 10 mA (Pulsed)

FIGURE 1 — TURN-ON AND TURN-OFF TIME TEST CIRCUIT



	SWITCHING TEST CIRCUIT VALUES								INPUT PULSE		
Type	Test	V_{in}	V_{BB}	V_{CC}	R_1	R_2	R_3	R_4	t_r	t_f	Pulse Width
		(volts)			(ohms)				(nanoseconds)		
2N3009 2N3013	t_{on} & t_{off}	11	-5.0	15	300	50	75	170	<1.0	<1.0	>100
2N3014	t_{on}	7.0	GND	2.0	100	62	100	2.0 k	<1.0	-	>200
	t_{off}	-13	7.0	2.0							

FIGURE 2 — CHARGE STORAGE TIME CONSTANT TEST CIRCUIT



V_{in} Rise Time less than 1 ns   PW = 300 ns   Duty Cycle = 2%

2N3009, 2N3013, 2N3014 (continued)

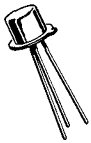
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage*		$BV_{CEO(sus)}$*			Vdc
(I_C = 10 mAdc, I_B = 0)	2N3009, 2N3013		15	-	
	2N3014		20	-	
Collector-Emitter Breakdown Voltage (I_C = 100 μAdc, V_{BE} = 0)		BV_{CES}	40	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)		BV_{CBO}	40	-	Vdc
Emitter-Base Breakdown Voltage		BV_{EBO}			Vdc
(I_E = 100 μAdc, I_C = 0)	2N3009		4.0	-	
	2N3013, 2N3014		5.0	-	
Collector-Cutoff Current		I_{CES}			μAdc
(V_{CE} = 20 Vdc, V_{BE} = 0)	2N3009		-	0.5	
(V_{CE} = 20 Vdc, V_{BE} = 0, T_A = +85°C)	2N3009		-	15	
(V_{CE} = 20 Vdc, V_{BE} = 0)	2N3013, 2N3014		-	0.3	
(V_{CE} = 20 Vdc, V_{BE} = 0, T_A = +125°C)	2N3013, 2N3014		-	40	
Base Current		I_B			μAdc
(V_{CE} = 20 Vdc, V_{BE} = 0)	2N3009		-	0.5	
	2N3013, 2N3014		-	0.3	
ON CHARACTERISTICS					
DC Current Gain*		h_{FE}*			-
(I_C = 30 mAdc, V_{CE} = 0.4 Vdc)	All Types		30	120	
(I_C = 10 mAdc, V_{CE} = 0.4 Vdc)	2N3014		25	-	
(I_C = 100 mAdc, V_{CE} = 0.5 Vdc)	2N3009, 2N3013		25	-	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)	2N3014		25	-	
(I_C = 300 mAdc, V_{CE} = 1.0 Vdc)	2N3009, 2N3013		15	-	
(I_C = 30 mAdc, V_{CE} = 0.4 Vdc, T_A = -55°C)	2N3013, 2N3014		12	-	
Collector-Emitter Saturation Voltage*		$V_{CE(sat)}$*			Vdc
(I_C = 30 mAdc, I_B = 3.0 mAdc)	All Types		-	0.18	
(I_C = 100 mAdc, I_B = 10 mAdc)	2N3009, 2N3013		-	0.28	
(I_C = 100 mAdc, I_B = 10 mAdc)	2N3014		-	0.35	
(I_C = 300 mAdc, I_B = 30 mAdc)	2N3009, 2N3013		-	0.50	
(I_C = 10 mAdc, I_B = 1.0 mAdc)	2N3014		-	0.18	
(I_C = 30 mAdc, I_B = 3.0 mAdc, T_A = +85°C)	2N3009		-	0.30	
(I_C = 30 mAdc, I_B = 3.0 mAdc, T_A = +125°C)	2N3013, 2N3014		-	0.25	
Base-Emitter Saturation Voltage*		$V_{BE(sat)}$*			Vdc
(I_C = 30 mAdc, I_B = 3.0 mAdc)	All Types		0.75	0.95	
(I_C = 100 mAdc, I_B = 10 mAdc)	All Types		-	1.20	
(I_C = 300 mAdc, I_B = 30 mAdc)	2N3009, 2N3013		-	1.70	
(I_C = 10 mAdc, I_B = 1.0 mAdc)	2N3014		0.70	0.80	
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 30 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)		f_T	350	-	MHz
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 140 kHz)		C_{ob}	-	5.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 140 kHz)		C_{ib}	-	8.0	pF
Turn-On Time (Figure 1)		t_{on}			ns
($V_{EB(off)}$ = 5.0 V, V_{CC} = 15 V, I_C = 300 mAdc, I_{B1} ≈ 30 mAdc)	2N3009, 2N3013		-	15	
($V_{EB(off)}$ = 0, V_{CC} = 2.0 V, I_C = 30 mAdc, I_{B1} ≈ 3.0 mAdc)	2N3014		-	16	
Turn-Off Time (Figure 1)		t_{off}			ns
(V_{CC} = 15 V, I_C = 300 mAdc, I_{B1} ≈ I_{B2} ≈ 30 mAdc)	2N3009, 2N3013		-	25	
(V_{CC} = 2.0 V, I_C = 30 mAdc, I_{B1} ≈ I_{B2} ≈ 3.0 mAdc)	2N3014		-	25	
Charge-Storage Time (Figure 2) (I_C ≈ I_{B1} ≈ I_{B2} ≈ 10 mAdc)		t_s	-	18	ns

* Pulse Test: Pulse Width = 300 μs; Duty Cycle ≤ 2%.

2N3010

f_T = 600 MHz min
$t_{on} + t_{off}$ = 24 ns max
BV_{CES} = 11 V



CASE 22
(TO-18)

NPN silicon low-power transistor primarily designed for high-speed, saturated switching applications.

Collector connected to case

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage*	V_{CEO}*	6.0	Vdc
Collector-Emitter Voltage	V_{CES}	11	Vdc
Collector-Base Voltage	V_{CB}	15	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous	I_C	50	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.30 1.71	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C
Lead Temperature (Soldering, 60 second time limit)	T_L	300	°C

* Applicable from 0.01 mAdc to 10 mAdc (Pulsed).

FIGURE 1 — TURN-ON AND TURN-OFF TIME TEST CIRCUIT

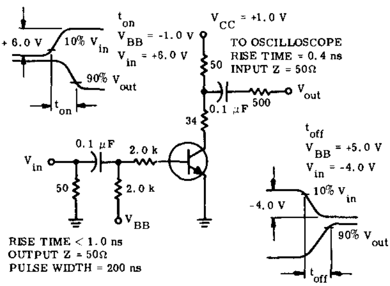
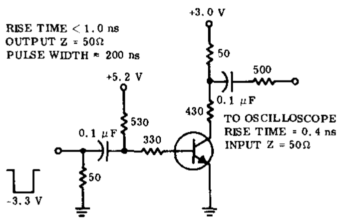


FIGURE 2 — CHARGE-STORAGE TIME TEST CIRCUIT



2N3010 (continued)

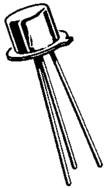
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage* (I_C = 10 mAdc, I_B = 0)	$BV_{CEO(sus)}$*	6.0	-	Vdc
Collector-Emitter Breakdown Voltage (I_C = 10 μAdc, V_{BE} = 0)	BV_{CES}	11	-	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BV_{CBO}	15	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	4.0	-	Vdc
Collector Cutoff Current	I_{CES}			μAdc
(V_{CE} = 11 Vdc, V_{BE} = 0)		-	10	
(V_{CE} = 5.0 Vdc, V_{BE} = 0)		-	0.1	
(V_{CE} = 5.0 Vdc, V_{BE} = 0, T_A = +85°C)		-	5.0	
Base Cutoff Current (V_{CE} = 11 Vdc, $V_{EB(off)}$ = 0)	I_{BL}	-	10	μAdc
ON CHARACTERISTICS				
DC Current Gain*	h_{FE}*			-
(I_C = 1.0 mAdc, V_{CE} = 0.4 Vdc)		15	-	
(I_C = 10 mAdc, V_{CE} = 0.4 Vdc)		25	125	
(I_C = 30 mAdc, V_{CE} = 0.4 Vdc)		15	-	
Collector-Emitter Saturation Voltage*	$V_{CE(sat)}$*			Vdc
(I_C = 1.0 mAdc, I_B = 0.1 mAdc)		-	0.25	
(I_C = 10 mAdc, I_B = 1.0 mAdc)		-	0.25	
(I_C = 30 mAdc, I_B = 3.0 mAdc)		-	0.38	
(I_C = 10 mAdc, I_B = 1.0 mAdc, T_A = 85°C)		-	0.4	
Base-Emitter Saturation Voltage*	$V_{BE(sat)}$*			Vdc
(I_C = 1.0 mAdc, I_B = 0.1 mAdc)		0.68	0.85	
(I_C = 10 mAdc, I_B = 1.0 mAdc)		0.75	0.95	
(I_C = 30 mAdc, I_B = 3.0 mAdc)		-	1.3	
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 10 mAdc, V_{CE} = 4.0 Vdc, f = 100 MHz)	f_T	600	-	MHz
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 140 kHz)	C_{ob}	-	3.0	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 140 kHz)	C_{ib}	-	2.0	pF
Turn-On Time (Figure 1) (V_{CC} = 1.0 Vdc, $V_{BE(off)}$ = 1.0 Vdc, I_C = 10 mAdc, I_{B1} ≈ 2.0 mAdc)	t_{on}	-	12	ns
Turn-Off Time (Figure 1) (V_{CC} = 1.0 Vdc, I_C ≈ 10 mAdc, I_{B1} ≈ I_{B2} ≈ 1.0 mAdc)	t_{off}	-	12	ns
Charge Storage Time (Figure 2) (I_C = I_{B1} ≈ I_{B2} = 5.0 mAdc)	t_s	-	6.0	ns

* Pulse Test: Pulse Length = 300 μs; Duty Cycle ≤ 2.0%.

2N3011 (SILICON)

f_T = 400 MHz min
$t_{on} + t_{off}$ = 35 ns max



NPN silicon low-power transistor primarily designed for high-speed, saturated switching applications.

Collector connected to case

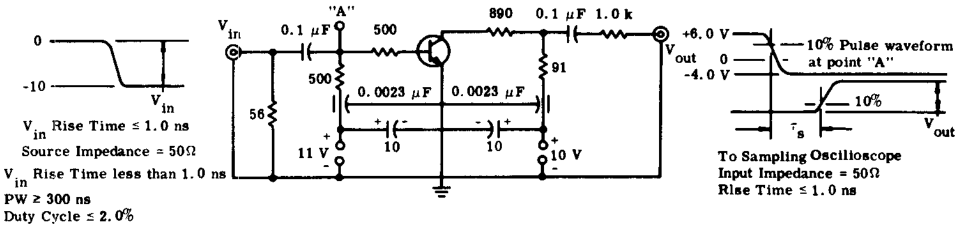
CASE 22
(TO-18)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage*	V_{CEO}*	12	Vdc
Collector-Emitter Voltage	V_{CES}	30	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector-Current-Continuous Peak (10 μs Pulse)	I_C	200 500	mAdc
Total Device Dissipation @ T_A=25°C Derate above 25°C	P_D	0.36 2.06	Watt mW/°C
Total Device Dissipation @ T_C=25°C T_C=100°C Derate above 25°C	P_D	1.20 0.68 6.85	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C
Lead Temperature (Soldering 60 second time limit)	T_L	300	°C

* Applicable from 0.01 mA to 10 mA (Pulsed)

FIGURE 1 — CHARGE-STORAGE TIME TEST CIRCUIT



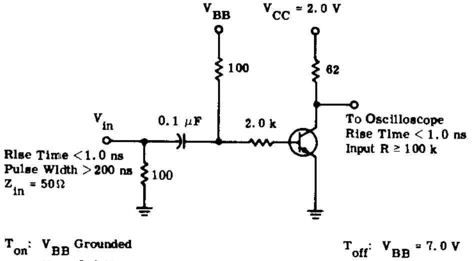
2N3011 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage* (I_C = 10 mAdc, I_B = 0)	$BV_{CEO(sus)}$*	12	-	Vdc
Collector-Emitter Breakdown Voltage (I_C = 10 μAdc, V_{BE} = 0)	BV_{CES}	30	-	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BV_{CBO}	30	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	5.0	-	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, V_{BE} = 0) (V_{CE} = 20 Vdc, V_{BE} = 0, T_A = +85°C)	I_{CES}	- -	0.4 10	μAdc
Base Cutoff Current (V_{CE} = 20 Vdc, V_{BE} = 0)	I_{BL}	-	0.4	μAdc
ON CHARACTERISTICS				
DC Current Gain* (I_C = 10 mAdc, V_{CE} = 0.35 Vdc) (I_C = 30 mAdc, V_{CE} = 0.4 Vdc) (I_C = 100 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}*	30 25 12	120 - -	-
Collector-Emitter Saturation Voltage* (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 30 mAdc, I_B = 3.0 mAdc) (I_C = 100 mAdc, I_B = 10 mAdc) (I_C = 10 mAdc, I_B = 1.0 mAdc, T_A = +85°C)	$V_{CE(sat)}$*	- - - -	0.20 0.25 0.50 0.30	Vdc
Base-Emitter Saturation Voltage* (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 30 mAdc, I_B = 3.0 mAdc) (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{BE(sat)}$*	0.72 - -	0.87 1.15 1.60	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 20 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	400	-	MHz
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 140 kHz)	C_{ob}	-	4.0	pF
Turn-On Time (Figure 2) (V_{CC} = 2.0 Vdc, $V_{EB(off)}$ = 0, I_C ≈ 30 mAdc, I_{B1} ≈ 3.0 mAdc)	t_{on}	-	15	ns
Turn-Off Time (Figure 2) (V_{CC} = 2.0 Vdc, I_C = 30 mAdc, I_{B1} ≈ $-I_{B2}$ ≈ 3.0 mAdc)	t_{off}	-	20	ns
Charge Storage Time (Figure 1) (I_C = I_{B1} ≈ $-I_{B2}$ ≈ 10 mAdc)	t_s	-	13	ns

* Pulse Test: Pulse Length = 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 — TURN-ON AND TURN-OFF TIME TEST CIRCUIT

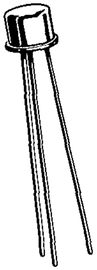


T_{on}: V_{BB} Grounded, V_{in} = 7.0 V

T_{off}: V_{BB} = 7.0 V, V_{in} = -13 V

2N3015 (SILICON)

V_{CEO} = 30 V
f_T = 250 MHz
P_D = 800 mW



NPN silicon annular transistor designed for high-speed, medium-power saturated switching applications.

CASE 31
(TO-5)

Collector connected to case

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage*	V_{CEO}*	30	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	800 4.6	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	3.0 17.2	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C
Lead Temperature (Soldering, 60 second time limit)	—	300	°C

*Applicable from 1.0 mA to 30 mA (Pulsed)

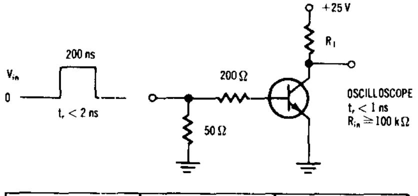
2N3015 (continued)

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage* (I_C = 30 mAdc, I_B = 0)	$BV_{CEO(sus)}$*	30	—	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	60	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	5	—	Vdc
Collector-Cutoff Current (V_{CE} = 30 Vdc, V_{BE} = 0)	I_{CES}	—	0.2	μAdc
Collector-Cutoff Current (V_{CB} = 30 Vdc, I_E = 0, T_A = 125°C)	I_{CBO}	—	200	μAdc
Base Leakage Current (V_{CE} = 30 Vdc, V_{BE} = 0)	I_{BL}	—	0.2	μAdc
ON CHARACTERISTICS				
DC Current Gain*	h_{FE}*			—
(I_C = 150 mAdc, V_{CE} = 10 Vdc)		30	120	
(I_C = 300 mAdc, V_{CE} = 0.7 Vdc)		10	—	
Collector-Emitter Saturation Voltage*	$V_{CE(sat)}$*			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)		—	0.4	
(I_C = 500 mAdc, I_B = 50 mAdc)		—	1.0	
Base-Emitter Saturation Voltage*	$V_{BE(sat)}$*			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)		—	1.2	
(I_C = 500 mAdc, I_B = 50 mAdc)		—	1.6	
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	250	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 140 kHz)	C_{ob}	—	8.0	pF
Turn-On Time (Figure 1)	t_{on}			ns
(V_{CC} = 25 Vdc, I_C ≈ 300 mAdc, I_{B1} ≈ 30 mAdc)		—	40	
(V_{CC} = 25 Vdc, I_C ≈ 500 mAdc, I_{B1} ≈ 50 mAdc)		—	40	
Turn-Off Time (Figure 2)	t_{off}			ns
(V_{CC} = 25 Vdc, I_C ≈ 300 mAdc, I_{B1} ≈ I_{B2} = 30 mAdc)		—	60	
(V_{CC} = 25 Vdc, I_C ≈ 500 mAdc, I_{B1} ≈ I_{B2} = 50 mAdc)		—	60	

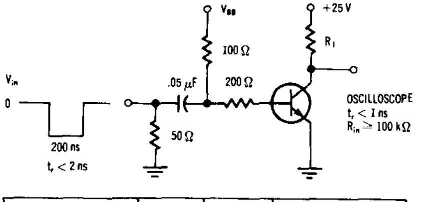
*Pulse Test: Pulse Width = 300 μs; Duty Cycle ≤ 2%

FIGURE 1 — TURN-ON TIME TEST CIRCUIT



I_C mA	V_{in} Volts	R_l ohms
300	7	80
500	11	48

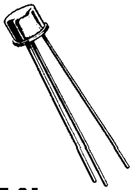
FIGURE 2 — TURN-OFF TIME TEST CIRCUIT



I_C mA	V_{in} Volts	V_{BB} Volts	R_l ohms
300	−13	10	80
500	−21	16	48

2N3053 (SILICON)

$V_{CEO} = 40\ V$
$I_C = 700\ mA$
$P_D = 5\ W$



CASE 31
(TO-5)

NPN silicon annular transistor designed for medium-current switching and amplifier applications.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current-Continuous	I_C	700	mAdc
Total Device Dissipation @ $T_C = 25^{\circ}C$ Derate above $25^{\circ}C$	P_D	5 28.6	Watts $mW/^{\circ}C$
Operating Junction Temperature Range	T_J	200	$^{\circ}C$
Storage Temperature Range	T_{stg}	-65 to +200	$^{\circ}C$

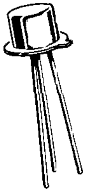
ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage ($I_C = 100\ \mu Adc$, $I_E = 0$)	BV_{CEO}	40	—	Vdc
Collector-Emitter Breakdown Voltage ($I_C = 100\ mAdc$, $R_{BE} = 10$ ohms)	BV_{CER}	50	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 100\ \mu Adc$, $I_E = 0$)	BV_{CBO}	60	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100\ \mu Adc$, $I_C = 0$)	BV_{EBO}	5	—	Vdc
Collector Cutoff Current ($V_{CE} = 60$ Vdc, $V_{EB(off)} = 1.5$ Vdc)	I_{CEX}	—	0.25	μAdc
Base Cutoff Current ($V_{CE} = 60$ Vdc, $V_{EB(off)} = 1.5$ Vdc)	I_{BL}	—	0.25	μAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 150$ mAdc, $V_{CE} = 2.5$ Vdc) ($I_C = 150$ mAdc, $V_{CE} = 10$ Vdc)*	h_{FE}	 25 50	 — 250	—
Collector-Emitter Saturation Voltage ($I_C = 150$ mAdc, $I_B = 15$ mAdc)	$V_{CE(sat)}$	—	1.4	Vdc
Base-Emitter Saturation Voltage ($I_C = 150$ mAdc, $I_B = 15$ mAdc)	$V_{BE(sat)}$	—	1.7	Vdc
Base-Emitter On Voltage ($I_C = 150$ mAdc, $V_{CE} = 2.5$ Vdc)	$V_{BE(on)}$	—	1.7	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product ($I_C = 50$ mAdc, $V_{CE} = 10$ Vdc, $f = 20$ MHz)	f_T	100	—	MHz
Output Capacitance ($V_{CB} = 10$ Vdc, $I_E = 0$, $f = 140$ kHz)	C_{ob}	—	15	pF
Input Capacitance ($V_{BE} = 0.5$ Vdc, $I_C = 0$, $f = 140$ kHz)	C_{ib}	—	80	pF

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%

2N3210 (SILICON)

V_{CEO} = 15 V
I_C = 500 mA
P_D = 360 mW



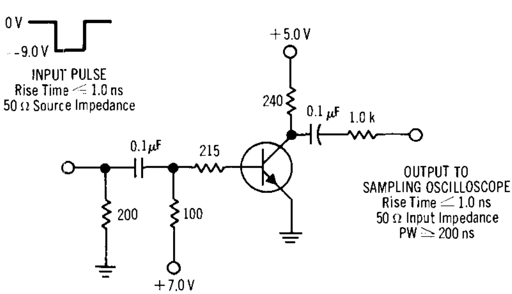
CASE 22
(TO-18)

NPN silicon high frequency switching transistor is designed for high speed, saturated switching applications for industrial service.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage Applicable from 0 to 500 mAdc	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	500	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.36 2.06	Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.2 6.9	Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +300	°C

FIGURE 1 — STORAGE TIME TEST CIRCUIT



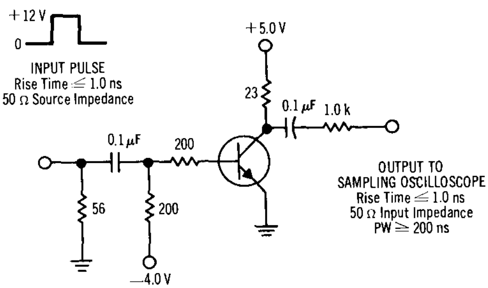
2N3210 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage* (I_C = 30 mAdc, I_B = 0)	$BV_{CEO(sus)}$*	15	-	Vdc
Collector-Base Breakdown Voltage (I_C = 2.0 μAdc, I_E = 0)	BV_{CBO}	40	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0	-	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	I_{CEX}	-	25	nAdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0) (V_{CB} = 20 Vdc, I_E = 0, T_A = 150°C)	I_{CBO}	- -	0.010 15	μAdc
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, I_C = 0)	I_{EBO}	-	100	nAdc
Base Cutoff Current (V_{CE} = 20 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	I_{BL}	-	0.025	μAdc
ON CHARACTERISTICS				
DC Current Gain* (I_C = 10 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}*	30	120	-
Collector-Emitter Saturation Voltage (I_C = 20 mAdc, I_B = 2.0 mAdc, T_A = +125°C) (I_C = 200 mAdc, I_B = 20 mAdc)	$V_{CE(sat)}$	- -	0.25 0.75	Vdc
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 200 mAdc, I_B = 20 mAdc)	$V_{BE(sat)}$	0.7 -	0.8 1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 20 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	300	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	-	6.0	pF
Turn-On Time ($V_{BE(off)}$ ≧ 0.2 Vdc, I_C = 200 mAdc, I_{B1} = 40 mAdc) (Figure 2)	t_{on}	-	40	ns
Turn-Off Time (I_C = 200 mAdc, I_{B1} = 40 mAdc, I_{B2} = 20 mAdc) (Figure 2)	t_{off}	-	40	ns
Storage Time ($I_C \approx I_{B1} \approx I_{B2} \approx$ 20 mAdc) (Figure 1)	t_s	-	20	ns

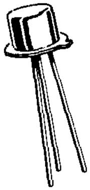
*Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

FIGURE 2 — TURN-ON AND TURN-OFF TEST CIRCUIT



2N3211 (SILICON)

V_{CEO} = 15 V
I_C = 500 mA
P_D = 360 mW



CASE 22
(TO-18)

NPN silicon high frequency switching transistor designed for high speed, saturated switching applications for industrial service.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current	I_C	500	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.36 2.06	Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.2 6.9	Watts mW/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C
Lead Temperature 1/16" ± 1/32" from Case for 60 s		300	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 30 mAdc, I_B = 0)	BV_{CEO}	15	-	Vdc
Collector-Base Breakdown Voltage (I_C = 10 µAdc, I_E = 0)	BV_{CBO}	40	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 µAdc, I_C = 0)	BV_{EBO}	6.0	-	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	I_{CEX}	-	25	nAdc
Base Cutoff Current (V_{CE} = 20 Vdc, $V_{EB(off)}$ = 3.0 Vdc) (V_{CE} = 20 Vdc, $V_{EB(off)}$ = 3.0 Vdc, T_A = 85°C)	I_{BL}	 - -	 0.025 10	µAdc
ON CHARACTERISTICS				
DC Current Gain* (I_C = 100 µAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc) (I_C = 10 mAdc, V_{CE} = 1.0 Vdc) (I_C = 10 mAdc, V_{CE} = 1.0 Vdc, T_A = -55°C) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 100 mAdc, V_{CE} = 1.0 Vdc) (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}*	 20 50 50 20 40 30 10	 - - 150 - - - -	-
Collector-Emitter Saturation Voltage* (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 50 mAdc, I_B = 5.0 mAdc) (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$*	 - - -	 0.2 0.3 0.4	Vdc
Base-Emitter Saturation Voltage* (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 50 mAdc, I_B = 5.0 mAdc) (I_C = 100 mAdc, I_B = 10 mAdc)	$V_{BE(sat)}$*	 - - -	 0.85 1.0 1.2	Vdc

*Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

2N3211 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	350	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	-	4.0	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{ib}	-	7.0	pF
Charge-Storage Time Constant ($I_C \approx I_{B1} \approx I_{B2} \approx$ 10 mAdc) (Figure 1)	τ_s	-	15	ns
Total Control Charge (I_C = 10 mAdc, I_B = 1.0 mAdc) (Figure 2)	Q_T	-	60	pC
Active Region Time Constant (I_C = 10 mAdc, I_B = 1.0 mAdc) (Figure 3)	τ_A	-	2.5	ns

FIGURE 1 — CHARGE STORAGE TIME CONSTANT TEST CIRCUIT

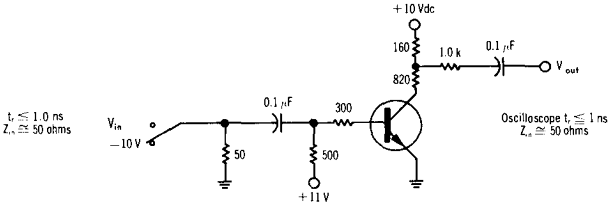


FIGURE 2 — TOTAL CONTROL CHARGE TEST CIRCUIT

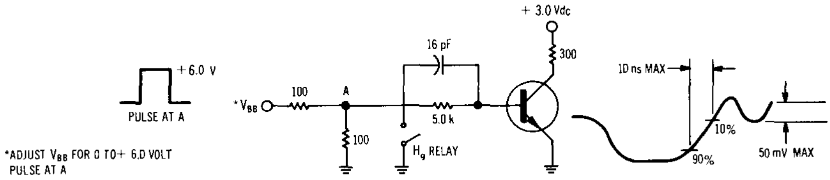
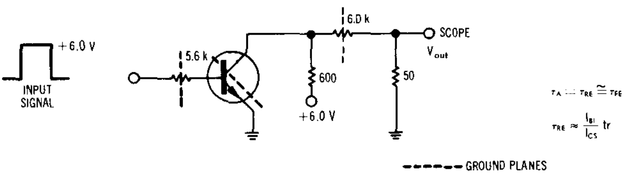


FIGURE 3 — ACTIVE REGION TIME CONSTANT TEST CIRCUIT

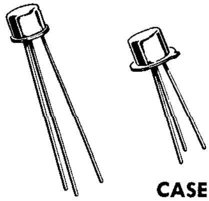


NOTES FOR FIGURES 2, 3

INPUT PULSE – TRANSITION TIME TO +6.0 Vdc ≤ 2.0 ns
INPUT PULSE – OPTIONAL GENERATOR OUTPUT IMPEDANCE: ADJUST FOR +6.0 Vdc
SCOPE INPUT CAPACITANCE ≤ 3.0 pF MAX
SCOPE INPUT IMPEDANCE = 10 MEGOHMS
SCOPE RISE TIME ≤ 0.7 ns

2N3299 thru 2N3302 (SILICON)

V_{CEO} = 30 V
I_C = 500 mA
P_D = 360 to 800 mW



CASE 31
(TO-5)
2N3299
2N3300

CASE 22
(TO-18)
2N3301
2N3302

NPN silicon annular transistors for high-speed switching circuits and DC to UHF amplifier applications.

Collector connected to case

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
Collector-Emitter Voltage (Applicable 0 to 10 mAdc)	V_{CEO}	30		Vdc
Collector-Base Voltage	V_{CB}	60		Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	500		mAdc
Operating Junction Temperature Range	T_J	-65 to +200		°C
Storage Temperature Range	T_{stg}	-65 to +300		°C
		2N3299 2N3300	2N3301 2N3302	
Total Device Dissipation @ T_A = 25°C	P_D	0.8	0.36	Watt
Derate above 25°C		4.56	2.06	mW/°C
Total Device Dissipation @ T_C = 25°C	P_D	3.0	1.8	Watts
Derate above 25°C		17.2	10.3	mW/°C

FIGURE 1 — SATURATED TURN-ON SWITCHING TIME TEST CIRCUIT

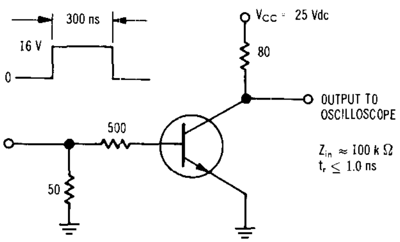
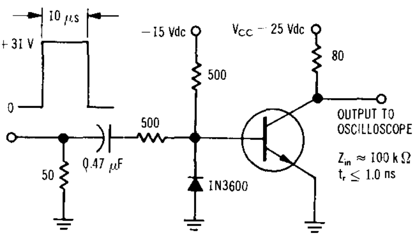


FIGURE 2 — SATURATED TURN-OFF SWITCHING TIME TEST CIRCUIT



2N3299 thru 2N3302 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

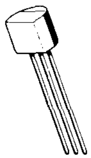
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 10 mAdc, I_B = 0)		BV_{CEO}*	30	-	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)		BV_{CBO}	60	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		BV_{EBO}	5.0	-	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, V_{BE} = 0)		I_{CES}	-	0.01	μAdc
(V_{CE} = 50 Vdc, V_{BE} = 0, T_A = 150°C)			-	10	
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)		I_{EBO}	-	10	nAdc
Base Current (V_{CE} = 50 Vdc, V_{BE} = 0)		I_B	-	10	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.1 mAdc, V_{CE} = 10 Vdc)	2N3299, 2N3301	h_{FE}	20	-	-
	2N3300, 2N3302		35	-	
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)	2N3299, 2N3301		25	-	
	2N3300, 2N3302		50	-	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)*	2N3299, 2N3301		35	-	
	2N3300, 2N3302		75	-	
(I_C = 150 mAdc, V_{CE} = 1.0 Vdc)*	2N3299, 2N3301		20	-	
	2N3300, 2N3302		50	-	
(I_C = 150 mAdc, V_{CE} = 10 Vdc)*	2N3299, 2N3301		40	120	
	2N3300, 2N3302		100	300	
(I_C = 500 mAdc, V_{CE} = 10 Vdc)*	2N3299, 2N3301		20	-	
	2N3300, 2N3302		50	-	
Collector-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)		$V_{CE(sat)}$	-	0.22	Vdc
(I_C = 300 mAdc, I_B = 30 mAdc)			-	0.45	
(I_C = 500 mAdc, I_B = 50 mAdc)			-	0.6	
Base-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)		$V_{BE(sat)}$	-	1.1	Vdc
(I_C = 300 mAdc, I_B = 30 mAdc)			-	1.3	
(I_C = 500 mAdc, I_B = 50 mAdc)			-	1.5	
Base-Emitter On Voltage (I_C = 150 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	-	1.1	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)		f_T	250	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 140 kHz)		C_{ob}	-	8.0	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 140 kHz)		C_{ib}	-	20	pF
Turn-On Time (Figure 1) (V_{CC} = 25 Vdc, I_C ≈ 300 mAdc, I_{B1} ≈ 30 mAdc)		t_{on}	-	60	ns
Turn-Off Time (Figure 2) (V_{CC} = 25 Vdc, I_C ≈ 300 mAdc, I_{B1} = I_{B2} ≈ 30 mAdc)		t_{off}	-	150	ns

* Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2%.

2N4123 (SILICON)
2N4124

V_{CEO} to 30V

I_C = 200 mAdc



CASE 29(1)
(TO-92)

NPN silicon transistors designed for general purpose switching and amplifier applications and for complementary circuitry with PNP types 2N4125 and 2N4126. Features one-piece, injection-molded plastic package for high reliability.

MAXIMUM RATINGS

Characteristic	Symbol	2N4123	2N4124	Unit
Collector-Emitter Voltage	V_{CEO}	30	25	Vdc
Collector-Base Voltage	V_{CB}	40	30	Vdc
Emitter-Base Voltage	V_{EB}	5		Vdc
Collector Current	I_C	200		mAdc
Total Device Dissipation @ T_A = 60°C	P_D	210		mW
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	310 2.81		mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +135		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.357	°C/mW

FIGURE 1 — CAPACITANCE

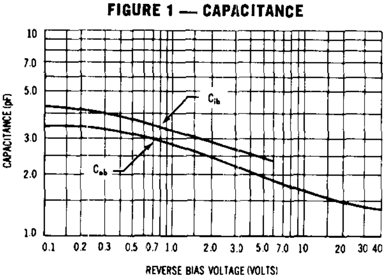
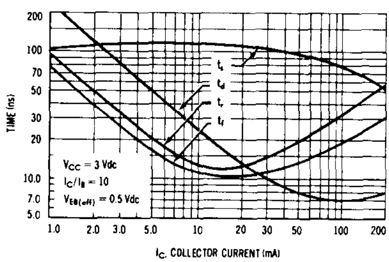


FIGURE 2 — SWITCHING TIMES



2N4123, 2N4124 (continued)

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage* (I_C = 1 mAdc, I_E = 0)	2N4123 2N4124		BV_{CEO}*	30 25	– –	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	2N4123 2N4124		BV_{CBO}	40 30	– –	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)			BV_{EBO}	5	–	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)			I_{CBO}	–	50	nAdc
Emitter Cutoff Current (V_{BE} = 3 Vdc, I_C = 0)			I_{EBO}	–	50	nAdc
ON CHARACTERISTICS						
DC Current Gain* (I_C = 2 mAdc, V_{CE} = 1 Vdc)	2N4123 2N4124	9	h_{FE}*	50 120	150 360	–
(I_C = 50 mAdc, V_{CE} = 1 Vdc)	2N4123 2N4124			25 60	– –	
Collector-Emitter Saturation Voltage* (I_C = 50 mAdc, I_B = 5 mAdc)		10, 11	$V_{CE(sat)}$*	–	0.3	Vdc
Base-Emitter Saturation Voltage* (I_C = 50 mAdc, I_B = 5 mAdc)		11	$V_{BE(sat)}$*	–	0.95	Vdc
SMALL SIGNAL CHARACTERISTICS						
High-Frequency Current Gain (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N4123 2N4124		$\|h_{fe}\|$	2.5 3.0	– –	–
Current-Gain — Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N4123 2N4124		f_T	250 300	– –	MHz
Output Capacitance (V_{CB} = 5 Vdc, I_E = 0, f = 100 kHz)		1	C_{ob}	–	4	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz)		1	C_{ib}	–	8	pF
Small-Signal Current Gain (I_C = 2 mAdc, V_{CE} = 1 Vdc, f = 1 kHz)	2N4123 2N4124	5	h_{fe}	50 120	200 480	–
Noise Figure (I_C = 100 μAdr, V_{CE} = 5 Vdc, R_S = 1 kohm, Noise Bandwidth = 10 Hz to 15.7 kHz)	2N4123 2N4124	3, 4	NF	– –	6 5	dB

SWITCHING CHARACTERISTICS

Characteristic		Fig. No.	Symbol	Typ	Unit
Delay Time	V_{CC} = 3 Vdc, $V_{EB(off)}$ = 0.5 Vdc,	2	t_d	24	ns
Rise Time	I_C = 10 mAdc, I_{B1} = 1 mAdc	2	t_r	13	ns
Storage Time	V_{CC} = 3 Vdc, I_C = 10 mAdc,	2	t_s	125	ns
Fall Time	I_{B1} = I_{B2} = 1 mAdc	2	t_f	11	ns

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%

2N4123, 2N4124 (continued)

AUDIO SMALL SIGNAL CHARACTERISTICS

NOISE FIGURE

V_{CE} = 5 Vdc, T_A = 25°C

FIGURE 3 — FREQUENCY VARIATIONS

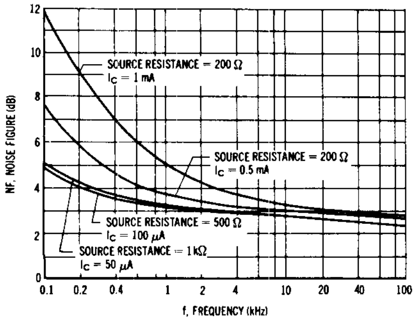
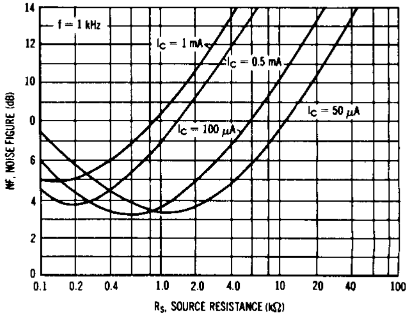


FIGURE 4 — SOURCE RESISTANCE



h PARAMETERS

V_{CE} = 10 V, f = 1 kHz, T_A = 25°C

FIGURE 5 — CURRENT GAIN

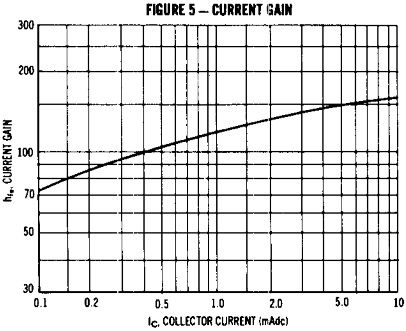


FIGURE 6 — OUTPUT ADMITTANCE

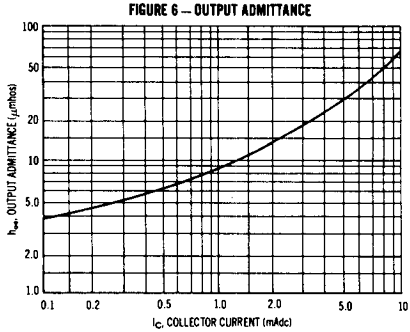


FIGURE 7 — INPUT IMPEDANCE

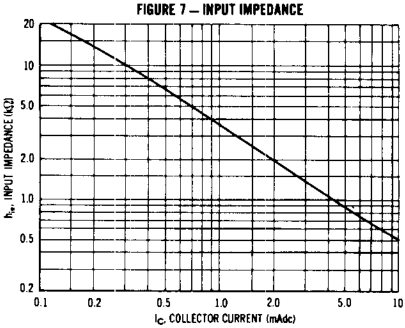
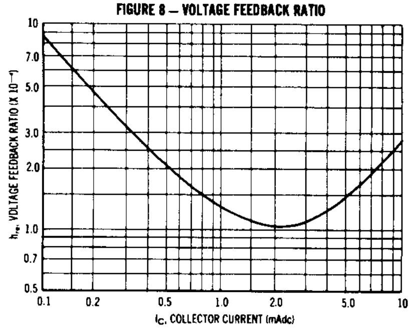


FIGURE 8 — VOLTAGE FEEDBACK RATIO



2N4123, 2N4124 (continued)

STATIC CHARACTERISTICS

FIGURE 9 — NORMALIZED CURRENT GAIN

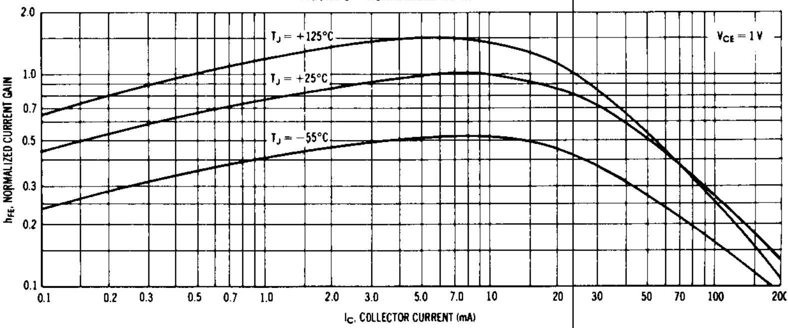


FIGURE 10 — COLLECTOR SATURATION REGION

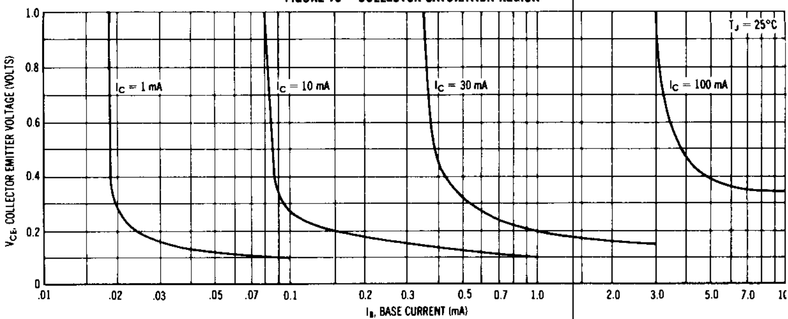


FIGURE 11 — "ON" VOLTAGES

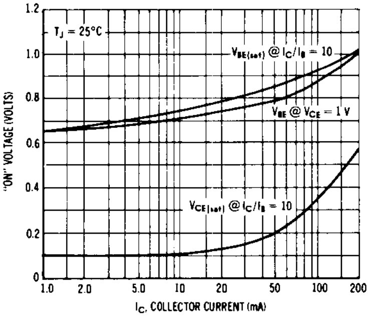
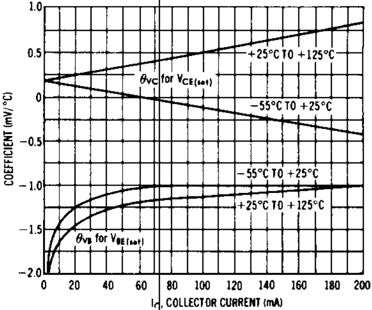


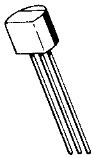
FIGURE 12 — TEMPERATURE COEFFICIENTS



2N4125 (SILICON)
2N4126

V_{CEO} to 30V

I_C = 200 mAdc



CASE 29(1)
(TO-92)

PNP silicon transistors designed for general purpose switching and amplifier applications and for complementary circuitry with NPN types 2N4123 and 2N4124 Features one-piece, injection-molded plastic package for high reliability.

MAXIMUM RATINGS

Characteristic	Symbol	2N4125	2N4126	Unit
Collector-Emitter Voltage	V_{CEO}	30	25	Vdc
Collector-Base Voltage	V_{CB}	30	25	Vdc
Emitter-Base Voltage	V_{EB}	4		Vdc
Collector Current	I_C	200		mAdc
Total Device Dissipation @ T_A = 60°C	P_D	210		mW
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	310 2.81		mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +135		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.357	°C/mW

FIGURE 1 — CAPACITANCE

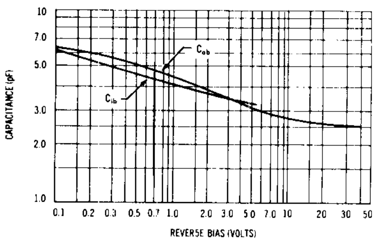
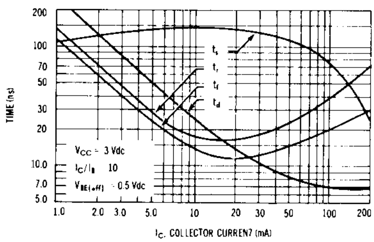


FIGURE 2 — SWITCHING TIMES



2N4125, 2N4126 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage* (I_C = 1 mAdc, I_E = 0)	2N4125 2N4126		BV_{CEO}*	30 25	– –	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	2N4125 2N4126		BV_{CBO}	30 25	– –	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)			BV_{EBO}	4	–	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)			I_{CBO}	–	50	nAdc
Emitter Cutoff Current (V_{BE} = 3 Vdc, I_C = 0)			I_{EBO}	–	50	nAdc
ON CHARACTERISTICS						
DC Current Gain* (I_C = 2 mAdc, V_{CE} = 1 Vdc)	2N4125 2N4126	9	h_{FE}*	50 120	150 360	–
(I_C = 50 mAdc, V_{CE} = 1 Vdc)	2N4125 2N4126			25 60	– –	
Collector-Emitter Saturation Voltage* (I_C = 50 mAdc, I_B = 5 mAdc)		10, 11	$V_{CE(sat)}$*	–	0.4	Vdc
Base-Emitter Saturation Voltage* (I_C = 50 mAdc, I_B = 5 mAdc)		11	$V_{BE(sat)}$*	–	0.95	Vdc
SMALL SIGNAL CHARACTERISTICS						
High-Frequency Current Gain (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N4125 2N4126		$\|h_{fe}\|$	2.0 2.5	– –	–
Current-Gain – Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N4125 2N4126		f_T	200 250	– –	MHz
Output Capacitance (V_{CB} = 5 Vdc, I_E = 0, f = 100 kHz)		1	C_{ob}	–	4.5	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz)		1	C_{ib}	–	10	pF
Small-Signal Current Gain (I_C = 2 mAdc, V_{CE} = 1 Vdc, f = 1 kHz)	2N4125 2N4126	5	h_{fe}	50 120	200 480	–
Noise Figure (I_C = 100 μAdc, V_{CE} = 5 Vdc, R_S = 1 kohm, Noise Bandwidth = 10 Hz to 15.7 kHz)	2N4125 2N4126	3, 4	NF	– –	5.0 4.0	dB

SWITCHING CHARACTERISTICS

Characteristic		Fig. No.	Symbol	Typ	Unit
Delay Time	V_{CC} = 3 Vdc, $V_{BE(off)}$ = 0.5 Vdc,	2	t_d	25	ns
Rise Time	I_C = 10 mAdc, I_{B1} = 1 mAdc	2	t_r	18	ns
Storage Time	V_{CC} = 3 Vdc, I_C = 10 mAdc,	2	t_s	140	ns
Fall Time	I_{B1} = I_{B2} = 1 mAdc	2	t_f	15	ns

*Pulse Test: Pulse Width = 300 μsec, Duty Cycle = 2%

2N4125, 2N4126 (continued)

AUDIO SMALL SIGNAL CHARACTERISTICS

NOISE FIGURE

V_{CE} = 5 Vdc, T_A = 25°C

FIGURE 3 — FREQUENCY VARIATIONS

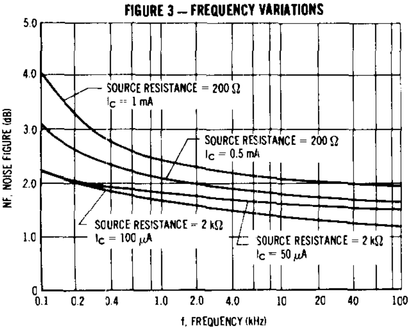
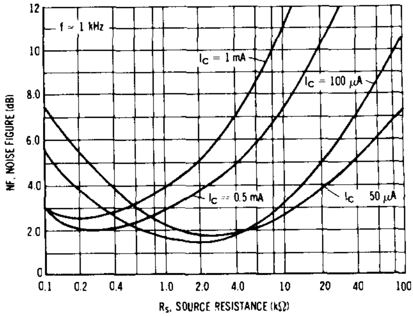


FIGURE 4 — SOURCE RESISTANCE



h PARAMETERS

V_{CE} = 10 V, f = 1 kHz, T_A = 25°C

FIGURE 5 — CURRENT GAIN

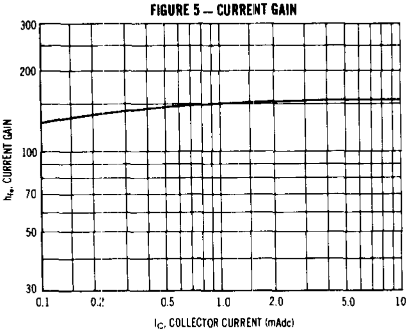


FIGURE 6 — OUTPUT ADMITTANCE

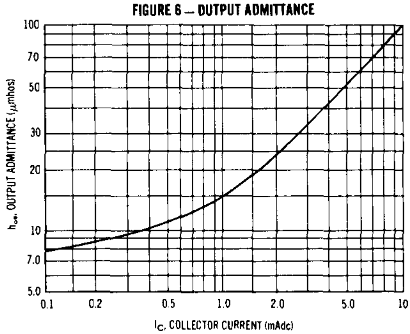


FIGURE 7 — INPUT IMPEDANCE

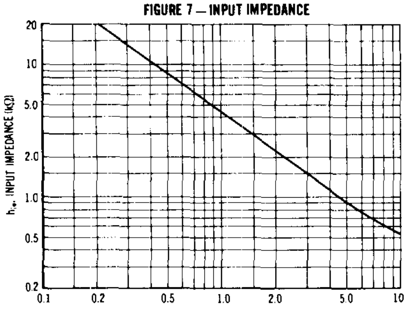
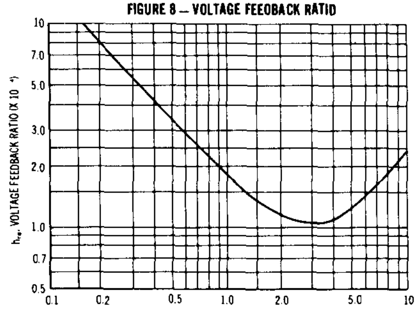


FIGURE 8 — VOLTAGE FEEOBACK RATIO



2N4125, 2N4126 (continued)

STATIC CHARACTERISTICS

FIGURE 9 — NORMALIZED CURRENT GAIN

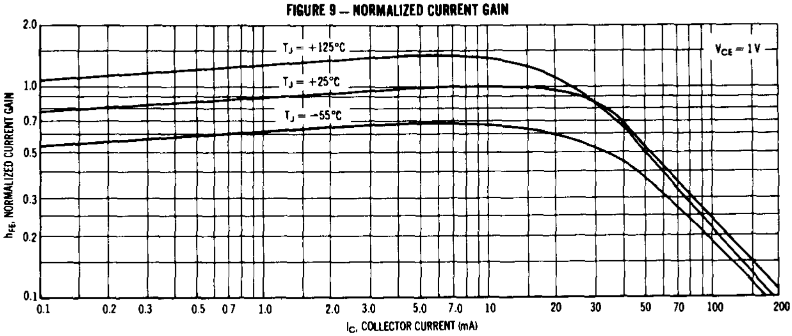


FIGURE 10 — COLLECTOR SATURATION REGION

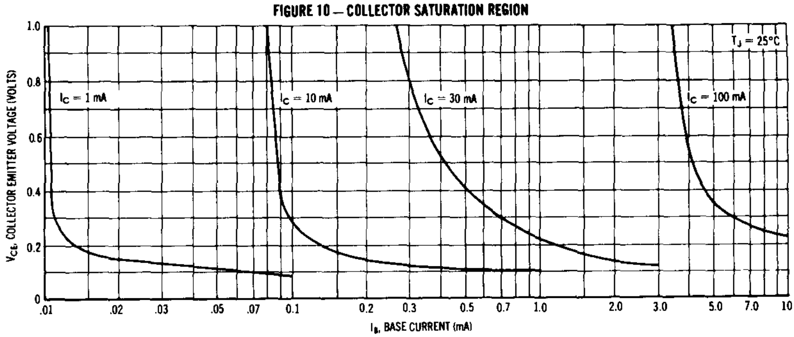


FIGURE 11 — "ON" VOLTAGES

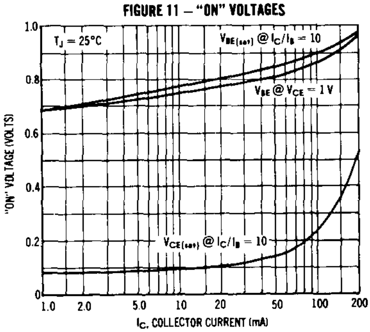
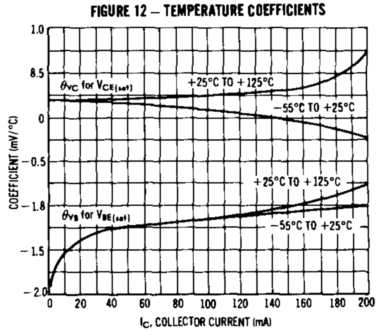


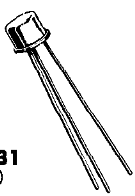
FIGURE 12 — TEMPERATURE COEFFICIENTS



2N4890

V_{CEO} = 40 V
I_C = 700 mA
f_T = 100 MHz

PNP silicon annular transistor designed for medium-current switching and amplifier applications.



CASE 31
(TO-5)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current-Continuous	I_C	700	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 5.7	Watts W/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	5 28.6	Watts W/°C
Operating Junction Temperature Range	T_J	200	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 100 μAdc, I_B = 0)	BV_{CEO}	40	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, R_{BE} = 10 ohms)	BV_{CER}	50	—	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	60	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	5	—	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	—	0.25	μAdc
Base Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{BL}	—	0.25	μAdc
ON CHARACTERISTICS				
DC Current Gain * (I_C = 150 mAdc, V_{CE} = 2.5 Vdc) (I_C = 150 mAdc, V_{CE} = 10 Vdc)*	h_{FE}*	25 50	— 250	—
Collector-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{CE(sat)}$	—	1.4	Vdc
Base-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{BE(sat)}$	—	1.7	Vdc
Base-Emitter On Voltage (I_C = 150 mAdc, V_{CE} = 2.5 Vdc)	$V_{BE(on)}$	—	1.7	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)	f_T	100	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 140 kHz)	C_{ob}	—	15	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 140 kHz)	C_{ib}	—	80	pF

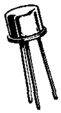
*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%

2N4924 (SILICON)
2N4925

V_{CEO} = 100, 150 V
f_T = 100 – 500 MHz
P_D = 5.0 W

. . . NPN silicon annular transistors designed for high-voltage, high-frequency amplifier applications.

Collector connected to case



CASE 79
(TO-39)

MAXIMUM RATINGS

Rating	Symbol	2N2724	2N2725	Unit
Collector-Emitter Voltage	V_{CEO}	100	150	Vdc
Collector-Base Voltage	V_{CB}	100	150	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current - Continuous	I_C	200		mAdc
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	1.0 5.71		W mW/°C
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	5.0 28.6		W mW/°C
Operating Junction Temperature Range	T_J	-65 to +175		°C
Storage Temperature Range	T_{stg}	-65 to + 200		°C

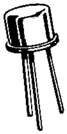
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 10 mAdc, I_B = 0)	2N4924 2N4925	BV_{CEO}*	100 150	- -	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_C = 0)	2N4924 2N4925	BV_{CBO}	100 150	- -	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0	-	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0) (V_{CB} = 75 Vdc, I_E = 0)		I_{CBO}	- -	0.1 0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain* (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 150 mAdc, V_{CE} = 10 Vdc)		h_{FE}*	25 35 40	- - 200	-
Collector-Emitter Saturation Voltage* (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 50 mAdc, I_B = 5.0 mAdc)		$V_{CE(sat)}$*	- -	0.25 0.4	Vdc
Base-Emitter On Voltage* (I_C = 50 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$*	-	0.95	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain - Bandwidth Product (I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)		f_T	100	500	MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 100 kHz)		C_{cb}	-	10	pF
Collector-Emitter Capacitance (V_{BE} = 1.0 Vdc, I_C = 0, f = 100 kHz)		C_{eb}	-	80	pF

*Pulsed, PW = ≤ 300 μs, Duty Cycle = ≤ 2.0%

2N4926 (SILICON)
2N4927

V_{CEO} = 200 – 250 V
I_C = 50 mA
P_D = 5.0 W



CASE 79
(TO-39)

. . . NPN silicon annular transistors designed for high-voltage, high-frequency amplifier applications.

Collector connected to case

MAXIMUM RATINGS

Rating	Symbol	2N4926	2N4927	Unit
Collector-Emitter Voltage	V_{CEO}	200	250	Vdc
Collector-Base Voltage	V_{CB}	200	250	Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current - Continuous	I_C	50		mAdc
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	1.0 5.71		W mW/°C
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	5.0 28.6		W mW/°C
Operating Junction Temperature Range	T_J	-65 to +175		°C
Storage Temperature Range	T_{stg}	-65 to + 200		°C

2N4926, 2N4927 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 0.01 mAdc, I_B = 0)	2N4926 2N4927	BV_{CEO}*	200 250	- -	Vdc
Collector-Base Breakdown Voltage (I_C = 0.1 mAdc, I_C = 0)	2N4926 2N4927	BV_{CBO}	200 250	- -	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)		BV_{EBO}	7.0	-	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0, T_A = 100°C) (V_{CB} = 150 Vdc, I_E = 0) (V_{CB} = 150 Vdc, I_E = 0, T_A = 100°C)	2N4926 2N4927 	I_{CBO}	- - - -	0.1 10 0.1 10	μAdc
Emilter Cutoff Current (V_{BE} = 5.0 V		I_{EBO}	-	0.1	μAdc

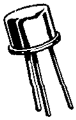
*Pulse Width ≦ 300 μs, Duty Cycle ≦ 1.0%

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS				
DC Current Gain** (I_C = 3.0 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 30 mAdc, V_{CE} = 10 Vdc) (I_C = 50 mAdc, V_{CE} = 20 Vdc)	h_{FE}**	10 15 20 20	- - 200 -	-
Collector-Emitter Saturation Voltage** (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 30 mAdc, I_B = 3.0 mAdc)	$V_{CE(sat)}$**	- -	1.0 2.0	Vdc
Base-Emitter Saturation Voltage** (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 50 mAdc, I_B = 3.0 mAdc)	$V_{BE(sat)}$**	-	1.2 1.5	Vdc
Base-Emitter On Voltage (I_C = 30 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	-	1.5	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)	f_T	30	300	MHz
Output Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 100 kHz)	C_{cb}	-	6.0	pF
Input Impedance (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{ie}	75	750	k ohm
Voltage Feedback Ratio (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{ie}	0.1	1.0	$X10^{-4}$
Small-Signal Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	25	250	-
Output Admittance (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{oe}	5.0	50	μmhos
Real Part of Input Impedance (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 5.0 MHz)	$Re(h_{ie})$	4	40	ohms

** Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%

2N4928 thru 2N4931

V_{CEO} = 100 to 250 V
P_D = 0.6 to 1.0 W



High-voltage PNP silicon annular transistors for use in general purpose high voltage applications.

CASE 79
(TO-39)

Collector connected to case

MAXIMUM RATINGS

Rating	Symbol	2N4928	2N4929	2N4930	2N4931	Unit
Collector-Emitter Voltage	V_{CEO}	100	150	200	250	Vdc
Collector-Base Voltage	V_{CB}	100	150	200	250	Vdc
Emitter-Base Voltage	V_{EB}	4.0	4.0	4.0	4.0	Vdc
Collector Current — Continuous	I_C	100	500	500	500	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.6 3.4	1.0 5.71	1.0 5.71	1.0 5.71	Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	3.0 17.2	5.0 28.6	5.0 28.6	5.0 28.6	Watt mW/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200				°C

2N4928 thru 2N4931 (continued)

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 10 mAdc, I_B = 0)	2N4928	BV_{CEO}*	100	-	Vdc
	2N4929		150	-	
	2N4930		200	-	
	2N4931		250	-	
Collector-Base Breakdown Voltage (I_E = 0, I_C = 100 μAdc)	2N4928	BV_{CBO}	100	-	Vdc
	2N4929		150	-	
	2N4930		200	-	
	2N4931		250	-	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	4.0	-	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	2N4928	I_{CBO}	-	0.5	μAdc
(V_{CB} = 75 Vdc, I_E = 0)	2N4929		-	0.5	
(V_{CB} = 150 Vdc, I_E = 0)	2N4930, 2N4931		-	1.0	
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	2N4928, 2N4929	I_{EBO}	-	0.5	μAdc
(V_{BE} = 3.0 Vdc, I_C = 0)	2N4930, 2N4931		-	1.0	
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc)	All Types	h_{FE}	20	-	-
(I_C = 10 mAdc, V_{CE} = 10 Vdc)*	2N4928, 2N4929		25	200	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)*	2N4930, 2N4931		20	200	
(I_C = 50 mAdc, V_{CE} = 10 Vdc)*	2N4928, 2N4929		20	-	
(I_C = 30 mAdc, V_{CE} = 10 Vdc)*	2N4930, 2N4931		20	-	
Collector-Emitter Saturation Voltage* (I_C = 10 mAdc, I_B = 1.0 mAdc)	2N4928, 2N4929	$V_{CE(sat)}$*	-	0.5	Vdc
	2N4930, 2N4931		-	5.0	
Base-Emitter On Voltage (I_C = 10 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	-	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Gandwidth Product (I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N4928, 2N4929	f_T	100	1,000	MHz
(I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)	2N4930, 2N4931		20	200	
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 140 kHz)	2N4928	C_{cb}	-	6.0	pF
(V_{CB} = 20 Vdc, I_E = 0, f = 140 kHz)	2N4929		-	10	
(V_{CB} = 20 Vdc, I_E = 0, f = 140 kHz)	2N4930, 2N4931		-	20	
Emitter-Base Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 140 kHz)	2N4928	C_{eb}	-	40	pF
(V_{BE} = 1.0 Vdc, I_C = 0, f = 140 kHz)	2N4929		-	80	
(V_{BE} = 0.5 Vdc, I_C = 0, f = 140 kHz)	2N4930, 2N4931		-	400	

Pulse Width ≦ 300 μs: Duty Cycle ≦ 2.0%

2N5086 (SILICON)
2N5087

$V_{CEO} = 50\,V$
$I_C = 50\,mA$
$P_D = 310\,mW$

CASE 29 (1)
(TO-92)

PNP silicon annular transistors designed for low-level, low-noise amplifier applications.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current – Continuous Peak	I_C	50 100	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	310 2.81	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +135	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.357	°C/mW

2N5086, 2N5087 (continued)

ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)		BV_{CEO}	50	-	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)		BV_{CBO}	50	-	-	Vdc
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)		I_{CBO}	-	-	10	nAdc
(V_{CB} = 35 Vdc, I_E = 0)			-	-	50	
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)		I_{EBO}	-	-	50	nAdc
ON CHARACTERISTICS						
DC Current Gain (I_C = 100 μAdc, V_{CE} = 5.0 Vdc)	2N5086	h_{FE}	150	-	500	-
	2N5087		250	-	800	
(I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc)	2N5086		150	-	-	
	2N5087		250	-	-	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	2N5086		150	-	-	
	2N5087		250	-	-	
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)		$V_{CE(sat)}$	-	-	0.3	Vdc
Base-Emitter On Voltage (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc		$V_{BE(on)}$	-	-	0.85	Vdc
DYNAMIC CHARACTERISTICS						
Current-Gain – Bandwidth Product (I_C = 500 μAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)	2N5086	f_T	40	120	-	MHz
	2N5087		40	150	-	
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	-	-	4.0	pF
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	2N5086	h_{fe}	150	-	600	-
	2N5087		250	-	900	
Noise Figure (I_C = 20 μAdc, V_{CE} = 5.0 Vdc, R_S = 10 k ohms, f = 10 Hz to 15.7 kHz)	2N5086	NF	-	-	3.0	dB
	2N5087		-	-	2.0	
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 3.0 k ohms, f = 1.0 kHz)	2N5086		-	1.2	3.0	
	2N5087		-	1.0	2.0	

NOISE FIGURE
V_{CE} = 5.0 Vdc, T_A = 25

FIGURE 1 — FREQUENCY EFFECTS

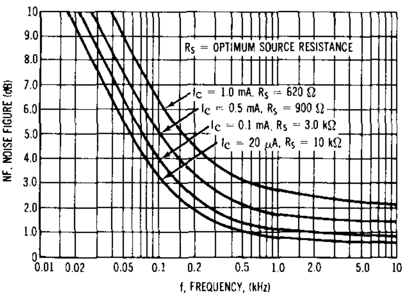
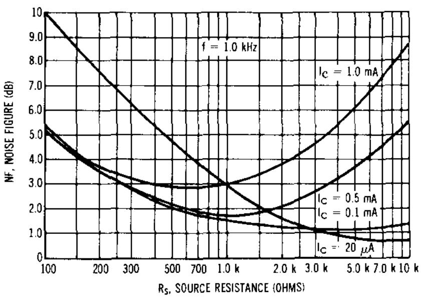


FIGURE 2 — SOURCE RESISTANCE EFFECTS



2N5086, 2N5087 (continued)

h PARAMETERS

V_{CE} = 10 Vdc, f = 1.0 kHz, T_A = 25°C
(For Figures 3, 4, 5, 6, 8)

This group of graphs illustrates the relationship of the "h" parameters for this series of transistors. To obtain these curves, 4 units were selected and identified by number — the same units were used to develop curves on each graph.

FIGURE 3 — INPUT IMPEDANCE

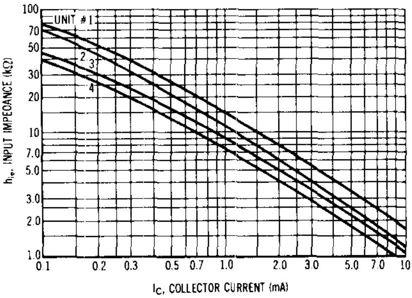


FIGURE 4 — VOLTAGE FEEDBACK RATIO

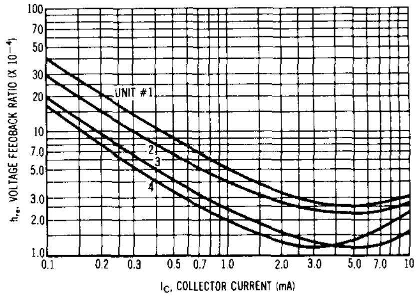


FIGURE 5 — CURRENT GAIN

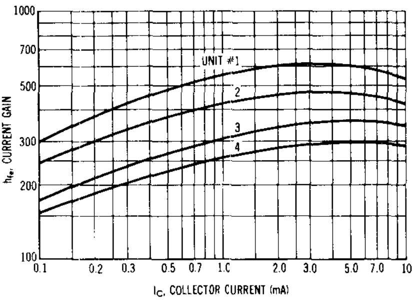


FIGURE 6 — OUTPUT ADMITTANCE

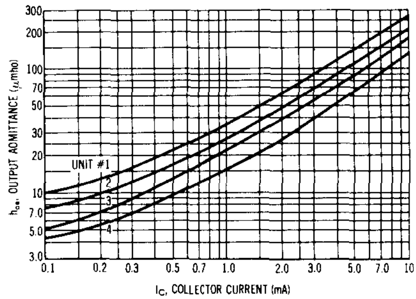


FIGURE 7 — EFFECT OF VOLTAGE

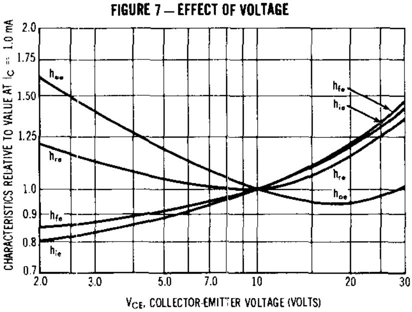
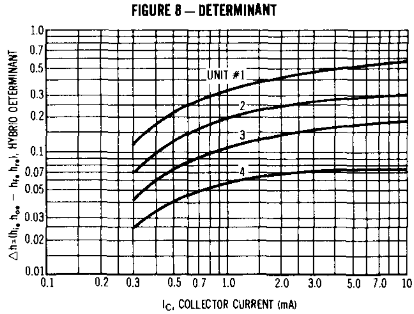


FIGURE 8 — DETERMINANT



2N5086, 2N5087 (continued)

FIGURE 9 — DC CURRENT GAIN

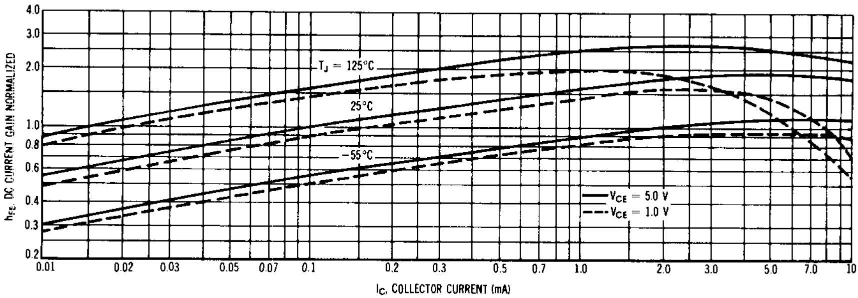


FIGURE 10 — COLLECTOR SATURATION REGION

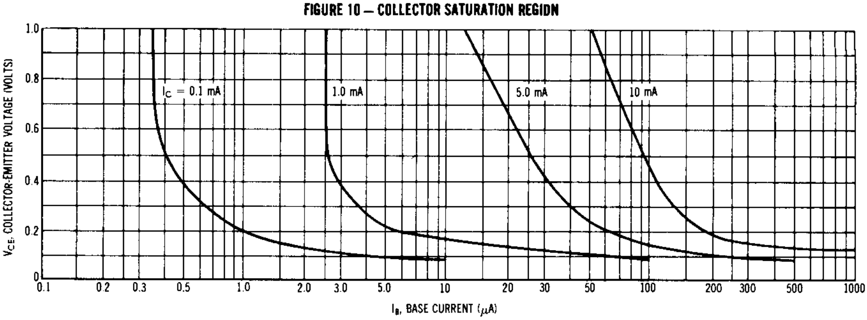


FIGURE 11 — CURRENT-GAIN — BANDWIDTH PRODUCT

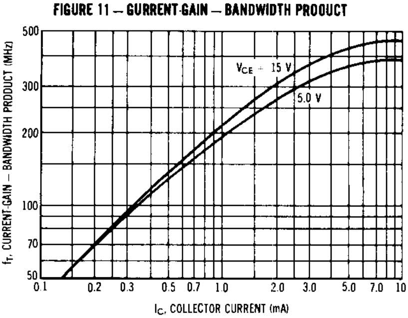
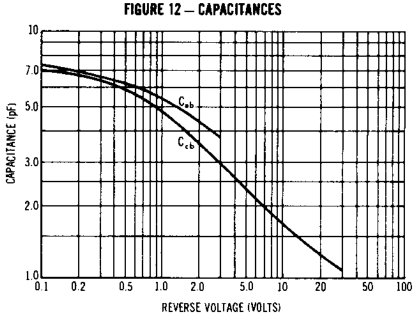
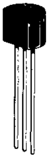


FIGURE 12 — CAPACITANCES



2N5088 (SILICON)
2N5089

V_{CEO} = 25-30 V
I_C = 50 mA
P_D = 310 mW



CASE 29 (1)
(TO-92)

NPN silicon annular transistors designed for low-level, low-noise amplifier applications.

MAXIMUM RATINGS

Rating	Symbol	2N5088	2N5089	Unit
Collector-Emitter Voltage	V_{CEO}	30	25	Vdc
Collector-Base Voltage	V_{CB}	35	30	Vdc
Emitter-Base Voltage	V_{EB}	4.5		Vdc
Collector Current	I_C	50		mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	310 2.81		mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +135		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.357	°C/mW

2N5088, 2N5089 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	2N5088 2N5089	BV_{CEO}	30 25	- -	- -	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	2N5088 2N5089	BV_{CBO}	35 30	- -	- -	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0) (V_{CB} = 15 Vdc, I_E = 0)	2N5088 2N5089	I_{CBO}	- -	- -	50 50	nAdc
Emitter Cutoff Current ($V_{EB(off)}$ = 3.0 Vdc, I_C = 0) ($V_{EB(off)}$ = 4.5 Vdc, I_C = 0)		I_{EBO}	- -	- -	50 100	nAdc
ON CHARACTERISTICS						
DC Current Gain (I_C = 100 μAdc, V_{CE} = 5.0 Vdc) (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc) (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	2N5088 2N5089 2N5088 2N5089 2N5088 2N5089	h_{FE}	300 400 350 450 300 400	- - - - - -	900 1200 - - - -	-
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)		$V_{CE(sat)}$	-	-	0.5	Vdc
Base-Emitter On Voltage (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	-	-	0.8	Vdc
DYNAMIC CHARACTERISTICS						
Current-Gain - Bandwidth Product (I_C = 500 μAdc, V_{CE} = 5.0 Vdc, f = 20 MHz		f_T	50	175	-	MHz
Collector-Base Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 100 kHz, emitter guarded)		C_{cb}	-	1.8	4.0	pF
Emitter-Base Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz, collector guarded)		C_{eb}	-	4.0	10	pF
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	2N5088 2N5089	h_{fe}	350 450	- -	1400 1800	-
Noise Figure (I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 10 k ohms, f = 10 Hz to 15.7 kHz	2N5088 2N5089	NF	- -	- -	3.0 2.0	dB

NOISE FIGURE

V_{CE} = 5.0 Vdc, T_A = 25°C

FIGURE 1 — FREQUENCY EFFECTS

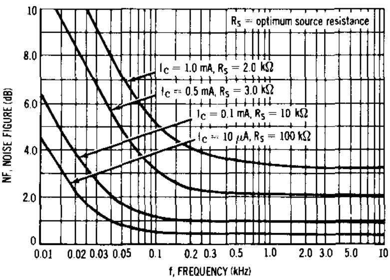
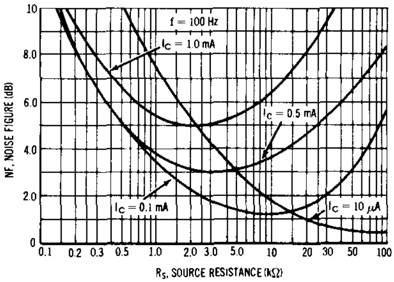


FIGURE 2 — SOURCE RESISTANCE EFFECTS



2N5088, 2N5089 (continued)

h PARAMETERS

V_{CE} = 10 Vdc, f = 1.0 kHz, T_A = 25°C
(For Figures 3, 4, 5, 6, 8)

This group of graphs illustrates the relationship of the "h" parameters for this series of transistors. To obtain these curves, 4 units were selected and identified by number – the same units were used to develop curves on each graph.

FIGURE 3 — INPUT IMPEDANCE

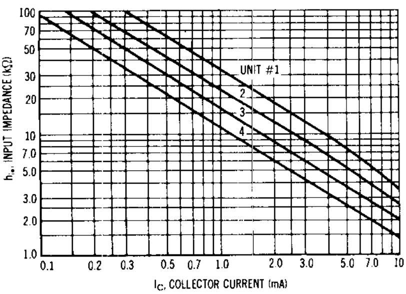


FIGURE 4 — VOLTAGE FEEDBACK RATIO

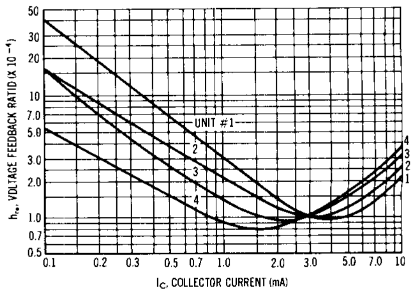


FIGURE 5 — CURRENT GAIN

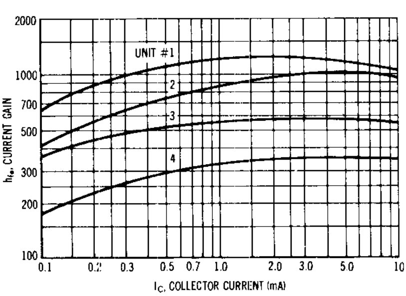


FIGURE 6 — OUTPUT ADMITTANCE

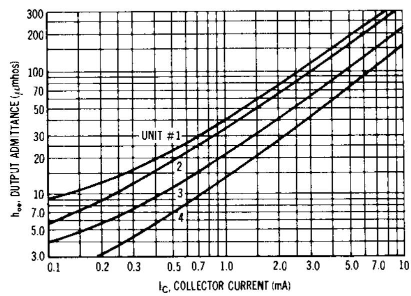


FIGURE 7 — EFFECT OF VOLTAGE

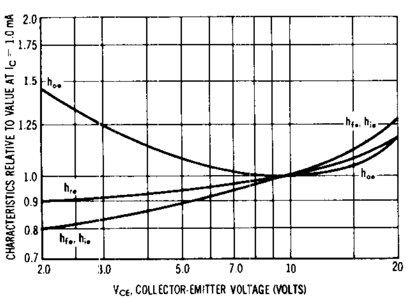
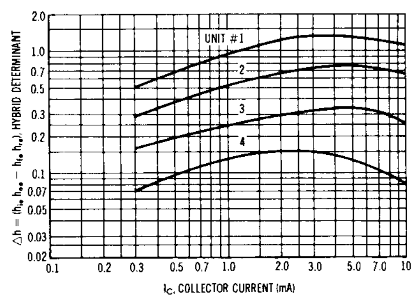


FIGURE 8 — DETERMINANT



2N5088, 2N5089 (continued)

FIGURE 9 — DC CURRENT GAIN

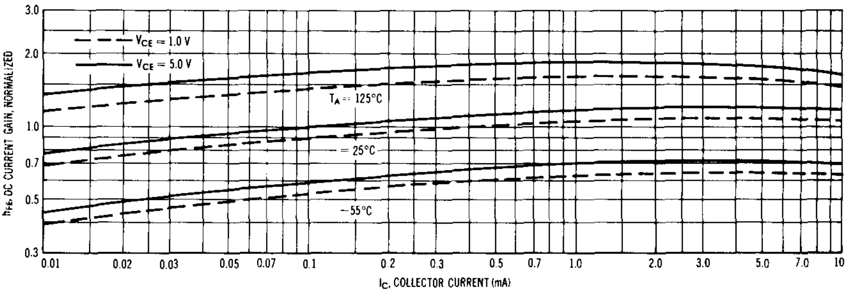


FIGURE 10 — COLLECTOR SATURATION REGION

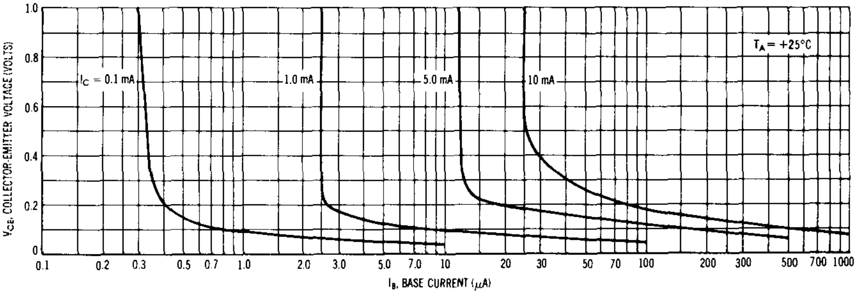


FIGURE 11 — CURRENT GAIN — BANDWIDTH PRODUCT

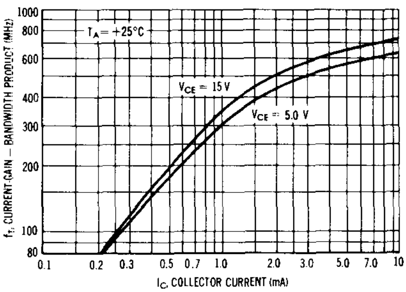
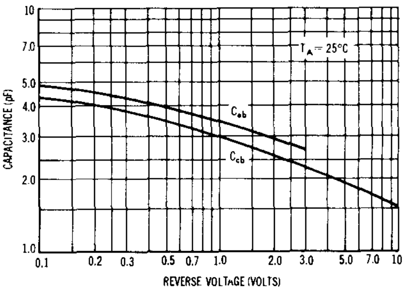
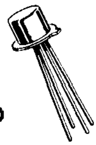


FIGURE 12 — CAPACITANCE



AF239 (GERMANIUM)

V_{CES} = 20 V
I_C = 10 mA
f_T = 720 MHz Typ



CASE 20
(TO-72)

Active Elements Isolated From Case

Germanium high frequency transistor designed for use in UHF/RF amplifier and autodyne converter applications.

MAXIMUM RATINGS

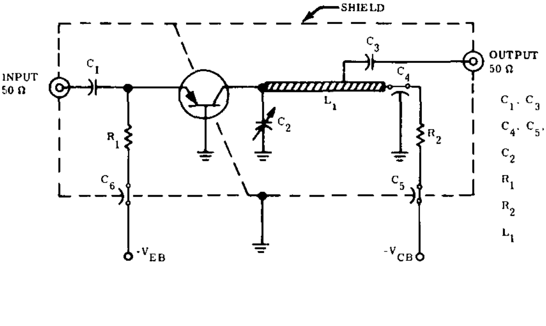
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CES}	20	Vdc
Collector-Base Voltage	V_{CB}	20	Vdc
Emitter-Base Voltage	V_{EB}	0.3	Vdc
Collector Current – Continuous	I_C	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	60 0.8	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +100	°C

AF239 (continued)

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 8.0 μAdc, V_{BE} = 0)	BV_{CES}	20	-	-	Vdc
Collector-Base Breakdown Voltage (I_C = 8.0 μAdc, I_E = 0)	BV_{CBO}	20	-	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	0.3	-	-	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.5 mAdc, V_{CE} = 12 Vdc)	h_{FE}	15	50	-	-
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 1.5 mAdc, V_{CE} = 12 Vdc, f = 100 MHz)	f_T	600	720	-	MHz
Common-Emitter Reverse Transfer Capacitance (V_{CE} = 12 Vdc, I_E = 0, f = 1.0 MHz)	C_{re}	-	0.23	0.30	pF
Collector-Base Time Constant (I_E = 1.5 mAdc, V_{CB} = 12 Vdc, f = 31.8 MHz)	$r_b'C_c$	-	2.0	5.0	ps
Noise Figure (Figure 1) (I_C = 1.5 mAdc, V_{CE} = 12 Vdc, R_S = 50 ohms, f = 800 MHz)	NF	-	5.0	6.0	dB
Noise Figure (Figure 1) (I_C = 1.5 mAdc, V_{CE} = 12 Vdc, R_S = 50 ohms, f = 860 MHz)	NF	-	-	6.7	dB
FUNCTIONAL TEST					
Common-Base Amplifier Power Gain (I_C = 1.5 mAdc, V_{CE} = 12 Vdc, f = 800 MHz) (Figure 1)	G_{pb}	11.2	14	-	dB
Common-Base Amplifier Power Gain (I_C = 1.5 mAdc, V_{CE} = 12 Vdc, f = 860 MHz) (Figure 1)	G_{pb}	-	13.2	-	dB

FIGURE 1 — 800 MHz POWER GAIN AND NOISE FIGURE TEST CIRCUIT



C_1, C_3	10 pF DUR-MICA
C_4, C_5, C_6	240 pF FEEDTHROUGH ERIE
C_2	0.4 - 6.0 pF JOHANSEN
R_1	2.2 k Ω, 0.25 W
R_2	100 Ω, 0.25 W
L_1	SILVER PLATED BRASS STRIP 0.08" WIDE, 0.025" THICK, APPROX. LENGTH 1" – TAP @ 1/3 LENGTH

AF239 (continued)

COMMON-BASE y PARAMETERS

$T_A = 25\ C$

FIGURE 2 — INPUT ADMITTANCE

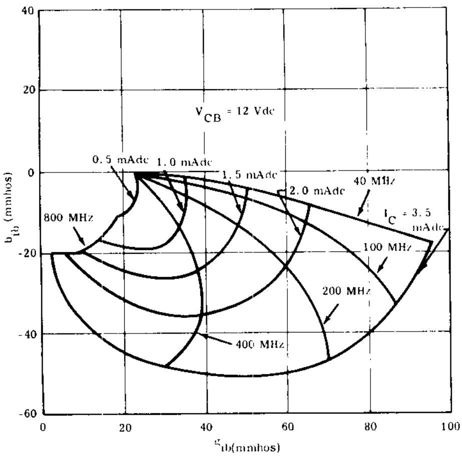


FIGURE 3 — REVERSE TRANSFER ADMITTANCE

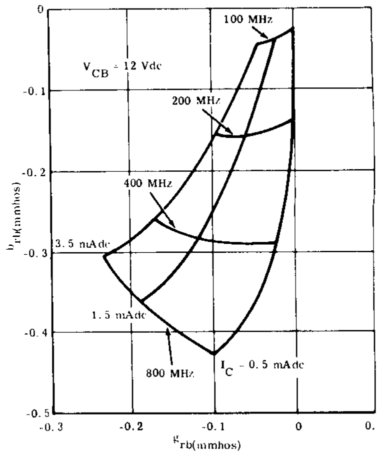


FIGURE 4 — FORWARD TRANSFER ADMITTANCE

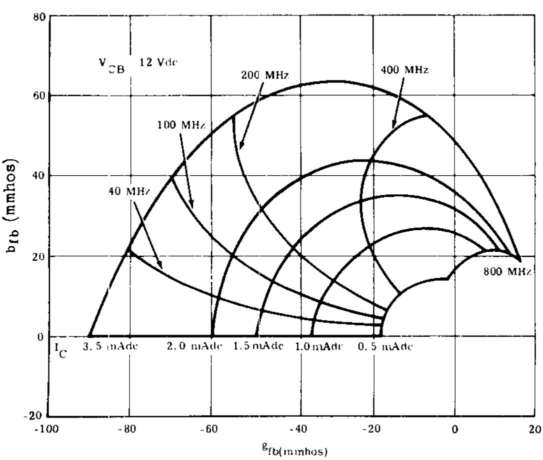
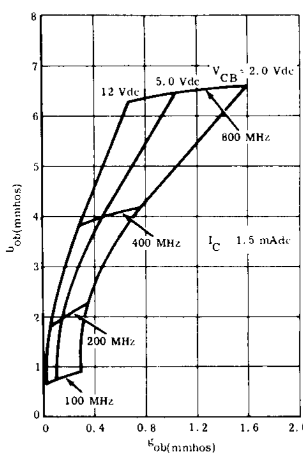


FIGURE 5 — OUTPUT ADMITTANCE



AF239 (continued)

FIGURE 6 — CURRENT-GAIN-BANDWIDTH PRODUCT

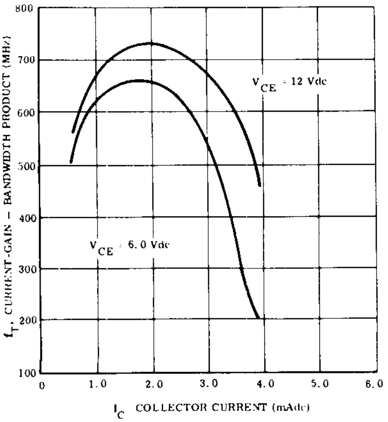
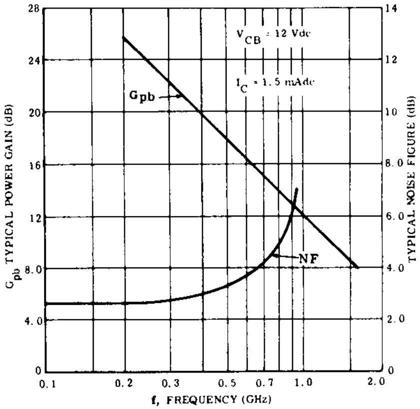


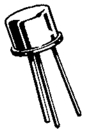
FIGURE 7 — TYPICAL POWER GAIN AND NOISE FIGURE



MM4000 thru MM4003

V_{CEO} = 100 to 250 V
P_D = 0.6 to 1.0 W

High-voltage PNP silicon annular transistors for use in general purpose, high-voltage applications.



Collector connected to case

CASE 79
(TO-39)

MAXIMUM RATINGS

Rating	Symbol	MM4000	MM4001	MM4002	MM4003	Unit
Collector-Emitter Voltage	V_{CEO}	100	150	200	250	Vdc
Collector-Base Voltage	V_{CB}	100	150	200	250	Vdc
Emitter-Base Voltage	V_{EB}	4.0	4.0	4.0	4.0	Vdc
Collector Current — Continuous	I_C	100	500	500	500	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.6 3.4	1.0 5.71	1.0 5.71	1.0 5.71	Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	3.0 17.2	5.0 28.6	5.0 28.6	5.0 28.6	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200				°C

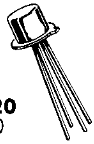
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 10 mAdc, I_B = 0)	MM4000 MM4001 MM4002 MM4003	BV_{CEO}*	100 150 200 250	- - - -	Vdc
Collector-Base Breakdown Voltage (I_E = 0, I_C = 10 μAdc)	MM4000 MM4001 MM4002 MM4003	BV_{CBO}	100 150 200 250	- - - -	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	4.0	-	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0) (V_{CB} = 75 Vdc, I_E = 0) (V_{CB} = 150 Vdc, I_E = 0)	 MM4000 MM4001 MM4002, MM4003	I_{CBO}	 - - -	 1.0 1.0 5.0	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc)*		h_{FE}	20	-	-
Collector-Emitter Saturation Voltage* (I_C = 10 mAdc, I_B = 1.0 mAdc)	MM4000, MM4001 MM4002, MM4003	$V_{CE(sat)}$*	- -	0.6 5.0	Vdc
SMALL SIGNAL CHARACTERISTICS					
Output Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 100 kHz)	MM4000 MM4001 MM4002, MM4003	C_{ob}	- - -	6.0 10 20	pF

* Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

MM5000 (GERMANIUM)
MM5001
MM5002

V_{CEO} = 15 V
I_C = 10 mA
P_D = 150 mW



CASE 20
(TO-72)

Germanium high frequency transistors designed for use in low-noise, high-gain VHF/UHF amplifiers.

Active Elements Isolated From Case

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	0.3	Vdc
Collector Current	I_C	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	150 2.0	mW mW/°C
Operating & Storage Junction Temperature	T_J, T_{stg}	-65 to +100	°C

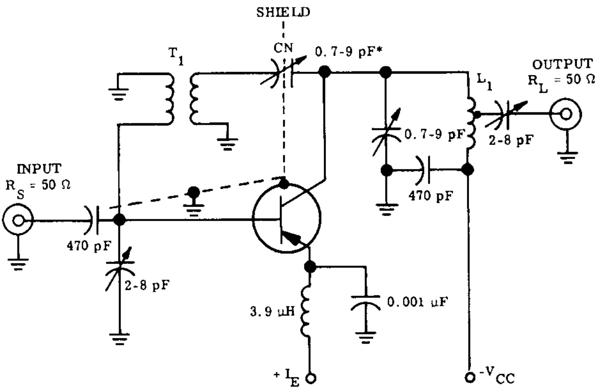


FIGURE 1 — TEST CIRCUIT FOR POWER GAIN AND NOISE FIGURE

NOTES:

L_1 1/4 in. ID, 1/2 in. long, 4 turns #20 solid copper wire, center tapped.

T_1 1/4 in. ID, close wound, 3 turns #26 solid copper wire, 1:1 ratio bi-filler wound.

* High Quality piston type capacitor.

Distance from emitter of transistor to ground side of bypass capacitor should be kept minimal.

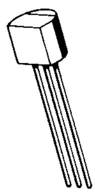
MM5000, MM5001, MM5002 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Units
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 2.0 mAdc, I_B = 0)	BV_{CEO}	15	-	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 µAdc, I_E = 0)	BV_{CBO}	30	-	-	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 3.0 mAdc, V_{CE} = 12 Vdc)	h_{FE}	30	-	-	-
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain-Bandwidth Product (I_C = 3.0 mAdc, V_{CE} = 12 Vdc, f = 100 MHz)	f_T	800	-	-	MHz
Collector-Base Capacitance (V_{CB} = 12 Vdc, I_E = 0, f = 100 kHz)	C_{cb}	-	0.4	0.6	pF
Collector-Base Time Constant (I_E = 3.0 mAdc, V_{CB} = 12 Vdc, f = 31.8 MHz)	$r_b'C_c$				ps
MM5000		-	-	3.5	
MM5001		-	-	5.0	
MM5002		-	-	7.5	
Noise Figure (Figure 1) (I_C = 3.0 mAdc, V_{CE} = 12 Vdc, R_S = 50 ohms, f = 200 MHz)	NF				dB
MM5000		-	-	1.6	
MM5001		-	-	2.0	
MM5002		-	-	2.2	
Noise Figure (I_C = 3.0 mAdc, V_{CE} = 12 Vdc, R_S = 50 ohms, f = 450 MHz)	NF	-	3.5	-	dB
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (I_C = 3.0 mAdc, V_{CE} = 12 Vdc, f = 200 MHz) (Figure 1)	G_{pe}				dB
MM5000		24	-	-	
MM5001		22	-	-	
MM5002		20	-	-	
Common-Emitter Amplifier Power Gain (I_C = 3.0 mAdc, V_{CE} = 12 Vdc, f = 450 MHz)	G_{pe}	-	16	-	dB

MPS 2369 (SILICON)

V_{CEO} = 15 V min
$V_{CE(sat)}$ = 0.25 V max
t_s = 13 ns max



CASE 29 (1)
(TO-92)

NPN silicon annular transistors for high-speed low-current switching applications.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	4.5	Vdc
Collector Current-Peak	I_C	500	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.310 2.81	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to + 135	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.357	°C/mW

FIGURE 1 — t_{on} CIRCUIT

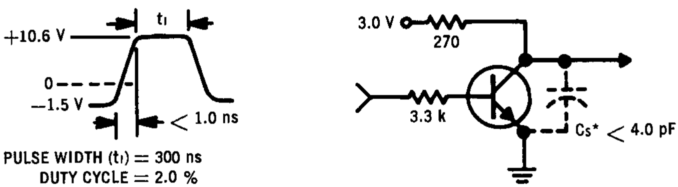
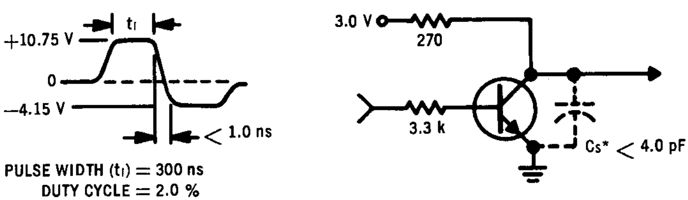


FIGURE 2 — t_{off} CIRCUIT



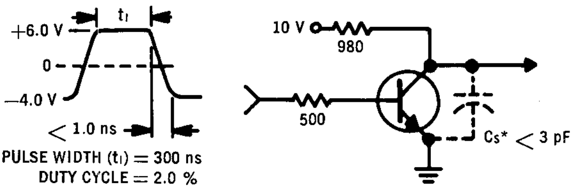
MPS2369 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage* (I_C = 10 mAdc, I_B = 0)	BV_{CEO}*	15	-	Vdc
Collector-Emitter Breakdown Voltage (I_C = 10 µAdc, V_{BE} = 0)	BV_{CES}	40	-	Vdc
Collector-Base Breakdown Voltage (I_C = 10 µAdc, I_E = 0)	BV_{CBO}	40	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 µAdc, I_C = 0)	BV_{EBO}	4.5	-	Vdc
Collector Cutoff Current	I_{CBO}			µAdc
(V_{CB} = 20 Vdc, I_E = 0)		-	0.4	
(V_{CB} = 20 Vdc, I_E = 0, T_A = 125°C)		-	30	
ON CHARACTERISTICS				
DC Current Gain*	h_{FE}*			-
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)		40	120	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc, T_A = -55°C)		20	-	
(I_C = 100 mAdc, V_{CE} = 2.0 Vdc)		20	-	
Collector-Emitter Saturation Voltage* (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$*	-	0.25	Vdc
Base-Emitter Saturation Voltage* (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$*	0.70	0.85	Vdc
SMALL SIGNAL CHARACTERISTICS				
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 140 kHz)	C_{ob}	-	4.0	pF
Small-Signal Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 mHz)	h_{fe}	5.0	-	-
SWITCHING CHARACTERISTICS				
Turn-On Time (V_{CC} = 3.0 Vdc, $V_{BE(off)}$ = 1.5 Vdc, I_C = 10 mAdc, I_{B1} = 3.0 mAdc) (Figure 1)	t_{on}	-	12	ns
Turn-Off Time (V_{CC} = 3.0 Vdc, I_C = 10 mAdc, I_{B1} = 3.0 mAdc, I_{B2} = 1.5 mAdc) (Figure 2)	t_{off}	-	18	ns
Storage Time (I_{B1} = I_{B2} = I_C = 10 mAdc) (Figure 3)	t_s	-	13	ns

* Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2%

FIGURE 3 — STORAGE TEST CIRCUIT



*Total shunt capacitance of test jig and connectors.

RF TRANSISTORS

THE FOLLOWING TRANSISTORS ARE INCLUDED IN THIS SECTION

2N2857
2N3839
2N3127
JAN2N3127
2N4957
2N4958
2N4959
MPS3693
MPS3694

2N2857 (SILICON)
2N3839

V_{CB} = 30 V
P_{out} = 30 mW
NF = 3.7 dB typ @ 450 MHz

CASE 20
(TO-72)

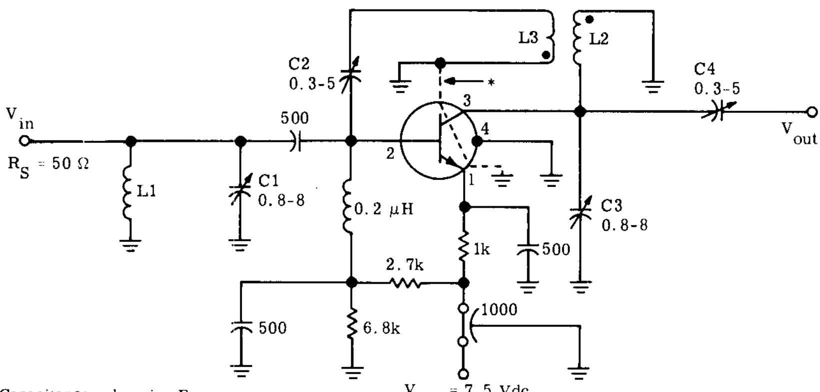
Active elements isolated from case

NPN silicon annular small-signal amplifier transistors designed for high-gain, low-noise amplifiers, oscillators, and mixers.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CB}	30	Vdr
Emitter-Base Voltage	V_{EB}	2.5	Vdc
Collector Current	I_C	40	mAdc
Total Device Dissipation, T_A = 25°C Derate above 25°C	P_D	200 1.14	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

FIGURE 1 – TEST CIRCUIT FOR NOISE FIGURE AND POWER GAIN



Capacitance values in pF

L1, L2 – Silver-plated brass rod, 1-1/2" long and 1/4" dia. Install at least 1/2" from nearest vertical chassis surface.

L3 – 1/2 turn #16 AWG wire, located 1/4" from and parallel to L2

* – External interlead shield to isolate collector lead from emitter and base leads.

Neutralization Procedure:

(A) Connect 450-MHz signal generator (with R_S = 50 ohms) to input terminals of amplifier.

(B) Connect 50-ohm RF voltmeter across output terminals of amplifier.

(C) Apply V_{EE}, and with signal generator adjusted for 5 mV output from amplifier, tune C1, C3, and C4 for maximum output.

(D) Interchange connections to signal generator and RF voltmeter.

(E) With sufficient signal applied to output terminals of amplifier, adjust C2 for minimum indication at input.

(F) Repeat steps (A), (B), and (C) to determine if retuning is necessary.

2N2857, 2N3839 (continued)

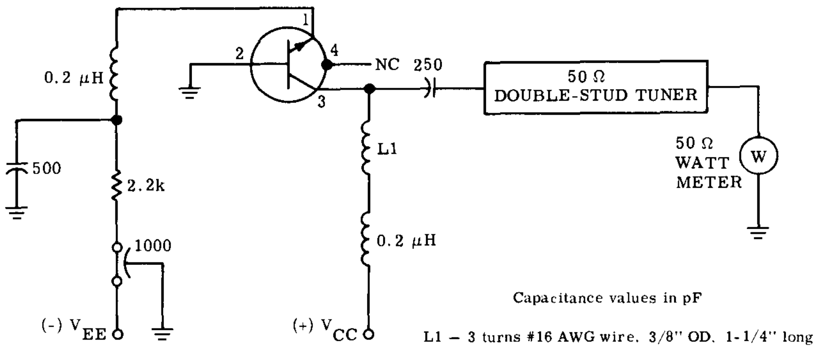
ELECTRICAL CHARACTERISTICS (T_A = 25° C and case grounded unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 3.0 mAdc, I_B = 0)	BV_{CEO}	15	-	-	Vdc
Collector-Base Breakdown Voltage (I_C = 1.0 μAdc, I_E = 0)	BV_{CBO}	30	-	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	2.5	-	-	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	-	-	0.01	μAdc
(V_{CB} = 15 Vdc, I_E = 0, T_A = 150°C)		-	-	1.0	
ON CHARACTERISTICS					
DC Current Gain (I_C = 3.0 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	30	-	150	-
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 5.0 mAdc, V_{CE} = 6.0 Vdc, f = 100 MHz)	f_T	1000	-	-	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 to 1.0 MHz, emitter and case guarded)	C_{cb}	-	-	1.0	pF
Small-Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 6.0 Vdc, f = 1.0 kHz)	h_{fe}	50	-	220	-
Collector-Base Time Constant (I_E = 2.0 mAdc, V_{CB} = 6.0 Vdc, f = 31.9 MHz)	$r_b'C_c$	-	-	15	ps
Noise Figure (I_C = 1.5 mAdc, V_{CE} = 10 Vdc, R_S = 50 ohms, f = 450 MHz) 2N2857	NF	-	3.7†	4.5*	dB
2N3839		-	3.1†	3.4*	
FUNCTIONAL TEST					
Common-Emitter Amplifier Power Gain (I_C = 1.5 mAdc, V_{CE} = 6.0 Vdc, f = 450 MHz, Figure 1)	G_{pe}	12.5	-	19	dB
Oscillator Power Output (I_E = 12 mAdc, V_{CE} = 10 Vdc, f = 500 MHz, Figure 2, fourth lead not connected)	P_{out}	30	-	-	mW

* Noise figure measurements include corrections for input-circuit losses and second-stage post-amplifier contributions per EIA-NEMA Standard #RS-311.

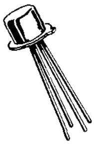
† Measured in circuit of Figure 1 with no corrections.

FIGURE 2 — TEST CIRCUIT FOR OSCILLATOR POWER OUTPUT



JAN 2N3127 (GERMANIUM)
(MIL-S-19500/346 EL)

V_{CEO} = 20 V
I_C = 50 mA
P_D = 100 mW



CASE 20
(TO-72)

PNP germanium mesa transistors designed for industrial and commercial VHF/UHF amplifier applications, and qualified to meet the requirements of MIL-S-19500/346 EL.

Active Elements Isolated From Case

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	20	Vdc
Collector-Emitter Voltage	V_{CES}	25	Vdc
Collector-Base Voltage	V_{CB}	25	Vdc
Emitter-Base Voltage	V_{EB}	0.75	Vdc
Collector Current	I_C	50	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	100 1.33	mW mW/°C
Operating & Storage Junction Temperature	T_J, T_{stg}	-65 to + 100	°C

JAN 2N3127 (continued)

TABLE I – GROUP A INSPECTION (T_A = 25°C unless otherwise noted) (LTPD applies to JAN 2N3127 only)

Examination or Test	MIL-STD-750 Method	Symbol	Limits Min	Limits Max	Unit	LTPD
SUBGROUP 1						
Visual and Mechanical Examination	2071	—	—	—	—	10
SUBGROUP 2						
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	3001 Condition D	BV_{CBO}	25	—	Vdc	5
Collector-Emitter Breakdown Voltage (I_C = 2 mAdc, I_B = 0)	3011 Condition D	BV_{CEO}	20	—	Vdc	
Collector-Emitter Breakdown Voltage (I_C = 100 μAdc, V_{BE} = 0)	3011 Condition C	BV_{CES}	25	—	Vdc	
Collector-Base Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	3036 Condition D	I_{CBO}	—	3	μAdc	
Emitter-Base Cutoff Current (V_{BE} = 0.75 Vdc, I_C = 0)	3061 Condition D	I_{EBO}	—	100	μAdc	
DC Current Gain (I_C = 3 mAdc, V_{CE} = 10 Vdc)	3076	h_{FE}	20	100	—	
Base-Emitter Saturation Voltage (I_C = 5 mAdc, I_B = 1 mAdc)	3066 Condition A	$V_{BE(sat)}$	—	0.6	Vdc	
Collector-Emitter Saturation Voltage (I_C = 5 mAdc, I_B = 1 mAdc)	3071	$V_{CE(sat)}$	—	0.3	Vdc	
SUBGROUP 3						
Small-Signal Current Gain (I_C = 3 mAdc, V_{CE} = 10 Vdc, f = 1 kHz)	3206	h_{fe}	20	125	—	10
Current-Gain — Bandwidth Product (I_C = 2 mAdc, V_{CE} = 6 Vdc, f = 100 MHz)	3261	f_T	400	—	MHz	
Collector - Base Capacitance* (V_{CB} = 10 Vdc, I_E = 0, $f \geq 0.1 \leq 1.0$ MHz)	3236	C_{cb}*	—	1.2	pF	
SUBGROUP 4						
Collector-Base Cutoff Current (V_{CB} = 10 Vdc, I_E = 0, T_A = 85°C)	3036 Condition D	I_{CBO}	—	50	μAdc	10
DC Current Gain ‡ (I_C = 3 mAdc, V_{CE} = 10 Vdc, T_A = -55^{+0}_{-3} °C)	3076	h_{FE}‡	7	—	—	
SUBGROUP 5						
Power Gain (Figure 1) (I_C = 3 mAdc, V_{CE} = 10 Vdc, R_S = 50 ohms, f = 200 MHz)	3256	G_{pe}	17	25	dB	15
Noise Figure (Figure 1) (I_C = 3 mAdc, V_{CE} = 10 Vdc, R_S = 50 ohms, f = 200 MHz)	3246	NF	—	5	dB	

STANDARD UNIT ONLY

Collector-Base Time Constant (Figure 2) (I_C = 3 mAdc, V_{CB} = 10 Vdc, f = 31.8 MHz)	$r_b'C_c$	1	12	ps	—

* Measured in a guarded circuit, such that the can capacitance is not included.

‡ Applies to JAN unit only.

JAN 2N3127 (continued)

TABLE II – GROUP B INSPECTION – JAN 2N3127 only (T_A = 25°C unless otherwise noted)

Examination or Test	MIL-STD-750 Method	Symbol	Limits Min	Limits Max	Unit	LTPD
SUBGROUP 1						
Physical Dimensions	2066	—	—	—	—	20
SUBGROUP 2						
Solderability (Omit aging)	2026	—	—	—	—	15
Temperature Cycling (T_{high} = 100^{+3}_{-0} °C)	1051 Condition B	—	—	—	—	
Thermal Shock (Glass Strain)	1056 Condition A	—	—	—	—	
Seal (Leak Rate)**	** Condition C, Procedure IIIa, Condition B for Gross Leaks	—	—	10^{-7}	atm cc/s	
Moisture Resistance	1021	—	—	—	—	
End-Point Tests: (Subgroups 2, 3)						
Collector-Base Cutoff Current (V_{CB} = 10 Vdc)	3036 Condition D	I_{CBO}	—	3	μAdc	
DC Current Gain (I_C = 3 mAdc, V_{CE} = 10 Vdc)	3076	h_{FE}	20	100	—	
SUBGROUP 3						
Shock (Non-operating; 1500 G; 5 blows of 0.5 ms each in Orientations X_1, Y_1, Y_2, and Z_1 (total = 20 blows)	2016	—	—	—	—	15
Vibration Fatigue (Non-operating; 20G)	2046	—	—	—	—	
Vibration, Variable Frequency	2056	—	—	—	—	
Constant Acceleration (Centrifugal) (20,000G, Orientations X_1, Y_1, Y_2, and Z_1)	2006	—	—	—	—	
End-Point Tests: Same as Subgroup 2						
SUBGROUP 4						
Lead Fatigue	2036 Condition E	—	—	—	—	15
SUBGROUP 5						
High-Temperature Life (Non-operating) (T_{stg} = 100°C)	1031	—	—	—	—	λ = 15
End-Point Tests: (Subgroups 5, 6)						
Collector-Base Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	3036 Condition D	I_{CBO}	—	6	μAdc	
DC Current Gain (I_C = 3 mAdc, V_{CE} = 10 Vdc)	3076	h_{FE}	17	125	—	
SUBGROUP 6						
Steady State Operation Life (I_C = 10 mAdc, V_{CB} = 10 Vdc)	1026	—	—	—	—	λ = 15
End-Point Tests: Same as Subgroup 5						

**Per Method 112 of MIL-STD-202

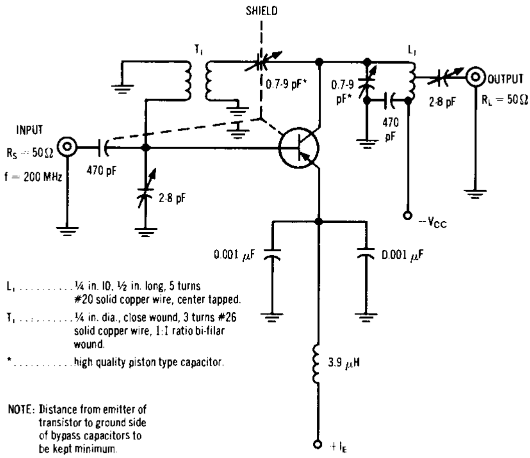
JAN 2N3127 (continued)

TABLE III – GROUP C INSPECTION‡ – JAN 2N3127 only (T_A = 25°C unless otherwise noted)

Examination or Test	MIL-STD-750 Method	Symbol	Limits Min	Limits Max	Unit	LTPD
SUBGROUP 1						
Collector-Base Time Constant (Figure 2) (I_C = 3 mAdc, V_{CB} = 10 Vdc, f = 31.8 MHz)		$r_b'C_c$	—	12	ps	20
Salt Atmosphere (Corrosion)	1041	—	—	—	—	
End-Point Tests:						
Collector-Base Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	3036 Condition D	I_{CBO}	-	3	μAdc	
DC Current Gain (I_C = 3 mAdc, V_{CE} = 10 Vdc)	3076	h_{FE}	20	100	—	
SUBGROUP 2						
Output Conductance (I_C = 2 mAdc, V_{CE} = 6 Vdc, f = 30 MHz)	3216	$Re(h_{oe})$	1.0	3.5	mmhos	10
Input Conductance (I_C = 2 mAdc, V_{CE} = 6 Vdc, f = 30 MHz)	3221	$Re(y_{ie})$	1.25	5.0	mmhos	

‡ Group C tests shall be performed on the initial lot and every six months thereafter.

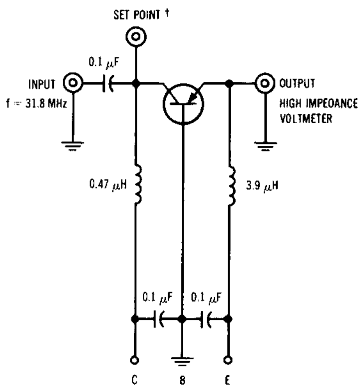
FIGURE 1 – TEST CIRCUIT FOR POWER GAIN AND NOISE FIGURE



L1 ....¼ in. ID, ½ in. long, 5 turns #20 solid copper wire, center tapped.
T1 ....¼ in. dia., close wound, 3 turns #26 solid copper wire, 1:1 ratio bi-filar wound.
* ....high quality piston type capacitor.

NOTE: Distance from emitter of transistor to ground side of bypass capacitors to be kept minimum.

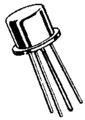
FIGURE 2 – TEST CIRCUIT FOR COLLECTOR-BASE TIME CONSTANT



† NOTE: E_{in} = 0.5 V measured at set point.
$r_b'C_c = E_{out}$ (in mV) × 10

2N4957 (SILICON)
2N4958
2N4959

V_{CEO} = 30 V
I_C = 30 mA
P_D = 200 mW



CASE 20
(TO-72)

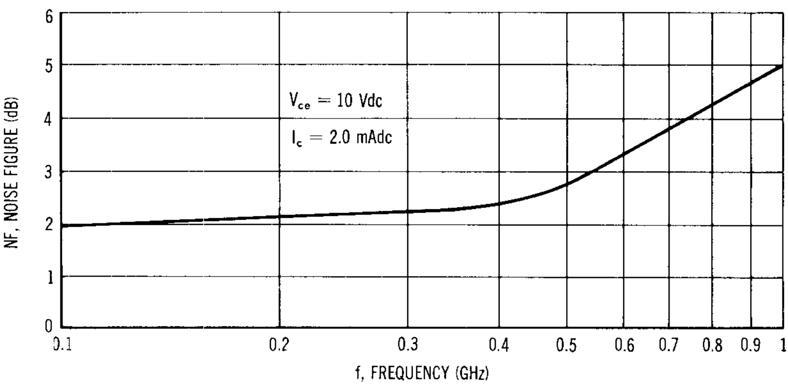
Active Elements Isolated From Case

PNP silicon annular small-signal RF transistor designed for high-gain, low-noise amplifier, oscillator, and mixer applications.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current -- Continuous	I_C	30	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	200 1.14	mWatt mW/°C
Operating Junction & Storage Temperature Range	T_J, T_{stg}	-65 to +200	°C

TYPICAL NOISE FIGURE vs. FREQUENCY (2N4957)

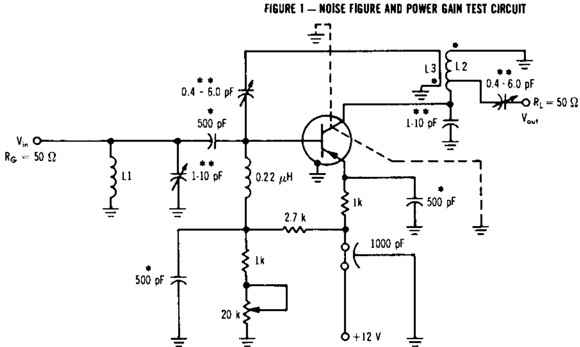


2N4957, 2N4958, 2N4959 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	30	-	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	30	-	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	3.0	-	-	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0) (V_{CB} = 20 Vdc, 0, T_A = 150°C)	I_{CBO}	- -	- -	0.1 100	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc)	h_{FE}	20	40	-	-
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_E = 2.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz) 2N4957 2N4958, 2N4959	f_T	1200 1000	1600 1500	- -	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{cb}	-	0.4	0.8	pF
Collector-Base Time Constant (I_E = 2.0 mAdc, V_{CB} = 10 Vdc, f = 63.6 MHz)	$r_b'C_C$	-	-	8.0	ps
Noise Figure (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 450 MHz) Fig. 1 2N4957 2N4958 2N4959 (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, R_G = 50 ohms, f = 1.0 GHz) 2N4957	NF	- - - -	2.6 2.9 3.2 5.0	3.0 3.3 3.8 -	dB
FUNCTIONAL TESTS					
Common-Emitter Amplifier Power Gain (V_{CE} = 10 Vdc, I_C = 2.0 mAdc, f = 450 MHz) 2N4957 2N4958 2N4959 (V_{CE} = 10 Vdc, I_C = 2.0 mAdc, R_G = 50 ohms, f = 1.0 GHz) 2N4957	G_{pe}	17 16 15 -	- - - 13	- - - -	dB

FIGURE 1 — NOISE FIGURE AND POWER GAIN TEST CIRCUIT



* Button type capacitors
** Variable air piston type capacitors

1. L1 — silver plated brass bar, 1.0 in. lg by 0.25 in od.
2. L2 — silver plated brass bar, 1.5 in. lg by 0.25 in od. Tap is 0.25 in. from collector
3. L3 — ½ turn of AWG #16 wire 0.25 in. from and parallel to L2.
4. The noise source is a hot-cold body (AIL type 70 or equivalent) with a test receiver (AIL type 136 or equivalent).

2N4957, 2N4958, 2N4959 (continued)

COMMON EMITTER Y PARAMETER VARIATIONS

Y PARAMETERS VS FREQUENCY
V_{CE} = 10 Vdc
I_C = 2.0 mAdc

Y PARAMETERS VS CURRENT
V_{CE} = 10 Vdc ——— V_{CE} = 15 Vdc — — —
f = 450 MHZ

FIGURE 2 — INPUT ADMITTANCE

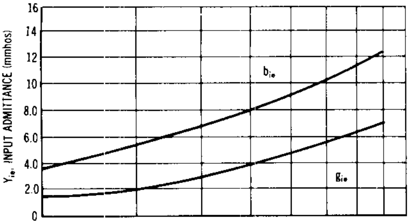


FIGURE 3 — FORWARD TRANSFER ADMITTANCE

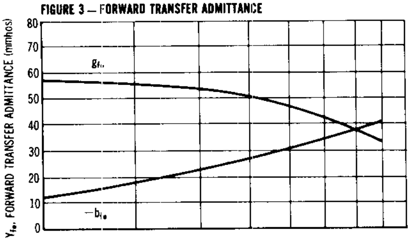


FIGURE 4 — OUTPUT ADMITTANCE

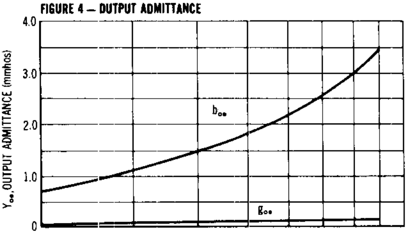


FIGURE 5 — REVERSE TRANSFER ADMITTANCE

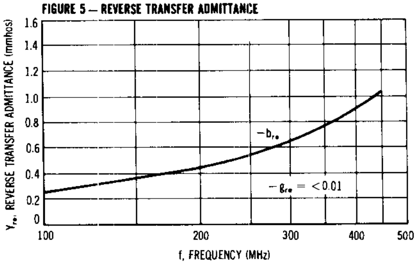


FIGURE 6 — INPUT ADMITTANCE

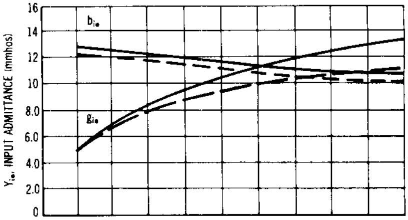


FIGURE 7 — FORWARD TRANSFER ADMITTANCE

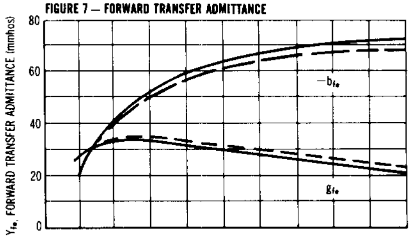


FIGURE 8 — OUTPUT ADMITTANCE

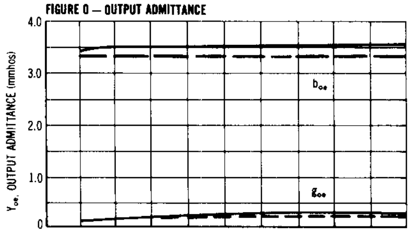
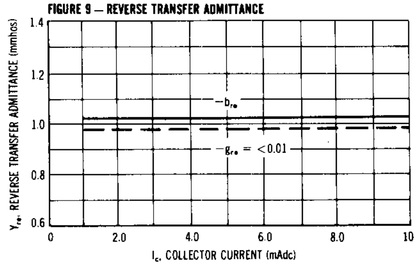


FIGURE 9 — REVERSE TRANSFER ADMITTANCE



2N4957, 2N4958, 2N4959 (continued)

COMMON BASE Y PARAMETER VARIATIONS

Y PARAMETERS versus FREQUENCY
V_{CB} = 10 Vdc
I_C = 2.0 mAdc

FIGURE 10 — INPUT ADMITTANCE

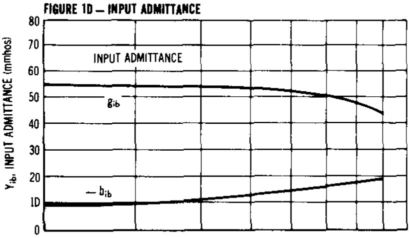


FIGURE 11 — FORWARD TRANSFER ADMITTANCE

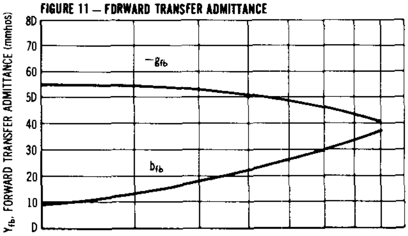


FIGURE 12 — OUTPUT ADMITTANCE

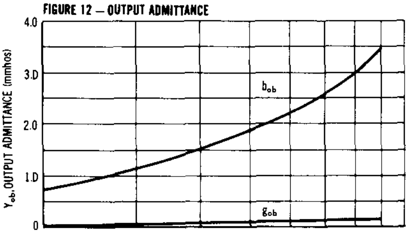
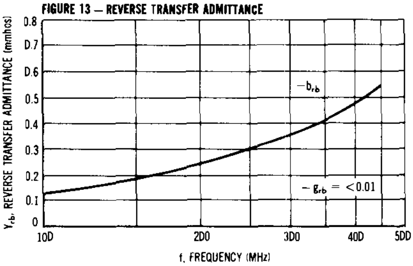


FIGURE 13 — REVERSE TRANSFER ADMITTANCE



Y PARAMETERS versus CURRENT
V_{CB} = 10 Vdc ——— V_{CB} = 15 Vdc – – –
f = 450 MHZ

FIGURE 14 — INPUT ADMITTANCE

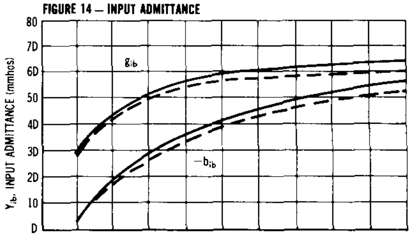


FIGURE 15 — FORWARD TRANSFER ADMITTANCE

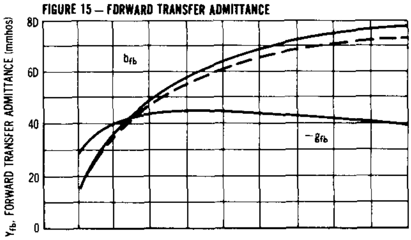


FIGURE 16 — OUTPUT ADMITTANCE

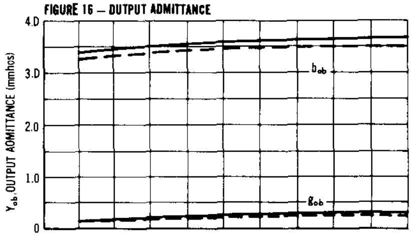
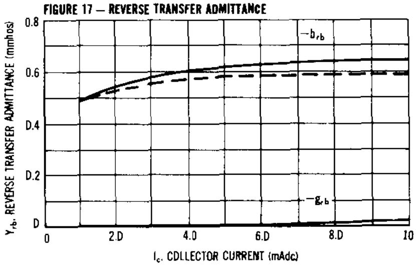
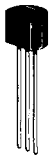


FIGURE 17 — REVERSE TRANSFER ADMITTANCE



MPS3693 (SILICON)
MPS3694

V_{CEO} = 45 V
P_D = 310 mW



CASE 29 (2)
(TO-92)

NPN silicon annular amplifier transistors designed for general purpose RF amplifier applications in the frequency range of up to 50 MHz. These devices are particularly well suited for use in AM/FM receivers.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	45	Vdc
Collector-Base Voltage	V_{CB}	45	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	310 2.81	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +135	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	0.357	°C/mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage* (I_C = 10 mAdc, I_B = 0)	$BV_{CEO(sus)}$*	45	-	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	45	-	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	4.0	-	-	Vdc
Collector Cutoff Current (V_{CB} = 35 Vdc, I_E = 0) (V_{CB} = 35 Vdc, I_E = 0, T_A = 65°C)	I_{CBO}	- -	- -	50 5.0	nAdc μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc) MPS3693 MPS3694	h_{FE}	40 100	- -	160 400	-
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 10 mAdc, V_{CE} = 15 Vdc, f = 100 MHz)	f_T	200	-	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	-	-	3.5	pF
Collector-Base Time Constant (I_E = 10 mAdc, V_{CB} = 15 Vdc, f = 31.8 MHz)	$r'_b C_c$	-	-	55	ps
Noise Figure (I_C = 3.0 mAdc, V_{CE} = 10 Vdc, R_S = 300 ohms, f = 1.0 MHz)	NF	-	4.0	-	dB

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 1.0%.

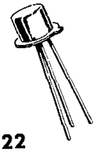
FIELD-EFFECT TRANSISTORS

THE FOLLOWING FIELD-EFFECT TRANSISTORS
ARE INCLUDED IN THIS SECTION

2N3796
2N3797
MPF102

2N3796 (SILICON)
2N3797

V_{DS} = 20-25 V
$|Y_{fs}|$ = 900-1500 μmhos (min)
P_D = 200 mW



CASE 22
(TO-18)

Silicon n-channel MOS field-effect transistor designed for low-power applications in the audio frequency range.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage 2N3796 2N3797	V_{DS}	 25 20	Vdc
Gate-Source Voltage	V_{GS}	±10	Vdc
Drain Current	I_D	20	mAdc
Power Dissipation at T_A = 25°C Derate above 25°C	P_D	200 1.14	mW mW/°C
Operating Junction Temperature	T_J	+200	°C
Storage Temperature	T_{stg}	-65 to +200	°C

HANDLING CONSIDERATIONS:

MOS field-effect transistors, due to their extremely high input resistance, are subject to potential damage by the accumulation of excess static charge. To avoid possible damage to the devices while handling, testing, or in actual operation. the following procedure should be followed:

1. The leads of the devices should remain wrapped in the shipping lead washer or foil except when being tested or in actual operation to avoid the build-up of static charge.
2. Avoid unnecessary handling; when handled, the devices should be picked up by the *can* instead of the leads.
3. The devices should not be inserted or removed from circuits with the power on as transient voltages may cause permanent damage to the devices.

2N3796, 2N3797 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage		BV_{DSX}				Vdc
(V_{GS} = -4.0 V, I_D = 5.0 μA)	2N3796		25	30	—	
(V_{GS} = -7.0 V, I_D = 5.0 μA)	2N3797		20	25	—	
Zero-Gate-Voltage Drain Current		I_{DSS}				mAdc
(V_{DS} = 10 V, V_{GS} = 0)	2N3796		0.5	1.5	3.0	
	2N3797		2.0	2.9	6.0	
Gate-Source Voltage Cutoff		$V_{GS(off)}$				Vdc
(I_D = 0.5 μA, V_{DS} = 10 V)	2N3796		—	-3.0	-4.0	
(I_D = 2.0 μA, V_{DS} = 10 V)	2N3797		—	-5.0	-7.0	
"On" Drain Current		$I_{D(on)}$				mAdc
(V_{DS} = 10 V, V_{GS} = +3.5 V)	2N3796		7.0	8.3	14	
	2N3797		9.0	14	18	
Drain-Gate Reverse Current*		I_{DGO}*				pAdc
(V_{DG} = 10 V, I_S = 0)			—	—	1.0	
Gate-Reverse Current *		I_{GSS}*				pAdc
(V_{GS} = -10 V, V_{DS} = 0)			—	—	1.0	
(V_{GS} = -10 V, V_{DS} = 0, T_A = 150°C)			—	—	200	
Small-Signal, Common-Source Forward Transfer Admittance		$\|y_{fs}\|$				μmhos
(V_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz)	2N3796		900	1200	1800	
	2N3797		1500	2300	3000	
(V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)	2N3796		900	—	—	
	2N3797		1500	—	—	
Small-Signal, Common-Source, Output Admittance		$\|y_{os}\|$				μmhos
(V_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz)	2N3796		—	12	25	
	2N3797		—	27	60	
Small-Signal, Common-Source, Input Capacitance		C_{iss}				pF
(V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)	2N3796		—	5.0	7.0	
	2N3797		—	6.0	8.0	
Small-Signal, Common-Source, Reverse Transfer Capacitance		C_{rss}				pF
(V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)			—	0.5	0.8	
Noise Figure		NF				dB
(V_{DS} = 10 V, V_{GS} = 0, f = 1.0 kHz, R_S = 3 megohms)			—	3.8	—	

* This value of current includes both the FET leakage current as well as the leakage current associated with the test socket and fixture when measured under best attainable conditions.

2N3796, 2N3797 (continued)

TYPICAL DRAIN CHARACTERISTICS

FIGURE 1 – 2N3796

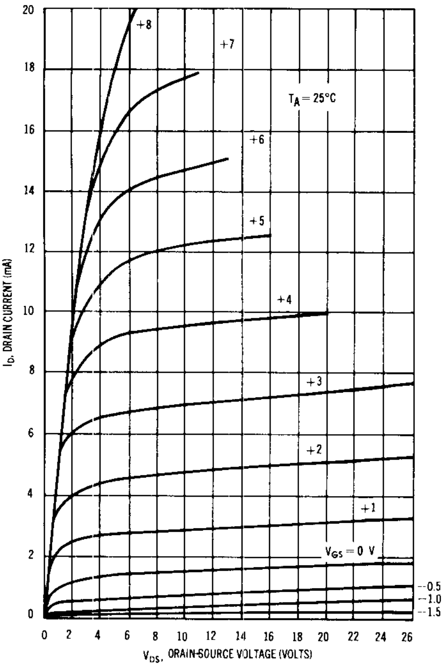
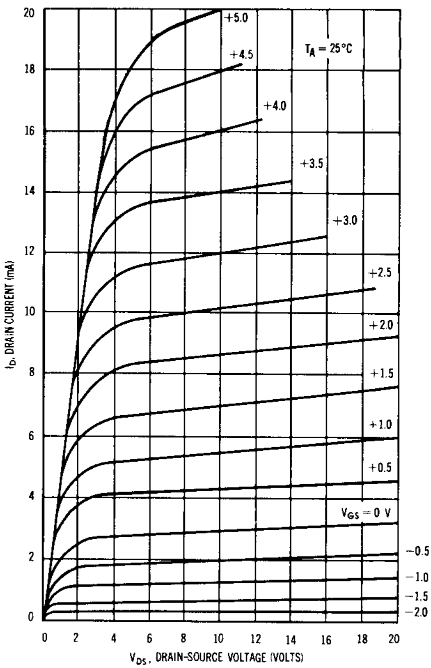


FIGURE 2 – 2N3797



COMMON SOURCE TRANSFER CHARACTERISTICS

FIGURE 3 – 2N3796

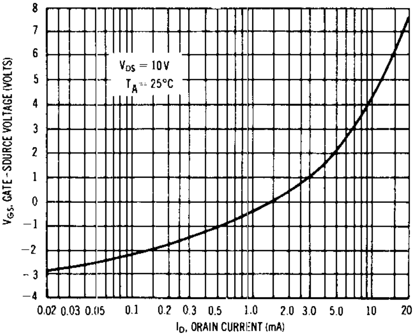
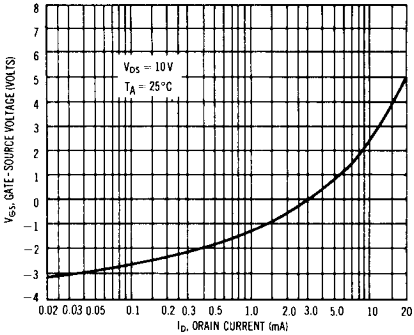


FIGURE 4 – 2N3797



2N3796, 2N3797 (continued)

FIGURE 5 — FORWARD TRANSFER ADMITTANCE

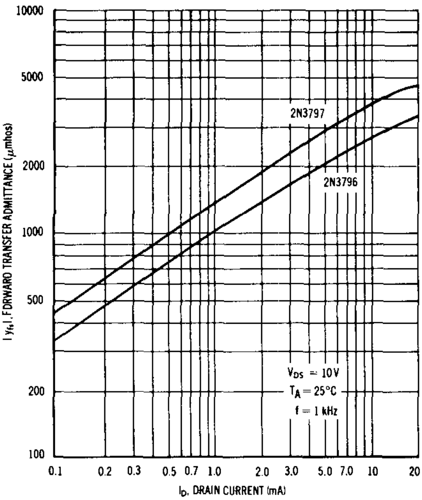


FIGURE 6 — AMPLIFICATION FACTOR

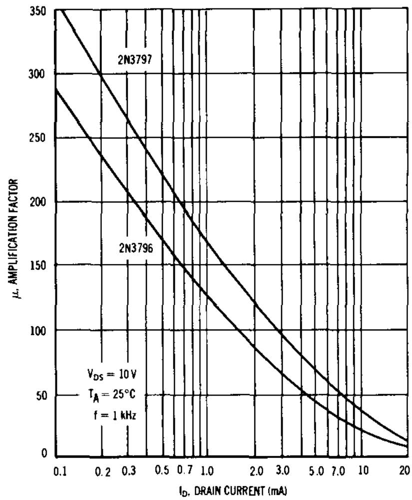


FIGURE 7 — OUTPUT ADMITTANCE

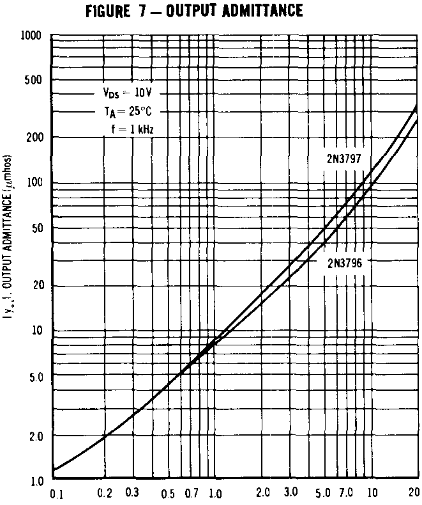
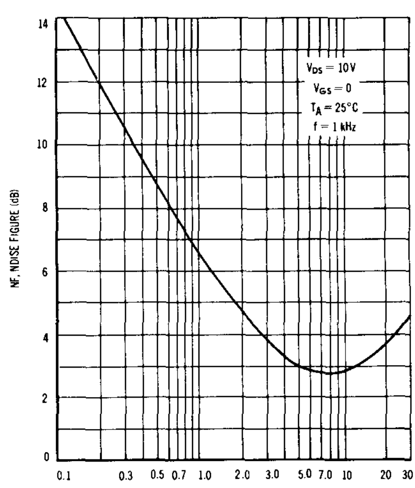


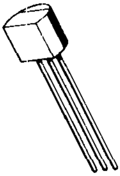
FIGURE 8 — NOISE FIGURE



MPF102

$V_{DS} = 25$ V
$|Y_{fs}| = 1600$ μmhos
$P_D = 200$ mW

Silicon n-channel junction field-effect transistor designed for VHF amplifier and mixer applications.



CASE 29 (5)
(TO-92)

Drain and Source may be interchanged

MAXIMUM RATINGS ($T_A = 25°C$)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	25	Vdc
Gate-Source Voltage	V_{GS}	-25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation Derate above 25°C	P_D	200 2	mW mW/°C
Operating Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate-Source Breakdown Voltage ($I_G = -10$ μAdc, $V_{DS} = 0$)	BV_{GSS}	-25	—	Vdc
Gate Reverse Current ($V_{GS} = -15$ Vdc, $V_{DS} = 0$) ($V_{GS} = -15$ Vdc, $V_{DS} = 0$, $T_A = 100°C$)	I_{GSS}	— —	-2.0 -2.0	nAdc μAdc
Gate-Source Cutoff Voltage ($V_{DS} = 15$ Vdc, $I_D = 2.0$ nAdc)	$V_{GS(off)}$	—	-8	Vdc
Gate-Source Voltage ($V_{DS} = 15$ Vdc, $I_D = 0.2$ mAdc)	V_{GS}	-0.5	-7.5	Vdc
ON CHARACTERISTICS				
Zero-Gate-Voltage Drain Current* ($V_{DS} = 15$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}*	2	20	mAdc
DYNAMIC CHARACTERISTICS				
Forward Transfer Admittance* ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1 kHz)	$\|y_{fs}\|$*	2000	7500	μmhos
Input Capacitance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1 MHz)	C_{iss}	—	7	pF
Reverse Transfer Capacitance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1 MHz)	C_{rss}	—	3	pF
Forward Transfer Admittance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 100 MHz)	$\|y_{fs}\|$	1600	—	μmhos
Input Conductance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 100 MHz)	$Re(y_{is})$	—	600	μmhos
Output Conductance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 100 MHz)	$Re(y_{os})$	—	200	μmhos

*Pulse Test: Pulse Width ≤ 630 ms; Duty Cycle ≤ 10%

MULTIPLE AND SPECIAL DEVICES

Low-current
germanium rectifiers
1N91
1N92
1N93

THE FOLLOWING MULTIPLE DEVICES ARE INCLUDED IN THIS SECTION

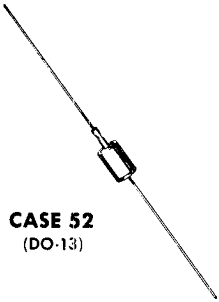
2N2652	2N3800
2N2652A	thru
2N2720	2N3817
2N2721	JAN2N3810
2N2722	JAN2N3811
2N2723	2N3838
2N2724	2N4937
2N2725	2N4938
2N2785	2N4939
2N3423	2N4940
2N3424	2N4941
2N3425	2N4942
2N3515	2N4974
2N3518	2N4975

Special Devices

MRD200	MPZ5-16
MRD300	MPZ5-32
	MPZ5-180

1N91 thru 1N93

$I_O = 1.0$ A
$V_R = 100 - 300$ V



CASE 52
(DO-13)

Low-current germanium rectifiers for applications requiring extremely low forward voltage drop, low power dissipation,and high rectification efficiency, such as biasing and battery charging circuits.

MAXIMUM RATINGS*

Ratings and Conditions	Symbol	1N91	1N92	1N93	Units
Peak Repetitive Reverse Voltage (Rated I_O, $T_A \leq 55°C$, see Figure 2)	$V_{RM(rep)}$	100	200	300	Volts
DC Blocking Voltage $T_A \leq 80°C$	V_R	100	200	300	Volts
$T_A \geq 80°C$		Derate V_R 6.7%/°C above 80°C			
Average Rectified Forward Current (Single Phase, Resistive Load, 60 Hz) $T_A = 55°C$, 100% V_{RM}	I_O	← 1.0 →			Amperes
$T_A = 75°C$, 50% V_{RM}		← 0.25 →			
Non-Repetitive Peak Surge Current (Surge Applied at Rated Load Conditions, see Figure 4)	$I_{FM(surge)}$	← 30 →			Amperes
Operating Junction Temperature Range	T_J	-65 to +95			°C
Storage Temperature Range	T_{stg}	-65 to +125			°C

THERMAL CHARACTERISTICS (ALL TYPES)

Characteristic	Symbol	Max Limit	Unit
Thermal Resistance, Junction to Ambient 1 inch Leads	θ_{JA}	100	°C/W
1/4 inch Leads		70	

ELECTRICAL CHARACTERISTICS (ALL TYPES)

Characteristic	Symbol	Max Limit	Unit
Peak Forward Voltage Drop (I_F = 150 mAdc, $T_A = 25°C$, see Figure 1)	V_F	0.45	Volts
DC Reverse Current (Rated V_R, $T_A = 25°C$, see Figure 3)	I_R	0.22	mA

* These ratings and characteristics as specified may surpass those specified in the original JEDEC registration for these device types.

1N91 thru 1N93 (continued)

FIGURE 1 — FORWARD CHARACTERISTICS

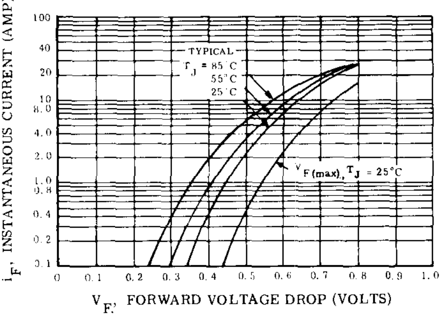


FIGURE 2 — MAXIMUM CURRENT RATINGS

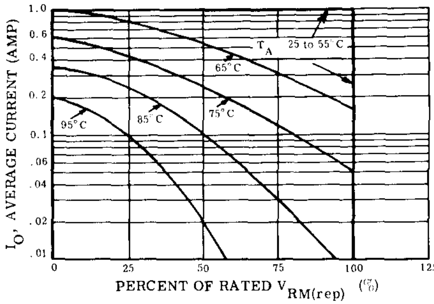


FIGURE 3 — TYPICAL REVERSE CHARACTERISTICS

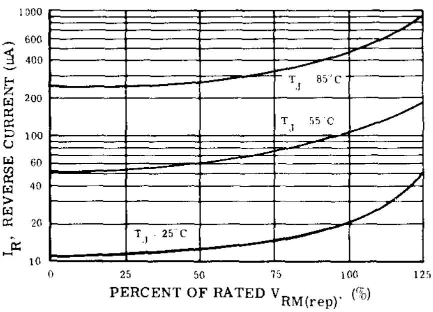
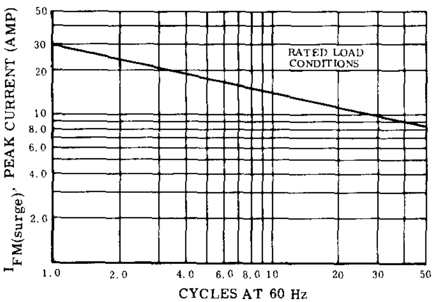
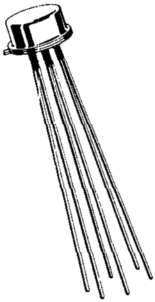


FIGURE 4 — MAXIMUM SURGE CURRENT



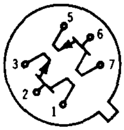
2N2652 (SILICON)
2N2652A

V_{CEO} = 60 V
I_C = 500 mA
P_D = 300 mW one side
600 mW both sides



CASE 32 A

Dual NPN silicon transistors for use as a differential amplifier.



Pin Connections, Bottom View
All Leads Electrically Isolated from Case

MAXIMUM RATINGS (each side)

Rating	Symbol	Value		Unit
Collector-Emitter Voltage	V_{CEO}	60		Vdc
Collector-Base Voltage	V_{CB}	100		Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current	I_C	500		mAdc
Operating Junction Temperature Range	T_J	-65 to +200		°C
Storage Temperature Range	T_{stg}	-65 to +300		°C
		One Side	Both Sides	
Total Device Dissipation @ T_A = 25°C	P_D	0.3	0.6	Watt
Derate above 25°C		1.72	3.43	mW/°C
Total Device Dissipation @ T_C = 25°C	P_D	1.0	2.0	Watts
T_C = 100°C		0.57	1.14	Watt
Derate above 25°C		5.7	11.4	mW/°C

2N2652, 2N2652A (continued)

ELECTRICAL CHARACTERISTICS (each side) (T_A = 25°C unless otherwise noted)

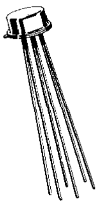
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 20 mAdc, I_B = 0)		BV_{CEO}*	60	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)		BV_{CBO}	100	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	7.0	-	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	2N2652	I_{CBO}	-	0.010	μAdc
	2N2652A		-	0.002	
(V_{CB} = 50 Vdc, I_E = 0, T_A = 150°C)	2N2652		-	15	
	2N2652A		-	10	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	2N2652	I_{EBO}	-	0.010	μAdc
	2N2652A		-	0.002	
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 μAdc, V_{CE} = 5.0 Vdc)		h_{FE}	35	-	-
(I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc)			50	200	
(I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, T_A = -55°C)			15	-	
Collector-Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 5.0 mAdc)		$V_{CE(sat)}$	-	1.2	Vdc
Base-Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 5.0 mAdc)		$V_{BE(sat)}$	-	0.9	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)		f_T	60	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	-	15	pF
Input Capacitance (V_{BE} = 0, 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ib}	-	85	pF
Input Impedance (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)		h_{ie}	1.0	10.5	k ohms
Input Impedance (I_C = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz)		h_{ib}	20	35	ohms
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)		h_{fe}	50	300	-
Output Admittance (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)		h_{oe}	4.0	50	μmhos
Noise Figure (I_C = 0.3 mAdc, V_{CE} = 10 Vdc, R_S = 510 ohms, B. W. = 1.0 Hz, f = 1.0 kHz)		NF	-	8.0	dB
MATCHING CHARACTERISTICS					
DC Current Gain Ratio** (I_C = 100 μAdc, V_{CE} = 5.0 Vdc)	2N2652	h_{FE1}/h_{FE2}**	0.85	1.0	-
	2N2652A		0.9	1.0	
(I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc)	2N2652		0.85	1.0	
	2N2652A		0.9	1.0	
Base Voltage Differential (I_C = 100 μAdc, V_{CE} = 5.0 Vdc)		$\lvert V_{BE1}-V_{BE2}\rvert$	-	3.0	mVdc
(I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc)			-	3.0	
Base Voltage Differential Gradient (I_C = 100 μAdc, V_{CE} = 5.0 Vdc, T_A = -55 to +125°C)		$\left\lvert \frac{\Delta V_{BE1}-V_{BE2}}{\Delta T_A} \right\rvert$	-	10	μV/°C

* Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

** The lowest of the two h_{FE} readings is taken as h_{FE1} for the purpose of measurement.

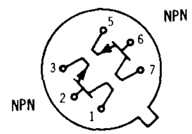
2N2720 (SILICON)
2N2721

V_{CEO} = 60 V
I_C = 40 mA
P_D = 300 mW one side
600 mW both sides



CASE 32A

Dual NPN silicon transistors for small-signal, low-power differential amplifier applications.



Pin Connections Bottom View
All Leads Electrically Isolated from Case

MAXIMUM RATINGS (each side) (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value		Unit
Collector-Emitter Voltage	V_{CEO}	60		Vdc
Collector-Base Voltage	V_{CB}	80		Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current	I_C	40		mAdc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C
		One Side	Both Sides	
Total Device Dissipation @ T_A = 25°C	P_D	0.3	0.6	Watt
Derate above 25°C		1.71	3.4	mW/°C
Total Device Dissipation @ T_C = 25°C	P_D	0.6	1.2	Watts
Derate above 25°C		3.4	6.8	mW/°C

2N2720, 2N2721 (continued)

ELECTRICAL CHARACTERISTICS (each side) (T_A = 25°C unless otherwise noted)

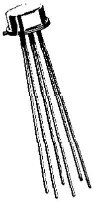
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 10 mAdc, I_B = 0)		BV_{CEO}*	60	-	Vdc
Collector Cutoff Current (V_{CE} = 5.0 Vdc, I_B = 0)		I_{CEO}	-	10	nAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0, T_A = 150°C)		I_{CBO}	- -	0.01 10	μAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	-	10	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 μAdc, V_{CE} = 5.0 Vdc) (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc) (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)		h_{FE}	 30 35 42	 120 - -	-
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)		$V_{CE(sat)}$	-	1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)		$V_{BE(sat)}$	0.65	0.85	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)		f_T	80	-	MHz
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	-	6.0	pF
Input Impedance (I_E = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz)		h_{ib}	25	32	ohms
Voltage Feedback Ratio (I_E = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz)		h_{rb}	-	500	X 10^{-6}
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)		h_{fe}	30	200	-
Output Admittance (I_E = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz)		h_{ob}	-	1.0	μmhos
MATCHING CHARACTERISTICS					
DC Current Gain Ratio** (I_C = 100 μAdc, V_{CE} = 5.0 Vdc)	2N2720 2N2721	h_{FE1}/h_{FE2}**	0.9 0.8	1.0 1.0	-
Base Voltage Differential (I_C = 100 μAdc, V_{CE} = 5.0 Vdc)	2N2720 2N2721	$\lvert V_{BE1}-V_{BE2}\rvert$	- -	5.0 10	mVdc
Base Voltage Differential Gradient (I_C = 100 μAdc, V_{CE} = 5.0 Vdc, T_A = -55 to +25°C) (I_C = 100 μAdc, V_{CE} = 5.0 Vdc, T_A = +25 to +125°C)	 2N2720 2N2721 2N2720 2N2721	$\Delta(V_{BE1}-V_{BE2})$	 - - - -	 0.8 1.6 1.0 2.0	mV

* Pulse Width = 12 ms, Duty Cycle = 2.0%.

** The lower of the two h_{FE} readings is taken as h_{FE1} for the purpose of measurement.

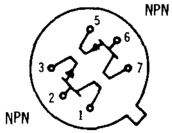
2N2722 (SILICON)

V_{CEO} = 45 V
I_C = 40 mA
P_D = 300 mW one side
600 mW both sides



CASE 32A

Dual NPN silicon transistor for small-signal, low-power differential amplifier applications.



Pin Connections Bottom View
All Leads Electrically Isolated from Case

MAXIMUM RATINGS (each side) (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value		Unit
Collector-Emitter Voltage	V_{CEO}	45		Vdc
Collector-Base Voltage	V_{CB}	45		Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	40		mAdc
Operating & Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C
		One Side	Both Sides	
Total Device Dissipation @ T_A = 25°C	P_D	0.3	0.6	Watt
Derate above 25°C		1.7	3.4	mW/°C
Total Device Dissipation @ T_C = 25°C	P_D	0.6	1.2	Watts
Derate above 25°C		3.4	6.8	mW/°C

2N2722 (continued)

ELECTRICAL CHARACTERISTICS (each side) (T_A = 25°C unless otherwise noted)

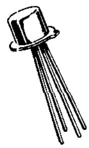
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage* (I_C = 10 mAdc, I_B = 0)	BV_{CEO}*	45	-	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BV_{CBO}	45	-	Vdc
Collector Cutoff Current (V_{CE} = 5.0 Vdc, I_B = 0)	I_{CEO}	-	2.0	nAdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_A = 150°C)	I_{CBO}	- -	0.001 1.0	μAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	-	1.0	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 1.0 μAdc, V_{CE} = 5.0 Vdc) (I_C = 10 μAdc, V_{CE} = 5.0 Vdc) (I_C = 0.1 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	50 100 125	250 - -	-
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 0.5 mAdc)	$V_{CE(sat)}$	-	1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 0.5 mAdc)	$V_{BE(sat)}$	0.65	0.85	Vdc
SMALL SIGNAL CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)	f_T	100	-	MHz
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	-	6.0	pF
Input Impedance (I_E = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz)	h_{ib}	25	32	ohms
Voltage Feedback Ratio (I_E = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz)	h_{rb}	-	600	X 10^{-6}
Small-Signal Current Gain (I_E = 0.1 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	h_{fe}	100	700	-
Output Admittance (I_E = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz)	h_{ob}	-	1.0	μmhos
Noise Figure (I_C = 10 μAdc, V_{CE} = 5.0 Vdc, R_G = 10 k ohms, f = 10 Hz to 15.7 kHz)	NF	-	4.0	dB
MATCHING CHARACTERISTICS				
DC Current Gain Ratio** (I_C = 1.0 μAdc, V_{CE} = 5.0 Vdc)	h_{FE1}/h_{FE2}**	0.9	1.0	-
Base Voltage Differential (I_C = 10 μAdc, V_{CE} = 5.0 Vdc)	$V_{BE1} - V_{BE2}$	-	5.0	mV
Base Voltage Differential Gradient (I_C = 10 μAdc, V_{CE} = 5.0 Vdc, T_A = -55 to +25°C) (I_C = 10 μAdc, V_{CE} = 5.0 Vdc, T_A = +25 to +125°C)	$\Delta(V_{BE1} - V_{BE2})$	- -	0.8 1.0	mV

* Pulse Width = 12 ms, Duty Cycle = 2.0%.

** The lower of the two h_{FE} readings is taken as h_{FE1} for the purpose of measurement.

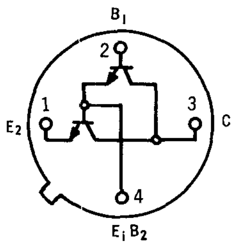
2N2723 thru 2N2725 (SILICON)

V_{CE2O} = 45 to 60 V
P_D = 500 mW
h_{FE} = to 50,000



CASE 20
(TO-72)

Two NPN silicon annular transistors connected as a darlington amplifier, and designed for applications requiring very high gain.



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	2N2723 2N2724	2N2725	Unit
Collector Emitter Voltage	V_{CE2O}	60	45	Vdc
Collector-Base Voltage	V_{CB1}	80	45	Vdc
Emitter-Base Voltage	V_{E2B1}	12	10	Vdc
Collector Current	I_C	40	30	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.5 2.9		Watt mW/°C
Total Device Dissipation @ T_C = 25°C T_C = 100°C Derate above 25°C	P_D	1.8 1.0 10.5		Watts Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

2N2723 thru 2N2725 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 10 mAdc, I_{B1} = 0)	2N2723, 2N2724 2N2725	BV_{CE2O}*	60 45	- -	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_{E2} = 0)	2N2723, 2N2724 2N2725	BV_{CB1O}	80 45	- -	Vdc
Emitter-Base Breakdown Voltage (I_{E2} = 10 μAdc, I_C = 0)	2N2723, 2N2724 2N2725	BV_{E2B1O}	12 10	- -	Vdc
Collector Cutoff Current (V_{CB1} = 60 Vdc, I_E = 0) (V_{CB1} = 60 Vdc, I_E = 0, T_A = 150°C) (V_{CB1} = 30 Vdc, I_E = 0) (V_{CB1} = 30 Vdc, I_E = 0, T_A = 150°C)	2N2723, 2N2724 2N2723, 2N2724 2N2725 2N2725	I_{CB1O}	- - - -	0.01 10 0.002 2.0	μAdc
Emitter Cutoff Current (V_{B1E2} = 10 Vdc, I_C = 0) (V_{B1E2} = 6.0 Vdc, I_C = 0)	2N2723, 2N2724 2N2725	I_{E2B1O}	- -	10 1.0	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 10 mAdc, V_{CE2} = 5.0 Vdc, I_{B2} = 0) (I_C = 100 μAdc, V_{CE2} = 5.0 Vdc, I_{B2} = 0)	2N2723 2N2724 2N2725	h_{FE}	2000 7000 2000	10,000 50,000 10,000	-
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_{B1} = 1.0 mAdc)	All Types	$V_{CE2(sat)}$	-	1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_{B1} = 1.0 mAdc)	All Types	$V_{BE2(sat)}$	-	1.7	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (Each Unit) (I_C = 10 mAdc, V_{CE1} or V_{CE2} = 10 Vdc, f = 20 MHz)	All Types	f_T	100	-	MHz
Output Capacitance (V_{CB1} = 10 Vdc, I_{E2} = 0, f = 140 kHz)	2N2723, 2N2724	C_{ob1}	-	10	pF
Small-Signal Current Gain (I_C = 10 mAdc, V_{CE2} = 5.0 Vdc, f = 1.0 kHz) (I_C = 10 μAdc, V_{CE2} = 5.0 Vdc, f = 1.0 kHz)	2N2723 2N2724 2N2725	h_{fe}	1500 5000 1500	15,000 60,000 15,000	-
Noise Figure (Input Stage Only) (I_C = 50 μAdc, V_{CE} = 5.0 Vdc, R_S = 3.0 k ohms, f = 1.0 kHz, BW = 100 kHz) (I_C = 10 μAdc, V_{CE} = 5.0 Vdc, R_S = 10 k ohms, f = 1.0 kHz, BW = 100 kHz) (I_C = 3.0 μAdr, V_{CE} = 5.0 Vdc, R_S = 30 k ohms, f = 1.0 kHz, BW = 100 kHz)	2N2723 2N2724 2N2725	NF	- - -	10 6.0 6.0	dB

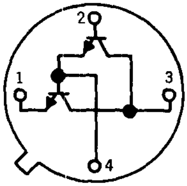
* Pulse Test: Pulse Width = 12 ms, Duty Cycle = 2.0 %.

2N2785 (SILICON)

V_{CE2O} = 40 V
P_D = 500 mW
h_{FE} — to 20,000

CASE 20
(TO-72)

Two NPN silicon annular transistors connected as a darlington amplifier, and designed for applications requiring very high gain.



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CE2O}	40	Vdc
Collector-Base Voltage	V_{CB1}	60	Vdc
Emitter-Base Voltage (Pin 4 to Pin 2)	V_{E2B1}	15 7.5	Vdc Vdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	0.5 3.33	Watt mW/°C
Total Device Dissipation @ T_C = 25°C T_C = 100°C Derate above 25°C	P_D	1.8 1.0 10	Watts Watt mW/°C
Operating Junction Temperature Range	T_J	-65 to +175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

2N2785 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

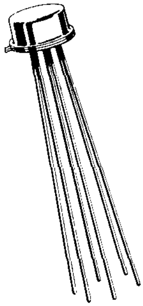
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage* (I_C = 20 mAdc, I_{B1} = 0)	BV_{CE2O}*	40	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 µAdc, I_{E2} = 0)	BV_{CB1O}	60	-	Vdc
Emitter-Base Breakdown Voltage (I_{E2} = 100 µAdc, I_C = 0)	BV_{E2B1O}	15	-	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0)	I_{CEO}	-	500	nAdc
Collector Cutoff Current (V_{CB1} = 30 Vdc, I_E = 0) (V_{CB1} = 30 Vdc, I_E = 0, T_A = 150°C)	I_{CB1O}	- -	0.05 10	µAdc
Emitter Cutoff Current (V_{E2B1} = 5.0 Vdc, I_C = 0)	I_{E2B1O}	-	20	nAdc
ON CHARACTERISTICS				
DC Current Gain* (I_C = 1.0 mAdc, V_{CE2} = 4.0 Vdc) (I_C = 10 mAdc, V_{CE2} = 5.0 Vdc) (I_C = 100 mAdc, V_{CE2} = 5.0 Vdc)	h_{FE}*	600 1200 2000	- - 20,000	-
Collector-Emitter Saturation Voltage (I_C = 15 mAdc, I_{B1} = 3.0 mAdc)	$V_{CE2(sat)}$	-	1.0	Vdc
SMALL SIGNAL CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 1.0 mAdc, V_{CE2} = 5.0 Vdc, f = 10 MHz)	f_T	10	-	MHz
Output Capacitance (V_{CB1} = 10 Vdc, I_{E2} = 0, f = 1.0 MHz)	C_{ob1}	-	30	pF
Input Impedance (I_C = 1.0 mAdc, V_{CB1} = 5.0 Vdc, f = 1.0 kHz)	h_{ib}	30	80	Ohm
Voltage Feedback Ratio (I_C = 1.0 mAdc, V_{CE2} = 5.0 Vdc, f = 1.0 kHz)	h_{rb}	-	10	x 10^{-4}
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE2} = 5.0 Vdc, f = 1.0 kHz)	h_{fe}	600	-	-
Output Admittance (I_C = 1.0 mAdc, V_{CB1} = 5.0 Vdc, f = 1.0 kHz)	h_{ob}	-	0.5	µmhos

* Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

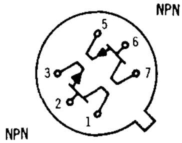
2N3423 (SILICON)
2N3424

V_{CEO} = 15 V
I_C = 50 mA
P_D = 300 mW one side
450 mW both sides

Dual NPN silicon transistors designed for use as sense and high-frequency differential amplifiers.



CASE 32A



Pin Connections Bottom View
All Leads Electrically Isolated from Case

MAXIMUM RATINGS (each side) (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value		Unit
Collector-Emitter Voltage	V_{CEO}	15		Vdc
Collector-Base Voltage	V_{CB}	30		Vdc
Emitter-Base Voltage	V_{EB}	3.0		Vdc
Collector Current	I_C	50		mAdc
Operating & Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C
		One Side	Both Sides	
Total Device Dissipation @ T_A = 25°C	P_D	0.3	0.45	Watt
Derate above 25°C		1.72	2.57	mW/°C
Total Device Dissipation @ T_C = 100°C	P_D	0.344	0.685	Watt
T_C = 25°C		0.6	1.2	Watt
Derate above 25°C		3.44	6.85	mW/°C

2N3423, 2N3424 (continued)

ELECTRICAL CHARACTERISTICS (each side) (T_A = 25°C unless otherwise noted)

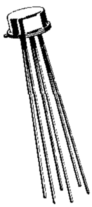
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage* (I_C = 3.0 mAdc, I_B = 0)	$BV_{CEO(sus)}$*	15	-	Vdc
Collector-Base Breakdown Voltage (I_C = 1.0 μAdc, I_E = 0)	BV_{CBO}	30	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	3.0	-	Vdc
Collector Cutoff Current (V_{CB} = 15 Vdc, I_E = 0)	I_{CBO}	-	0.01	μAdc
(V_{CB} = 15 Vdc, I_E = 0, T_A = 150°C)		-	1.0	
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	-	10	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 3.0 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	20	-	-
(I_C = 3.0 mAdc, V_{CE} = 3.0 Vdc)		20	200	
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	-	0.4	Vdc
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$	-	1.0	Vdc
SMALL SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 4.0 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	600	1200	MHz
Output Capacitance (V_{CB} = 0, I_E = 0, f = 140 kHz)	C_{ob}	-	3.0	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 140 kHz)		-	1.7	
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 140 kHz)	C_{ib}	-	2.0	pF
Real Part of Input Impedance (I_C = 3.0 mAdc, V_{CE} = 3.0 Vdc, f = 350 MHz)	$Re(h_{ie})$	-	45	Ohm
MATCHING CHARACTERISTICS				
DC Current Gain Ratio** (I_C = 3.0 mAdc, V_{CE} = 3.0 Vdc) 2N3423	h_{FE1}/h_{FE2}**	0.8	1.0	--
2N3424		0.9	1.0	
Base Voltage Differential (I_C = 3.0 mAdc, V_{CE} = 3.0 Vdc) 2N3423	$\|V_{BE1}-V_{BE2}\|$	-	10	mVdc
2N3424		-	5.0	
Base Voltage Differential Gradient (I_C = 3.0 mAdc, V_{CE} = 3.0 Vdc, T_{A1} = 25°C, T_{A2} = -55°C) 2N3423	$\Delta(V_{BE1}-V_{BE2})$	-	3.2	mVdc
2N3424		-	1.6	
(I_C = 3.0 mAdc, V_{CE} = 3.0 Vdc, T_{A1} = 25°C, T_{A2} = 125°C) 2N3423		-	4.0	
2N3424		-	2.0	

* Pulse Width = 300 μs; Duty Cycle = 1%

** Lowest of the two h_{FE} readings is taken as h_{FE1} for purposes of this ratio.

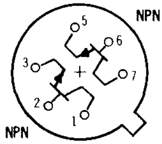
2N3425 (SILICON)

V_{CEO} = 15 V
P_D = 300 mW one side
400 mW both sides



CASE 32A

Dual NPN silicon transistor designed for use as a high-frequency sense amplifier.

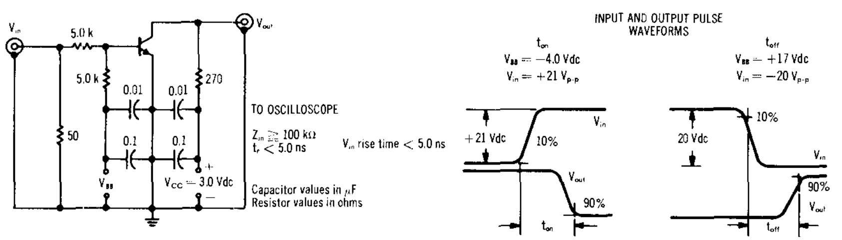


Pin Connections Bottom View
All Leads Electrically Isolated from Case

MAXIMUM RATINGS (each side) (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value		Unit
Collector-Emitter Voltage	V_{CEO}	15		Vdc
Collector-Emitter Voltage (R_{BE} ≦ 10 ohms)	V_{CER}	20		Vdc
Collector-Base Voltage	V_{CB}	40		Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Operating Junction Temperature Range	T_J	+200		°C
Storage Temperature Range	T_{stg}	-65 to +200		°C
		One Side	Both Sides	
Total Device Dissipation @ T_A = 25°C	P_D	0.3	0.4	Watt
Derate above 25°C		1.72	2.28	mW/°C
Total Device Dissipation @ T_C = 25°C	P_D	0.75	1.5	Watt
T_C = 100°C		0.43	0.86	Watt
Derate above 25°C		4.3	8.55	mW/°C

FIGURE 1 — SWITCHING TIME TEST CIRCUIT



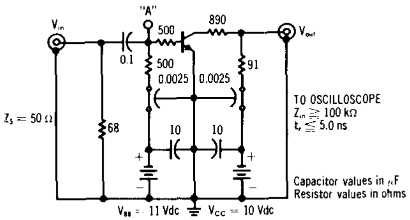
2N3425 (continued)

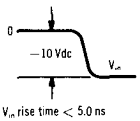
ELECTRICAL CHARACTERISTICS (each side) (T_A = 25°C unless otherwise noted)

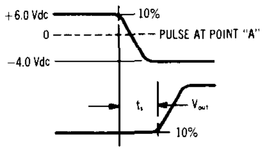
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage* (I_C = 10 mAdc, I_B = 0)	$BV_{CEO(sus)}$*	15	-	Vdc
Collector-Emitter Sustaining Voltage* (I_C = 30 mAdc, R_{BE} ≤ 10 ohms)	$BV_{CER(sus)}$*	20	-	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BV_{CBO}	40	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 uAdc, I_C = 0)	BV_{EBO}	5.0	-	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, $V_{EB(off)}$ = 0.25 Vdc, T_A = 125°C)	I_{CEX}	-	15	μAdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	-	0.025	μAdc
(V_{CB} = 20 Vdc, I_E = 0, T_A = 150°C)		-	15	
Emitter Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	-	0.2	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 0.5 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	12	-	-
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)		30	120	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc, T_A = -55°C)		12	-	
Collector-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	-	0.4	Vdc
(I_C = 7.0 mAdc, I_B = 0.7 mAdc, T_A = -55°C to +125°C)		-	0.5	
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$	0.7	0.85	Vdc
(I_C = 7.0 mAdc, I_B = 0.7 mAdc, T_A = -55°C)		-	0.9	
DYNAMIC CHARACTERISTICS				
Current-Gain — Bandwidth Product (I_C = 20 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	300	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 140 kHz)	C_{ob}	-	6.0	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 140 kHz)	C_{ib}	-	9.0	pF
Small-Signal Current Gain (I_C = 10 mAdc, V_{CE} = 1.0 Vdc, f = 1.0 kHz)	h_{fe}	20	-	-
Real Part of Input Impedance (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 300 MHz)	$Re(h_{ie})$	-	50	Ohms
Turn-On Time (Figure 1) (V_{CC} = 3.0 Vdc, $V_{EB(off)}$ = 2.0 Vdc, I_C ≈ 10 mAdc, I_{B1} ≈ 3.0 mAdc)	t_{on}	-	50	ns
Turn-Off Time (Figure 1) (V_{CC} = 3.0 Vdc, I_C ≈ 10 mAdc, I_{B1} ≈ 3.0 mAdc, I_{B2} ≈ 1.0 mAdc)	t_{off}	-	90	ns
Storage Time (Figure 2) (I_C ≈ 10 mAdc, I_{B1} ≈ 10 mAdc, I_{B2} ≈ 10 mAdc)	t_s	-	40	ns

* Pulse conditions: Pulse width = 300 μs; duty cycle = 1%

FIGURE 2 — STORAGE TIME TEST CIRCUIT

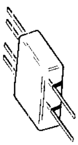






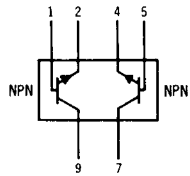
2N3515 (SILICON)
2N3518

V_{CEO} = 40 – 60 V
I_C = 500 mA
P_D = 250 mW one side
350 mW both sides



CASE 33
(TO-89)

Dual NPN silicon transistor for use as a differential amplifier.



Pin Connections,
Bottom View

MAXIMUM RATINGS (each side) (T_A = 25°C)

Rating	Symbol	2N3515	2N3518	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0	7.0	Vdc
Collector Current	I_C	500		mAdc
Operating Junction Temperature Range	T_J	-65 to +175		°C
Storage Temperature Range	T_{stg}	-65 to +200		°C
		One Side	Both Sides	
Total Device Dissipation @T_A = 25°C Derate above 25°C	P_D	250 1.67	350 2.33	mW mW/°C
Total Device Dissipation @T_C = 25°C Derate above 25°C	P_D	700 4.67	1,400 9.33	mW mW/°C

2N3515, 2N3518 (continued)

ELECTRICAL CHARACTERISTICS (each side) (T_A = 25°C unless otherwise noted)

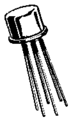
Characteristics		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 20 mAdc, I_B = 0)	 2N3515 2N3518	BV_{CEO}*	 40 60	 - -	Vdc
Collector-Base Breakdown Voltage (I_C = 50 nAdc, I_E = 0) (I_C = 100 μAdc, I_E = 0)	 2N3515 2N3518	BV_{CBO}	 80 100	 - -	Vdc
Emitter-Base Breakdown Voltage (I_E = 50 nAdc, I_C = 0) (I_E = 100 μAdc, I_C = 0)	 2N3515 2N3518	BV_{EBO}	 5.0 7.0	 - -	Vdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_A = 150°C) (V_{CB} = 50 Vdc, I_E = 0) (V_{CB} = 50 Vdc, I_E = 0, T_A = 150°C)	 2N3515 2N3515 2N3518 2N3518	I_{CBO}	 - - -	 0.02 15 0.002 10	μAdc
Emitter-Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	 2N3515 2N3518	I_{EBO}	 - -	 20 2.0	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 μAdc, V_{CE} = 5.0 Vdc) (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc) (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, T_A = -55°C)	 2N3518	h_{FE}	 35 50 15	 - 200 -	-
Collector-Emitter Saturatinn Voltage (I_C = 50 mAdc, I_B = 5.0 mAdc)		$V_{CE(sat)}$	-	1.2	Vdc
Base-Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 5.0 mAdc)		$V_{BE(sat)}$	-	0.9	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)	 2N3515 2N3518	f_T	 50 60	 - -	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	 2N3515 2N3518	C_{ob}	 - -	 18 15	pF
Input Capacitance (V_{BE} = 0, 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ib}	-	85	pF
Input Impedance (I_C = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz)		h_{ib}	20	35	ohms
Input Impedance (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	 2N3515 2N3518	h_{ie}	 1.0 1.0	 5.0 10.5	k ohms
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)		h_{fe}	50	300	-
Output Admittance (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	 2N3515 2N3518	h_{oe}	 4.0 4.0	 16 50	μmhos
Noise Figure (I_C = 0.3 mAdc, V_{CE} = 10 Vdc, R_G = 510 ohms, B. W. = 1.0 Hz, f = 1.0 kHz)		NF	-	8.0	dB
MATCHING CHARACTERISTICS					
DC Current Gain Ratio** (I_C = 100 μAdc, V_{CE} = 5.0 Vdc) (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc)	 2N3515 2N3518 2N3515 2N3516	h_{FE1}/h_{FE2}**	 0.8 0.9 0.8 0.9	 1.0 1.0 1.0 1.0	-
Base Voltage Differential (I_C = 100 μAdc, V_{CE} = 5.0 Vdc) (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc)	 2N3515 2N3518 2N3515 2N3518	$\lvert V_{BE1} - V_{BE2} \rvert$	 - - - -	 5.0 3.0 5.0 3.0	mVdc
Base Voltage Differential Gradient (I_C = 100 μAdc, V_{CE} = 5.0 Vdc, T_A = -55 to +125°C)	 2N3515 2N3518	$\frac{\Delta \lvert V_{BE1} - V_{BE2} \rvert}{\Delta T_A}$	 - -	 15 10	μV/°C

* Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

** The lowest of the two h_{FE} readings is taken as h_{FE1} for the purpose of measurement.

2N3800 thru 2N3817 (SILICON)
(JAN 2N3810 AND 2N3811 Available)

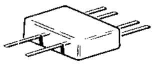
V_{CEO} = 60 V
I_C = 50 mA
P_D to 500 mW one side
600 mW both sides



Dual PNP silicon annular transistors specifically designed for differential amplifier applications.

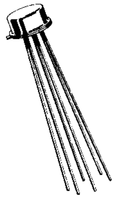
CASE 35
(TO-71)

2N3800 thru 2N3805



CASE 33
(TO-89)

2N3812 thru 2N3817



CASE 32

2N3806 thru 2N3811

MAXIMUM RATINGS (each side)

Rating	Symbol	Value		Unit
Collector-Emitter Voltage	V_{CEO}	60		Vdc
Collector-Base Voltage	V_{CB}	60		Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	50		mAdc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C
		One Side	Both Sides	
Total Device Dissipation @ T_A = 25°C	P_D			
Metal Can (2N3800 thru 2N3805)		250	360	mW
Derate above 25°C		1.5	2.06	mW/°C
Metal Can (2N3806 thru 2N3811)		500	600	mW
Derate above 25°C		2.9	3.4	mW/°C
Flat Package (2N3812 thru 2N3817)		250	350	mW
Derate above 25°C		1.5	2.0	mW/°C

2N3800 thru 2N3817 (continued)

ELECTRICAL CHARACTERISTICS (each side) (T_A = 25°C unless otherwise noted)
Characteristics apply also to corresponding flat package type numbers

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage* (I_C = 18 mAdc, I_B = 0)	BV_{CEO}*	60	90	—	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 8)	BV_{CBO}	60	—	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 18 μAdc, I_C = 0)	BV_{EBO}	5.0	—	—	Vdc
Colleclor Cutoff Current (V_{CB} = 50 Vdc, I_E = 8) (V_{CB} = 50 Vdc, I_E = 8, T_A = 150°C)	I_{CBO}	 — —	 — —	 0.81 18	μAdc
Emitter Cutoff Current ($V_{BE(off)}$ = 4.8 Vdc, I_C = 8)	I_{EBO}	—	—	20	nAdc
ON CHARACTERISTICS					
DC Current Gain*	h_{FE}*				—
(I_C = 1.0 μAdc, V_{CE} = 5.8 Vdc) 2N3881, 3, 5, 7, 9, 11, 13, 15, 17		75	—	—	
(I_C = 10 μAdc, V_{CE} = 5.8 Vdc) 2N3800, 2, 4, 6, 6, 19, 12, 14, 16 2N3801, 3, 5, 7, 9, 11, 13, 15, 17		190 225	— —	— —	
(I_C = 109 μAdc, V_{CE} = 5.8 Vdc) 2N3806, 2, 4, 6, 8, 19, 12, 14, 16 2N3801, 3, 5, 7, 8, 11, 13, 15, 17		150 300	— —	450 906	
(I_C = 180 μAdc, V_{CE} = 5.8 Vdc, T_A = -55°C) 2N3600, 2, 4, 6, 8, 18, 12, 14, 16 2N3801, 3, 5, 7, 9, 11, 13, 15, 17		75 158	— —	— —	
(I_C = 500 μAdc, V_{CE} = 5.0 Vdc) 2N3680, 2, 4, 6, 6, 18, 12, 14, 16 2N3801, 3, 5, 7, 8, 11, 13, 15, 17		158 309	— —	450 900	
(I_C = 1.6 mAdc, V_{CE} = 5.9 Vdc) 2N3880, 2, 4, 6, 8, 18, 12, 14, 16 2N3801, 3, 5, 7, 9, 11, 13, 15, 17		150 300	— —	458 000	
(I_C = 10 mAdc, V_{CE} = 5.8 Vdc) 2N3990, 2, 4, 6, 6, 18, 12, 14, 16 2N3881, 3, 5, 7, 9, 11, 13, 15, 17		125 250	— —	— —	
Collector-Emitter Saturation Voltage* (I_C = 100 μAdc, I_B = 18 μAdc) (I_C = 1.0 mAdc, I_B = 100 μAdc)	$V_{CE(sat)}$*	 — —	 — —	 9.2 8.25	Vdc
Base-Emitter Saturation Voltage* (I_C = 190 μAdc, I_B = 18 μAdc) (I_C = 1.0 mAdc, I_B = 100 μAdc)	$V_{BE(sat)}$*	 — —	 — —	 8.7 8.8	Vdc
Base-Emitter On Voltage (I_C = 100 μAdc, V_{CE} = 5.9 Vdc)	$V_{BE(on)}$	—	—	9.7	Vdc
SMALL SIGNAL CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 508 μAdc, V_{CE} = 5.0 Vdc, f = 38 MHz) (I_C = 1.8 mAdc, V_{CE} = 5.0 Vdc, f = 188 MHz)	f_T	 30 100	 — —	 — 500	MHz
Output Capacitance (V_{CB} = 5.8 Vdc, I_E = 0, f = 180 kHz)	C_{ob}	—	—	4.8	pF
Input Capacilance ($V_{BE(off)}$ = 8.5 Vdc, I_C = 8, f = 109 kHz)	C_{ib}	—	—	6.0	pF
Input Impedance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.9 kHz) 2N3908, 2, 4, 6, 9, 10, 12, 14, 16 2N3861, 3, 5, 7, 9, 11, 13, 15, 17	h_{ie}	3.0 19	— —	15 40	kΩ
Voltage Feedback Ratio (I_C = 1.8 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{re}	—	—	25	X 19^{-4}
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 19 Vdc, f = 1.0 kHz) 2N3808, 2, 4, 6, 8, 10, 12, 14, 16 2N3801, 3, 5, 7, 9, 11, 13, 15, 17	h_{fe}	150 306	— —	600 900	—
Output Admittance (I_C = 1.0 mAdc, V_{CE} = 19 Vdc, f = 1.9 kHz)	h_{oe}	5.0	—	80	μmhos
Noise Figure (I_C = 190 μAdc, V_{CE} = 19 Vdc, R_S = 3.0 kΩ,	NF				dB
f = 109 Hz) 2N3808, 2, 4, 6, 8, 10, 12, 14, 16 2N3801, 3, 5, 7, 9, 11, 13, 15, 17		— —	4.0 2.5	7.0 4.0	
f = 1.0 kHz) 2N3909, 2, 4, 6, 8, 10, 12, 14, 16 2N3801, 3, 5, 7, 8, 11, 13, 15, 17		— —	1.5 0.8	3.9 1.5	
f = 10 kHz) 2N3800, 2, 4, 6, 6, 10, 12, 14, 18 2N3801, 3, 5, 7, 9, 11, 13, 15, 17		— —	1.0 6.8	2.5 1.5	
Noise Bandwidth = 10 Hz to 15.7 kHz) 2N3800, 2, 4, 8, 8, 10, 12, 14, 18 2N3601, 3, 5, 7, 9, 11, 13, 15, 17		— —	2.5 1.5	3.5 2.5	
MATCHING CHARACTERISTICS					
DC Current Gain Ratio** (I_C = 108 μAdr, V_{CE} = 5.9 Vdc) 2N3802, 3, 8, 9, 14, 15 2N3804, 5, 18, 11, 16, 17	h_{FE1}/h_{FE2}**	0.8 0.9	— —	1.9 1.8	—
Base Vnltage Differential (I_C = 10 μAdc, to 18 mAdc, V_{CE} = 5.0 Vdc) 2N3802, 3, 8, 9, 14, 15 2N3884, 5, 10, 11, 16, 17	$\lvert V_{BE1}-V_{BE2}\rvert$	— —	— —	8.0 5.0	mVdc
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc) 2N3902, 3, 9, 8, 14, 15 2N3604, 5, 10, 11, 16, 17		— —	— —	5.9 3.9	
Base Voltage Differential Gradient (I_C = 109 μAdc, V_{CE} = 5.0 Vdc, T_A = -55 to +25°C) 2N3802, 3, 8, 9, 14, 15 2N3804, 5, 10, 11, 18, 17	$\frac{\Delta\lvert V_{BE1}-V_{BE2}\rvert}{\Delta T_A}$	— —	— —	1.8 8.8	mVdc
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc, T_A = +25 to +125°C) 2N3802, 3, 8, 9, 14, 15 2N3804, 5, 10, 11, 18, 17		— —	— —	2.8 1.8	

*Pulse Test: Pulse width ≤309 μs, duty cycle ≤2% **The lowest h_{FE} reading is taken as h_{FE1} for this ratio.

2N3800 thru 2N3817 (continued)

SMALL-SIGNAL CHARACTERISTICS

NDISE FIGURE

FIGURE 1 – FREQUENCY EFFECTS

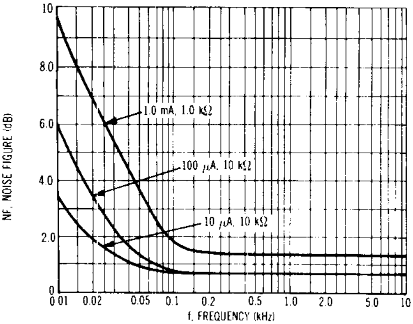
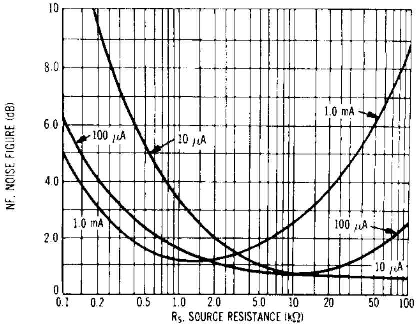


FIGURE 2 – SOURCE RESISTANCE EFFECTS



h PARAMETERS

V_{CE} = 10 Vdc, f = 1 kHz, T_A = 25°C

FIGURE 3 – INPUT IMPEDANCE

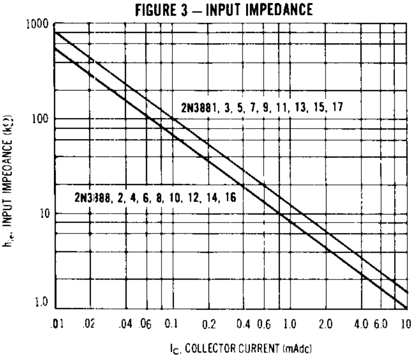


FIGURE 4 – VDLTAGE FEEDBACK RATID

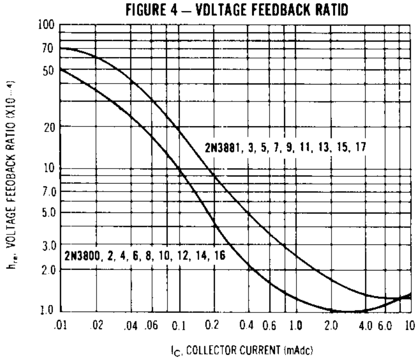


FIGURE 5 – CURRENT GAIN

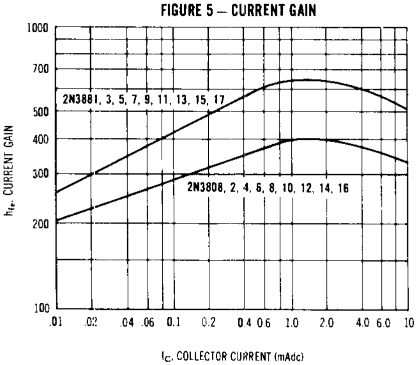
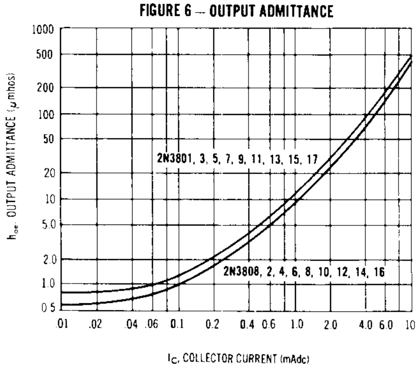


FIGURE 6 – OUTPUT ADMITTANCE



2N3838 (continued)

ELECTRICAL CHARACTERISTICS (each side) (T_A = 25°C unless otherwise noted)

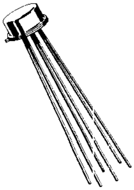
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage* (I_C = 10 mAdc, I_B = 0)	BV_{CEO}*	40	-	Vdc
Collector-Emitter Nonlatching Voltage (Figure 3) ($I_{C(on)}$ = 600 mAdc, $I_{B(on)}$ = 120 mAdc, $I_{B(off)}$ = 0)	$V_{CEO(NL)}$†	40	-	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BV_{CBO}	60	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0	-	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, $V_{BE(off)}$ = 0.5 Vdc)	I_{CEV}	-	0.01	μAdc
(V_{CE} = 50 Vdc, $V_{BE(off)}$ = 0.5 Vdc, T_A = 150°C)		-	10	
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}	-	10	nAdc
Base Cutoff Current (V_{CE} = 50 Vdc, $V_{BE(off)}$ = 0.5 Vdc)	I_{BEV}	-	10	nAdc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			-
(I_C = 0.1 mAdc, V_{CE} = 10 Vdc)		35	-	
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)		50	-	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)*		75	-	
(I_C = 150 mAdc, V_{CE} = 10 Vdc)*		100	300	
(I_C = 150 mAdc, V_{CE} = 1.0 Vdc)*		50	-	
Collector-Emitter Saturation Voltage* (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{CE(sat)}$*	-	0.4	Vdc
Base-Emitter Saturation Voltage* (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{BE(sat)}$*	0.85	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 20 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	200	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 140 kHz)	C_{ob}	-	8.0	pF
Input Impedance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{ie}	1.5	9.0	k ohm
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	60	300	-
Output Admittance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{oe}	-	50	μmho
Noise Figure (I_C = 100 μAdc, V_{CE} = 10 Vdc, R_S = 1.0 k ohm, f = 1.0 kHz)	NF	-	8.0	dB
Delay Time (V_{CC} = 10 Vdc, $V_{BE(off)}$ = 0 Vdc, I_C = 150 mAdc, I_{B1} = 15 mAdc, Figure 1)	t_d	-	10	ns
Rise Time (V_{CC} = 10 Vdc, $V_{BE(off)}$ = 0 Vdc, I_C = 150 mAdc, I_{B1} = 15 mAdc, Figure 1)	t_r	-	40	ns
Storage Time (V_{CC} = 10 Vdc, I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc, Figure 2)	t_s	-	250	ns
Fall Time (V_{CC} = 10 Vdc, I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc, Figure 2)	t_f	-	90	ns

* Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

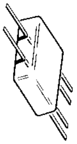
† The highest value of collector supply voltage that may be safely used with a resistive load switching circuit in which the collector current is 600 mAdc.

2N4937 thru 2N4942

V_{CEO} = 40 V
I_C = 50 mA
P_D = 500 mW one side
600 mW both sides

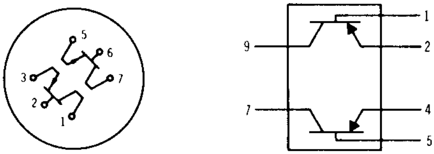


CASE 32



CASE 33
(TO-89)

Dual PNP silicon annular transistors especially designed for low-level, differential amplifier applications.



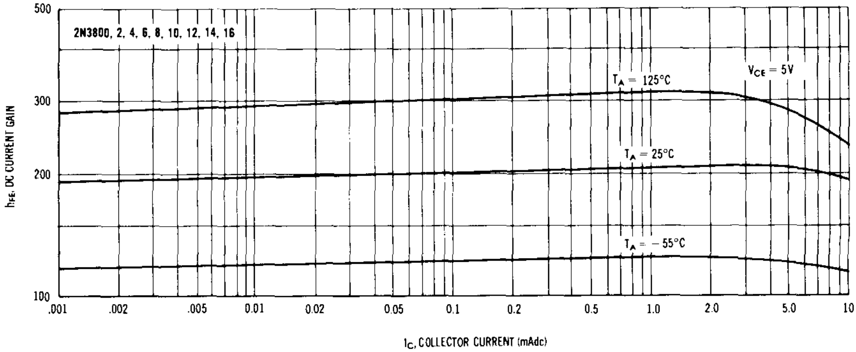
Pin Connections, Bottom View
All Leads Electrically Isolated from Case

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value		Unit
Collector-Emitter Voltage	V_{CEO}	40		Vdc
Collector-Base Voltage	V_{CB}	50		Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current - Continuous	I_C	50		mAdc
Base Current	I_B	10		mAdc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C
		One Side	Both Sides	
Total Device Dissipation @ T_A = 25°C	P_D			
Metal Can		500	600	mW
Derate above 25°C		2.9	3.4	mW/°C
Flat Pack		250	350	mW
Derate above 25°C		1.5	2.0	mW/°C

2N3800 thru 2N3817 (continued)

FIGURE 7 – TYPICAL CURRENT-GAIN CHARACTERISTICS



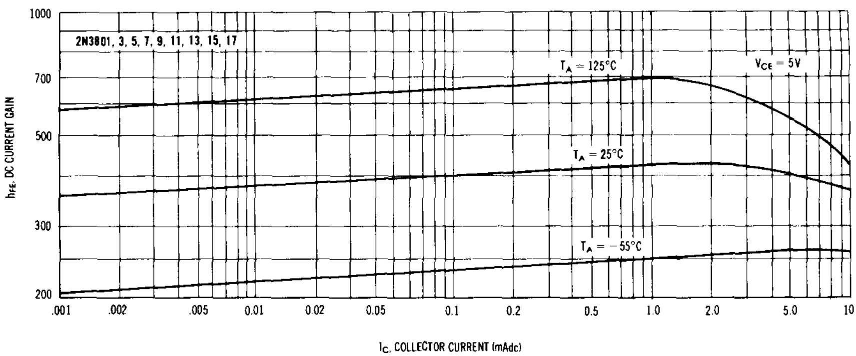
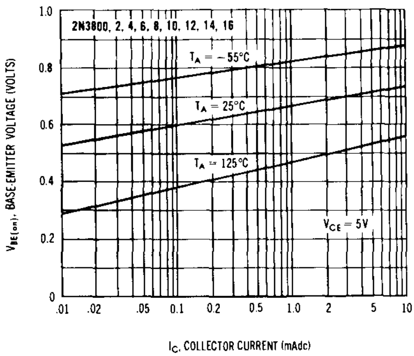
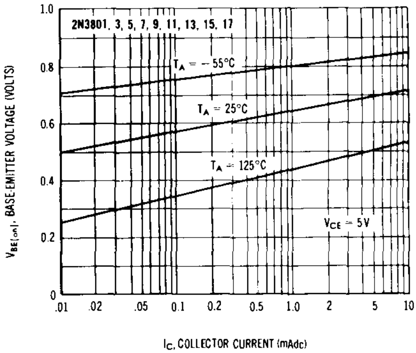
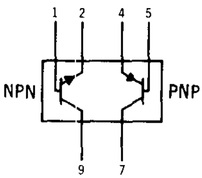


FIGURE 8 – BASE-EMITTER "ON" VOLTAGE versus TEMPERATURE

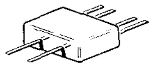




2N3838 (SILICON)



Pin Connections, Bottom View



CASE 33
(TO-89)

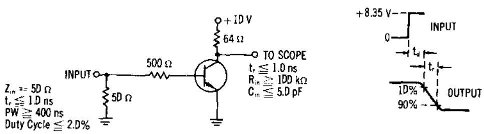
V_{CEO} = 40 V
I_C = 600 mA
P_D = 250 mW one side
350 mW both sides

NPN-PNP complementary-pair silicon annular transistor designed for switching and general purpose amplifier applications.

MAXIMUM RATINGS (each side) (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value		Unit
Collector-Emitter Voltage (Applicable from 0 to 10 mAdc)	V_{CEO}	40		Vdc
Collector-Base Voltage	V_{CB}	60		Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	600		mAdc
Operating Junction Temperature Range	T_J	-65 to +175		°C
Storage Temperature Range	T_{stg}	-65 to +200		°C
		One Side	Both Sides	
Total Device Dissipation @ T_A = 25°C	P_D	0.25	0.35	Watt
Derate above 25°C		1.67	2.34	mW/°C
Total Device Dissipation @ T_C = 25°C	P_D	0.7	1.4	Watt
Derate above 25°C		4.67	9.34	mW/°C

FIGURE 1 — TURN-ON TIME TEST CIRCUIT



(Reverse voltage polarities when testing the PNP unit.)

FIGURE 2 — TURN-OFF TIME TEST CIRCUIT

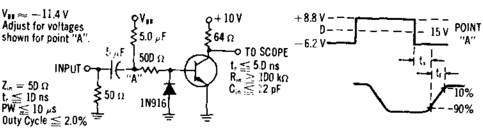
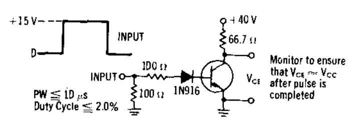


FIGURE 3 — COLLECTOR-EMITTER NONLATCHING VOLTAGE TEST CIRCUIT



2N4937 thru 2N4942 (continued)

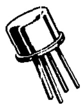
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	BV_{CEO}	40	45	-	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	BV_{CBO}	50	70	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0	5.6	-	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	I_{CBO}	-	2.0	20	nAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}	-	3.0	20	nAdc
ON CHARACTERISTICS					
DC Current Gain	h_{FE}				-
(I_C = 100 μAdc, V_{CE} = 10 Vdc)		40	-	200	
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)		50	-	250	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)		50	-	250	
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain-Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	f_T	300	400	900	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 140 kHz) Emitter Guarded	C_{cb}	-	3.0	5.0	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 140 kHz) Collector Guarded	C_{eb}	-	7.0	10	pF
Input Impedance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1 kHz)	h_{ie}	1.0	4.0	10	kΩ
Voltage Feedback Ratio (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1 kHz)	h_{re}	-	3.0	10	$X 10^{-4}$
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1 kHz)	h_{fe}	50	-	-	-
Output Admittance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1 kHz)	h_{oe}	5.0	15	50	μmhos
Noise Figure (I_C = 100 μAdc, V_{CE} = 10 Vdc, R_S = 3.0 kΩ, f = 10 Hz to 15.7 kHz)	NF	-	-	4.0	dB
MATCHING CHARACTERISTICS					
DC Current Gain Ratio (I_C = 100 μAdc to 1.0 mAdc, V_{CE} = 10 Vdc) 2N4937, 2N4940	h_{FE1}/h_{FE2}*	0.9	-	1.0	-
2N4938, 2N4941		0.8	-	1.0	
2N4939, 2N4942		-	0.7	-	
(I_C = 100 μAdc to 1.0 mAdc, V_{CE} = 10 Vdc, T_A = -55°C to +125°C) 2N4937, 2N4940		0.85	-	1.0	
2N4938, 2N4941		0.7	-	1.0	
2N4939, 2N4942		-	0.6	-	
Base Voltage Differential (I_C = 100 μA to 1.0 mAdc, V_{CE} = 10 Vdc) 2N4937, 2N4940	$V_{BE1}-V_{BE2}$	-	-	3.0	mVdc
2N4938, 2N4941		-	-	5.0	
2N4939, 2N4942		-	5.0	-	
Base Voltage Differential Gradient (I_C = 100 μAdc to 1.0 mAdc, V_{CE} = 10 Vdc, T_A = -55°C to +125°C) 2N4937, 2N4940	$\frac{\Delta V_{BE1}-V_{BE2}}{\Delta T_A}$	-	-	10	μV/°C
2N4938, 2N4941		-	-	20	
2N4939, 2N4942		-	20	-	

* The lowest h_{FE} reading is taken as h_{FE1} for this ratio

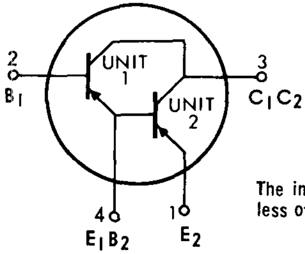
2N4974 (SILICON)
2N4975

$V_{CE2} = 30$ V
$I_C = 1.0$ A
$P_D = 0.8$ W



CASE 34A
(TO-12)

PNP silicon annular darlington amplifiers contain two PNP silicon annular transistors connected as a darlington amplifier.



The input unit is identified as Unit 1 regardless of terminal numbering.

MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Numerical subscripts refer to unit number

Rating	Symbol	Value	Unit
Collector-Emitter Voltage (Base 1 and Base 2 open)	V_{CE2}	30	Vdc
Collector-Base Voltage	V_{CB1}	40	Vdc
Emitter-Base Voltage	V_{E2B1}	10	Vdc
Collector Current — Continuous	I_C	1.0	Adc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	0.8 4.57	Watt mW/°C
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	2.5 14.3	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Unit
Thermal Resistance, Junction to Case Output Device Driver Device	θ_{JC}	 60 85	°C/W
Thermal Resistance, Junction to Junction	-	30	°C/W

2N4974, 2N4975 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

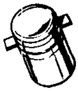
Numerical subscripts refer to unit number, lead 4 open unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage * (I_C = 10 mAdc, E_2B_1 termination open)	BV_{CE2}*	30	40	-	Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc)	BV_{CB1O}	40	50	-	Vdc
Emitter-Base Breakdown Voltage (I_{B1} = 10 μAdc)	BV_{E2B1O}	10	12.5	-	Vdc
Collector Cutoff Current (V_{CB1} = 30 Vdc)	I_{CB1O}	-	0.5	10	nAdc
Emitter Cutoff Current (V_{E2B1} = 5.0 Vdc)	I_{E2B1O}	-	0.15	10	nAdc
ON CHARACTERISTICS					
DC Current Gain	h_{FE}				-
(I_C = 1.0 μAdc, V_{CE2} = 5.0 Vdc) 2N4974		5,000	9,000	-	
2N4975		1,000	4,000	-	
(I_C = 1.0 μAdc, V_{CE2} = 5.0 Vdc, T_A = -55°C) 2N4974		-	2,000	-	
2N4975		-	1,000	-	
(I_C = 10 μAdc, V_{CE2} = 5.0 Vdc) 2N4974		10,000	15,000	-	
2N4975		5,000	9,000		
(I_C = 10 μAdc, V_{CE2} = 5.0 Vdc, T_A = -55°C) 2N4974		-	3,500	-	
2N4975		-	2,000	-	
(I_C = 100 μAdc, V_{CE2} = 5.0 Vdc) 2N4974		20,000	30,000	-	
2N4975		10,000	20,000	-	
(I_C = 1.0 mAdc, V_{CE2} = 5.0 Vdc) 2N4974		25,000	50,000	-	
2N4975		15,000	30,000		
(I_C = 10 mAdc, V_{CE2} = 5.0 Vdc)* 2N4974		30,000	60,000	150,000	
2N4975		15,000	30,000	75,000	
(I_C = 10 mAdc, V_{CE2} = 5.0 Vdc, T_A = -55°C)* 2N4974		-	15,000	-	
2N4975		-	10,000	-	
(I_C = 100 mAdc, V_{CE2} = 5.0 Vdc)* 2N4974		25,000	50,000	-	
2N4975		15,000	30,000	-	
(I_C = 500 mAdc, V_{CE2} = 5.0 Vdc)* 2N4974		15,000	25,000	-	
2N4975		5,000	10,000	-	
(I_C = 1.0 Adc, V_{CE2} = 5.0 Vdc)* 2N4974		2,000	4,000	-	
2N4975		1,000	2,000	-	
Collector-Emitter Saturation Voltage * (I_C = 500 mAdc, I_{B1} = 1.0 mAdc)	$V_{CE2(sat)}$*	-	1.4	2.0	Vdc
Base-Emitter Voltage * (I_C = 500 mAdc, I_{B1} = 1.0 mAdc)	V_{B1E2}*	-	2.0	2.7	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 20 mAdc, V_{CE2} = 5.0 Vdc, f = 100 MHz)	f_T	175	275	-	MHz
Output Capacitance (V_{CB1} = 10 Vdc, I_{E2} = 0, f = 140 kHz)	C_{ob1}	-	4.0	8.0	pF
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	h_{fe}				-
2N4974		25,000	-	-	
2N4975		15,000	-	-	
Noise Figure (I_C = 1.0 mAdc, V_{CB1} = 10 Vdc, R_S = 10 k ohms, BW = 15.7 kHz)	NF	-	3.0	6.0	dB

* Pulse Test: Pulse width ≦ 300 μs, duty cycle ≦ 2%

MRD200 (SILICON)

$V_{CEO} = 50\ V$
$P_D = 50\ mW$



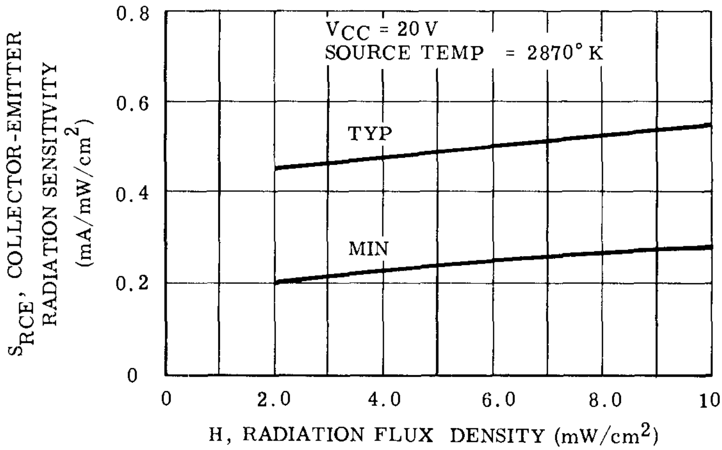
CASE 81

NPN silicon high sensitivity photo detector designed for use in circuits requiring high radiation sensitivity, stable characteristics, and high-density mounting.

MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Rating (NOTE 1)	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	Volts
Emitter-Collector Voltage	V_{ECO}	7.0	Volts
Total Device Dissipation @ $T_A = 25°C$	P_D	50	mW
Derate above 25°C		0.5	mW/°C
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 — COLLECTOR-EMITTER SENSITIVITY



MRD200 (continued)

STATIC ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristics (NOTE 1)	Fig. No.	Symbol	Min	Typ	Max	Units
Collector Dark Current (V_{CC} = 20 V; R_L = 100 ohms) (Note 3)	—	I_{CEO}				μA
T_A = 25°C			—	—	0.025	
T_A = 100°C			—	10	—	
Collector-Emitter Breakdown Voltage (I_C = 100 μA)	—	BV_{CEO}	50	—	—	Volts
Emitter-Collector Breakdown Voltage (I_E = 100 μA)	—	BV_{ECO}	7.0	—	—	Volts

OPTICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristics (NOTE 1)	Fig. No.	Symbol	Min	Typ	Max	Units
Collector-Emitter Radiation Sensitivity (V_{CC} = 20 V; R_L = 100 ohms)(Note 2)	1	S_{RCE}	0.25	0.5	—	mA/mW/cm²
Collector-Emitter Illumination Sensitivity (V_{CC} = 20 V; R_L = 100 ohms)(Note 4)	—	S_{ICE}	2.0	5.0		μA/lum/ft²
Photo Current Saturated Rise Time (Note 5)	4	$t_{r(sat)}$	—	1.0	—	μs
Photo Current Saturated Fall Time (Note 5)	4	$t_{f(sat)}$	—	10	—	μs
Photo Current Rise Time (Note 6)	4	t_r	—	—	2.5	μs
Photo Current Fall Time (Note 6)	4	t_f	—	—	4.0	μs
Wavelength of Maximum Sensitivity	—	λS(typ)	—	0.8	—	Microns

NOTES:

1. No base terminal available.
2. Radiation flux density (H) equal to 5.0 mW/cm² emitted from a tungsten source at a color temperature of 2870°K.
3. Measured under dark conditions. (H ≈ 0)
4. Luminous flux density (E) equal to 100 lumens/ft². (100 ft. -candles)
5. For saturated rise time measurements, radiation is provided by a pulsed xenon arc lamp with a pulse width of approximately 1.0 microsecond (see Figure 4).
6. For unsaturated rise time measurements, radiation is provided by a pulsed GaAs (gallium-arsenide) light-emitting diode (λ ≈ 0.9 microns) with a pulse width equal or greater than 10 microseconds (see Figure 4).

MRD200 (continued)

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 2 — COLLECTOR-EMITTER CHARACTERISTICS

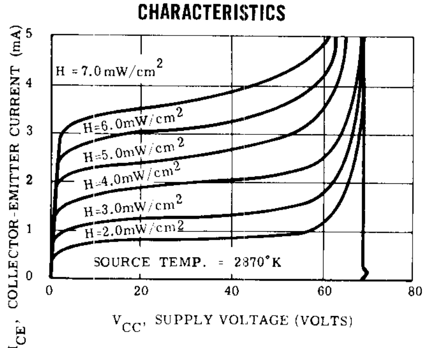


FIGURE 3 — PHOTO CURRENT vs TEMPERATURE

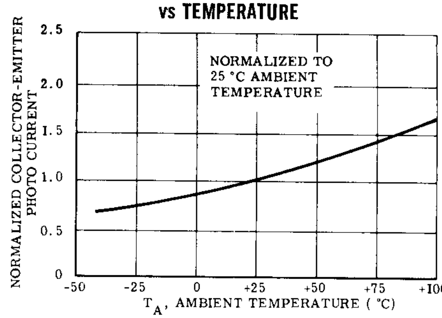
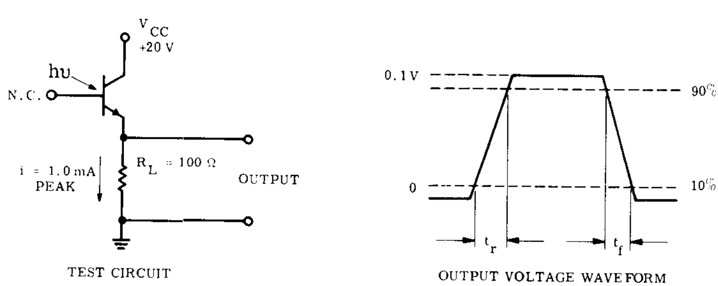
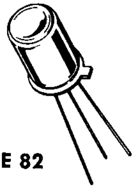


FIGURE 4 — PULSE RESPONSE TEST CIRCUIT



MRD300 (SILICON)

V_{CEO} = 50 V
P_D = 0.25 W



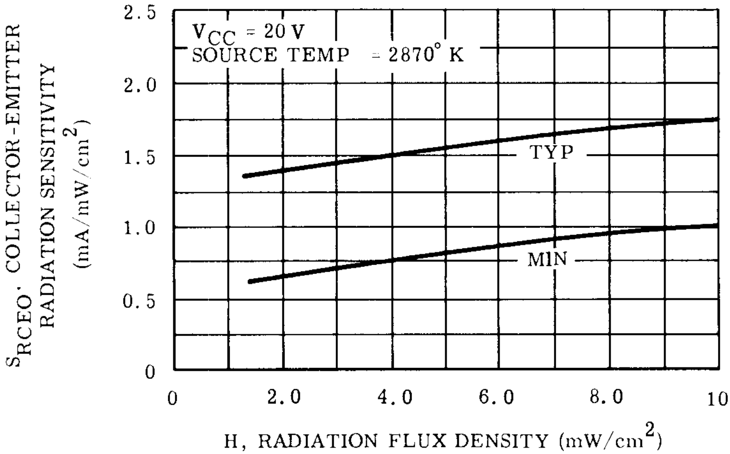
CASE 82

NPN silicon high sensitivity photo transistor designed for use in circuits requiring high radiation sensitivity and stable characteristics.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

RATING (NOTE 2)	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	Volts
Emitter-Collector Voltage	V_{ECO}	7.0	Volts
Collector-Base Voltage	V_{CBO}	80	Volts
Total Device Dissipation @ T_A = 25 °C Derate above 25 °C	P_D	0.25 1.43	Watt mW/°C
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-65 to +200	°C

FIGURE 1 — COLLECTOR-EMITTER SENSITIVITY



MRD300 (continued)

STATIC ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics	Fig. No.	Symbol	Min	Typ	Max	Units
Collector Dark Current (V_{CC} = 20 V; R_L = 100 ohms; Base Open) (Note 2)	—	I_{CEO}				μA
T_A = 25°C			—	—	0.025	
T_A = 100°C			—	10	—	
Collector-Base Breakdown Voltage (I_C = 100 μA; Emitter Open)	—	BV_{CBO}	80	—	—	Volts
Collector-Emitter Breakdown Voltage (I_C = 100 μA; Base Open)	—	BV_{CEO}	50	—	—	Volts
Emitter-Collector Breakdown Voltage (I_E = 100 μA; Base Open)	—	BV_{ECO}	7.0	—	—	Volts

OPTICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics	Fig. No.	Symbol	Min	Typ	Max	Units
Collector-Emitter Radiation Sensitivity (V_{CC} = 20V; R_L = 100 ohms; Base Open) (Note 1)	—	S_{RCEO}	0.8	1.6	—	mA/mW/cm²
Collector-Base Radiation Sensitivity (V_{CC} = 20V; R_L = 100 ohms; Emitter Open) (Note 1)	—	S_{RCBO}	1.4	—	—	μA/mW/cm²
Collector-Emitter Illumination Sensitivity (V_{CC} = 20V; R_L = 100 ohms; Base Open) (Note 3)	—	S_{ICEO}	4.0	10	—	μA/lum/ft²
Collector-Base Illumination Sensitivity (V_{CC} = 20V; R_L = 100 ohms; Emitter Open) (Note 3)	—	S_{ICBO}	0.01	—	—	μA/lum/ft²
Photo Current Saturated Rise Time (Note 4)	4	$t_{r(sat)}$	—	1.0	—	μs
Photo Current Saturated Fall Time (Note 4)	4	$t_{f(sat)}$	—	10	—	μs
Photo Current Rise Time (Note 5)	4	t_r	—	—	2.5	μs
Photo Current Fall Time (Note 5)	4	t_f	—	—	4.0	μs
Angular Alignment (Note 6)	6	θ	—	—	10	Degrees
Wavelength of Maximum Sensitivity	—	λS(typ)	—	0.8	—	Microns

NOTES:

1. Radiation Flux Density (H) equal to 5.0 mW/cm² emitted from a tungsten source at a color temperature of 2870°K.
2. Measured under dark conditions. (H ≈ 0)
3. Luminous flux density (E) equal to 100 lumens/ft². (100 ft.-candles)
4. For saturated rise time measurements, radiation is provided by a pulsed xenon arc lamp with a pulse width of approximately 1.0 microsecond (see Figure 4).
5. For unsaturated rise time measurements, radiation is provided by a pulsed GaAs (gallium-arsenide) light-emitting diode (λ ≈ 0.9 microns) with a pulse width equal or greater than 10 microseconds (see Figure 4).
6. Angular deviation from central axis of device within which the photo current will reach a maximum value.

MRD300 (continued)

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 2 — COLLECTOR-EMITTER CHARACTERISTICS

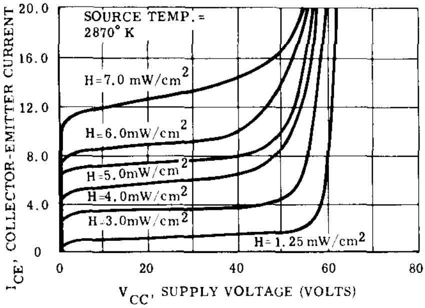


FIGURE 3 — PHOTO CURRENT vs TEMPERATURE

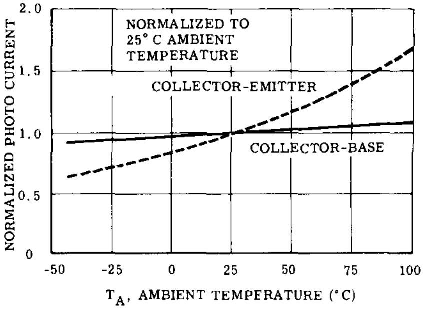


FIGURE 4 — PULSE RESPONSE TEST CIRCUIT

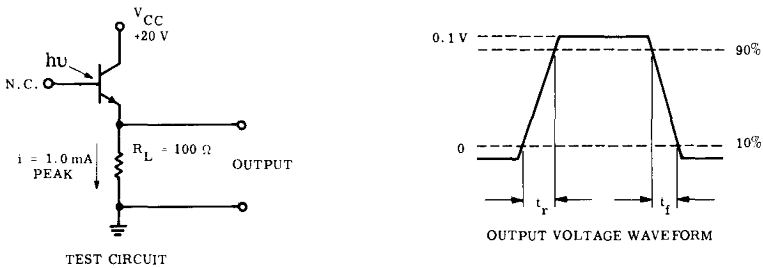


FIGURE 5 — BASE CURRENT vs RADIATION EQUIVALENT

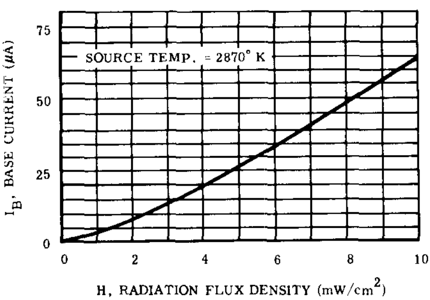
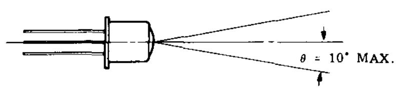
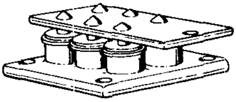


FIGURE 6 — AUGULAR ALIGNMENT



MPZ5-16 (SILICON)
MPZ5-32
MPZ5-180



CASE 119

Silicon power transient suppressor designed for applications requiring protection of voltage sensitive electronic devices in danger of destruction by high energy voltage transients. Individual cells are matched to insure current-sharing under high current pulse conditions.

MAXIMUM RATINGS

Transient Power Dissipation: 5.0 kW
Pulse Width: 1.0 ms

DC Power Dissipation: 350 Watts @ $T_C = 25^{o}C$
(Derate 2.33 W/^{o}C above 25^{o}C)

Operating Junction & Storage Temperature
Range: -65^{o}C to + 175^{o}C

Polarity:

Anode-to-Case is Standard
Cathode-to-Case Available Upon Request

MPZ5- SERIES (continued)

ELECTRICAL CHARACTERISTICS (Tc = 25°C)

Type	Nominal* Operating Voltage $V_{OP(PK)}$ Vdc	Nominal* Operating Voltage $V_{OP(RMS)}$ Vdc	Maximum Clamping Factor $C_F = \frac{V_{Z(max)}}{V_{Z(min)}}$	Minimum Zener Voltage $V_{Z(min)}$ Vdc	@ I_{ZT} Adc	Maximum Zener Voltage Pulse Width = 1.0 ms $V_{Z(max)}$ Vdc	@ I_Z Adc	Maximum Reverse Current $I_{R\,(max)}$ @ $V_R = V_{OP(PK)}$ μA	Typical Capacitance C (typ) @ $V_R = V_{OP(PK)}$ μF
MPZ5-16A	14	10	1.5	16	0.4	24	200	50	.025
-16B	14	10	1.25	16	0.4	20	200	↑	.025
-32A	28	20	1.56	32	0.2	50	100	│	.011
-32B	28	20	1.4	32	0.2	45	100	│	.011
-32C	28	20	1.25	32	0.2	40	100	│	.011
-180A	165	117	1.39	180	0.03	250	20	│	.0012
-180B	165	117	1.25	180	0.03	225	20	↓	.0012
-180C	165	117	1.14	180	0.03	205	20	50	.0012

* Nominal operating voltage defined as normal input voltage to device. If non-sinusoidal wave or dc input is present, peak voltage input values ($V_{OP(PK)}$) should be used to select type.

FIGURE 1 — PEAK SURGE POWER

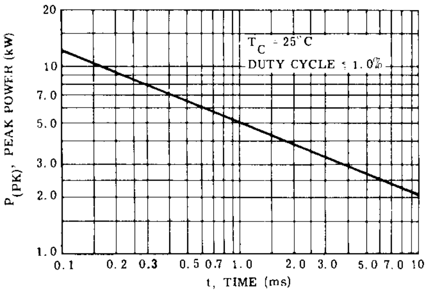
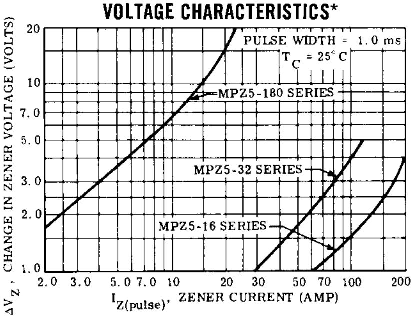


FIGURE 2 — TYPICAL DYNAMIC ZENER VOLTAGE CHARACTERISTICS*



* Figure 2 is intended to demonstrate the sharpness of the voltage breakdown characteristic of individual devices, and indicates the voltage overshoot.

$$\Delta V_Z = V_Z @ I_{Z(pulse)} - V_{Z(actual)} @ I_{ZT}$$

[redacted]

VARACTORS

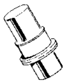
THE FOLLOWING VARACTORS ARE CHARACTERIZED IN THIS SECTION

1N5150A
1N5152A
1N5153A
1N5155A
1N5156
1N5157
MV1620
thru
MV1650
MV1720
thru
MV1750
MV1812A
MV1812B

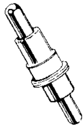
1N5150A (SILICON)
1N5152A
1N5153A
1N5155A

V_R = 35-80 V
I_F = 200-1000 mA
P_D = 8.75-29.2 W

Silicon high-frequency step-recovery power varactor devices optimized for critical multiplier applications requiring tight control of junction capacitance and power dissipation.



CASE 46



CASE 47

1N5152A
MV1808B1

1N5155A
MV1810B1

1N5150A
MV1807C1

1N5153A
MV1808C1

MAXIMUM RATINGS

Rating	Symbol	1N5150A	1N5152A	1N5153A	1N5155A	Unit
Reverse Voltage	V_R	80	75	75	35	Vdc
Forward Current	I_F	1000	250	250	200	mAdc
RF Power Input	P_{in}	40	15	15	7.0	Watts
Total Device Dissipation @ T_C = 25°C	P_D	29.2	11.7	11.7	8.75	Watts
Derate above 25°C		167	66.7	66.7	50	mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →				°C

1N5150A, 52A, 53A, 55A (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics		Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	1N5150A	BV_R	80	-	-	Vdc
	1N5152A, 1N5153A		75	-	-	
	1N5155A		35	-	-	
Reverse Current (V_R = 70 Vdc)	1N5150A	I_R	-	-	2.0	μAdc
(V_R = 70 Vdc, T_A = 150°C)	1N5150A		-	-	100	
(V_R = 60 Vdc)	1N5152A, 1N5153A		-	-	1.0	
(V_R = 60 Vdc, T_A = 150°C)	1N5152A, 1N5153A		-	-	100	
(V_R = 26 Vdc)	1N5155A		-	-	1.0	
(V_R = 26 Vdc, T_A = 150°C)	1N5155A		-	-	100	
Series Resistance (V_R = 6.0 Vdc, f = self-resonant frequency)	1N5150A	R_S	-	0.25	-	Ohms
	1N5152A, 1N5153A		-	0.5	-	
	1N5155A		-	0.9	-	
Series Inductance	1N5150A	L_S	-	1.5	-	nH
	1N5152A		-	0.8	-	
	1N5153A		-	1.7	-	
	1N5155A		-	0.9	-	
Diode Capacitance ($C_J + C_C$) (V_R = 6.0 Vdc, f = 1.0 MHz)	1N5150A	C_T	10.8	-	13.2	pF
	1N5152A		5.4	-	6.6	
	1N5153A		5.8	-	7.0	
	1N5155A		1.71	-	2.09	
Figure of Merit (V_R = 6.0 Vdc, f = 50 MHz)	1N5150A	Q	-	800	-	-
	1N5152A, 1N5153A		-	1100	-	
	1N5155A		-	1700	-	
Thermal Resistance	1N5150A	θ_{JC}	-	-	6.0	°C/W
	1N5152A, 1N5153A		-	-	15	
	1N5155A		-	-	20	

FUNCTIONAL TEST

1N5150A

RF Power Output	P_{in} = 37 W, f_{in} = 500 MHz,	P_{out}	25.1	-	-	Watts
Doubling Efficiency	f_{out} = 1.0 GHz	η	68	-	-	%

1N5152A, 1N5153A

RF Power Output	P_{in} = 12 W, f_{in} = 1.0 GHz,	P_{out}	7.2	-	-	Watts
Doubling Efficiency	f_{out} = 2.0 GHz	η	60	-	-	%

1N5155A

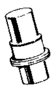
RF Power Output	P_{in} = 5.0 W, f_{in} = 2.0 GHz,	P_{out}	2.0	-	-	Watts
Tripling Efficiency	f_{out} = 6.0 GHz	η	40	-	-	%

For typical curves and test circuits, see the following data sheets: 1N5149-1N5150, 1N5151 thru 1N5153, and 1N5154-1N5155.

1N5156 (SILICON)
(MV1812A)
1N5157
(MV1812B)

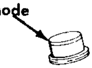
$V_R = 20$ V
$I_F = 160$ mA
$P_D = 3.25$ W

cathode



CASE 46

cathode



CASE 48

AVAILABLE IN PILL PACKAGE ON SPECIAL REQUEST

Silicon high-frequency step-recovery power varactors; epitaxial passivated devices designed for multiplier applications from 1 to 13 GHz with 1 watt minimum power output guaranteed at 10 GHz.

MAXIMUM RATINGS ($T_C = 25°C$ unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	20	Vdc
Forward Current	I_F	160	mAdc
RF Power Input	P_{in}	5.0	Watts
Total Device Dissipation @ $T_C = 75°C$ Derate above 75°C	P_D	3.25 26	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

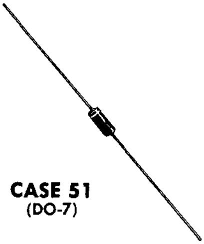
Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage	$I_R = 10\ \mu Adc$	BV_R	20	–	–	Vdc
Reverse Current	$V_R = 16$ Vdc $V_R = 16$ Vdc, $T_A = 150°C$	I_R	– –	– –	0.1 100	μAdc
Series Resistance	$V_R = 6.0$ Vdc, f = 50 MHz	R_S	–	1.1	–	Ohms
Diode Capacitance	$V_R = 6.0$ Vdc, f = 1.0 MHz	C_T	0.6	–	1.0	pF
Figure of Merit	$V_R = 6.0$ Vdc, f = 50 MHz	Q	–	3600	–	–
Thermal Resistance		θ_{JC}	–	–	38.5	°C/W

FUNCTIONAL TEST

RF Power Output	$P_{in} = 2.6$ watts, $f_{in} = 5.0$ GHz	P_{out}	1.0	–	–	Watt
Doubling Efficiency	$f_{out} = 10$ GHz	η	38.5	–	–	%

MV1620 thru MV1650

V_R = 20 V
I_F = 250 mA
Q = 150 to 300



CASE 51
(DO-7)

Silicon Epicap diodes, epitaxial passivated tuning diodes designed for AFC applications in radio, TV, and general electronic-tuning.

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	20	Volts
Forward Current	I_F	250	mA
Device Dissipation @ T_A = 25°C	P_D	400	mW
Derate above 25°C		2.67	mW/°C
Device Dissipation @ T_C = 25°C	P_D	2	Watts
Derate above 25°C		13.3	mW/°C
Junction Temperature	T_J	+175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic – All Types	Test Conditions	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage	I_R = 10 μAdc	BV_R	20	–	–	Vdc
Reverse Voltage Leakage Current	V_R = 15 Vdc	I_R	–	–	0.1	μAdc
Series Inductance	f = 250 MHz, lead length ≈ 1/16"	L_S	–	5.0	10	nH
Case Capacitance	f = 1 MHz, lead length ≈ 1/16"	C_C	–	0.25	0.3	pF

Device	C_T, Diode Capacitance V_R = 4 Vdc, f = 1 MHz pF			Q, Figure of Merit V_R = 4 Vdc, f = 50 MHz	TR, Tuning Ratio C_2/C_{20} f = 1 MHz	
	Min	Nom	Max	Min	Min	Max
MV1620	6.1	6.8	7.5	300	2.0	3.2
MV1622	7.4	8.2	9.0	300	2.0	3.2
MV1624	9.0	10.0	11.0	300	2.0	3.2
MV1626	10.8	12.0	13.2	300	2.0	3.2
MV1628	13.5	15.0	16.5	250	2.0	3.2
MV1630	16.2	18.0	19.8	250	2.0	3.2
MV1632	18.0	20.0	22.0	250	2.0	3.2
MV1634	19.8	22.0	24.2	250	2.0	3.2
MV1636	24.3	27.0	29.7	200	2.0	3.2
MV1638	29.7	33.0	36.3	200	2.0	3.2
MV1640	35.1	39.0	42.9	200	2.0	3.2
MV1642	42.3	47.0	51.7	200	2.0	3.2
MV1644	50.4	56.0	61.6	150	2.0	3.2
MV1646	61.2	68.0	74.8	150	2.0	3.2
MV1648	73.8	82.0	90.2	150	2.0	3.2
MV1650	90.0	100.0	110.0	150	2.0	3.2

TR, Tuning Ratio, is the ratio of C_T measured at 2 Vdc divided by C_T measured at 20 Vdc.

MV1720 thru MV1750

$V_R = 30\ V$
$I_F = 250\ mA$
$Q = 250\text{-}500$

CASE 51
(DO-7)

Silicon Epicap diodes, epitaxial passivated tuning diodes designed for VHF and UHF electronic tuning, FM, AFC and harmonic-generation applications, providing solid-state reliability to replace mechanical tuning methods.

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	30	Volts
Forward Current	I_F	250	mA
RF Power Input †	P_{in}	5.0	Watts
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 2.67	mW mW/°C
Device Dissipation @ T_C = 25°C Derate above 25°C	P_C	2.0 13.3	Watts mW/°C
Junction Temperature	T_J	+175	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

† Adequate heat sinking must be provided.

MV1720 thru MV1750 (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic – All Types	Test Conditions	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage	I_R = 10 μAdc	B_{VR}	30	—	—	Vdc
Reverse Voltage Leakage Current	V_R = 25 Vdc, T_A = 25°C V_R = 25 Vdc, T_A = 150°C	I_R	— —	— —	0.02 20	μAdc
Series Inductance	f = 250 MHz, lead length ≈ 1/16"	L_S	—	5.0	—	nH
Case Capacitance	f = 1 MHz, lead length ≈ 1/16"	C_C	—	0.25	—	pF
Diode Capacitance Temperature Coefficient	V_R = 4 Vdc, f = 1 MHz	TC_C	—	200	300	ppm/°C

Device	C_T, Diode Capacitance V_R = 4 Vdc, f = 1 MHz pF			TR, Tuning Ratio C_2/C_{30} f = 1 MHz		Q, Figure of Merit V_R = 4 Vdc f = 50 MHz
	Min	Nom	Max	Min	Max	Min
MV1720	6.1	6.8	7.5	2.80	3.80	500
MV1722	7.4	8.2	9.0	2.80	3.80	500
MV1724	9.0	10.0	11.0	2.80	3.80	500
MV1726	10.8	12.0	13.2	3.00	4.00	450
MV1728	13.5	15.0	16.5	3.00	4.00	450
MV1730	16.2	18.0	19.8	3.00	4.00	450
MV1732	18.0	20.0	22.0	3.20	4.20	400
MV1734	19.8	22.0	24.2	3.20	4.20	400
MV1736	24.3	27.0	29.7	3.20	4.20	400
MV1738	29.7	33.0	36.3	3.20	4.20	350
MV1740	35.1	39.0	42.9	3.20	4.20	350
MV1742	42.3	47.0	51.7	3.20	4.20	300
MV1744	50.4	56.0	61.6	3.20	4.20	300
MV1746	61.2	68.0	74.8	3.20	4.20	250
MV1748	73.8	82.0	90.2	3.20	4.20	250
MV1750	90.0	100.0	110.0	3.20	4.20	250

PARAMETER TEST METHODS

1. L_S, SERIES INDUCTANCE
L_S is measured on a shorted package at 250 MHz using an impedance bridge (Boonton Radio Model 250A RX Meter or equivalent).

2. C_C, CASE CAPACITANCE
C_C is measured on an open package at 1 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

3. C_T, DIODE CAPACITANCE
($C_T = C_C + C_J$). C_T is measured at 1 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

4. TR, TUNING RATIO
TR is the ratio of C_T measured at 2 Vdc divided by C_T measured at 30 Vdc.

5. Q, FIGURE OF MERIT
Q is calculated by taking the G and C readings of an admittance bridge at the specified frequency and substituting in the following equations:

$$Q = \frac{2\pi fC}{G}$$

(Boonton Electronics Model 33AS8 or equivalent).

6. TC_C, DIODE CAPACITANCE TEMPERATURE COEFFICIENT
TC_C is guaranteed by comparing C_T at V_R = 4 Vdc, f = 1 MHz, T_A = −65°C with C_T at V_R = 4 Vdc, f = 1 MHz, T_A = +85°C in the following equation, which defines TC_C:

$$TC_C = \left| \frac{C_T(+85°C) - C_T(-65°C)}{85 + 65} \right| \cdot \frac{10^6}{C_T(25°C)}$$

MV1720 thru MV1750 (continued)

FIGURE 1 — DIODE CAPACITANCE versus REVERSE VOLTAGE

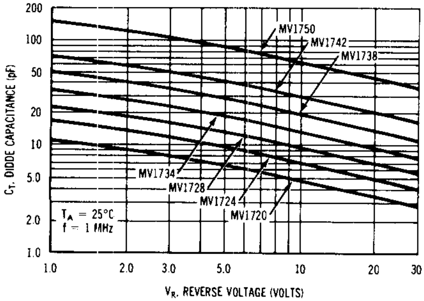


FIGURE 2 — FIGURE OF MERIT versus REVERSE VOLTAGE

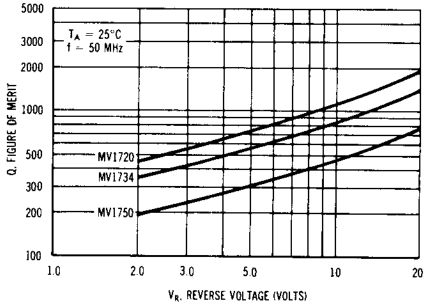


FIGURE 3 — NORMALIZED DIODE CAPACITANCE versus JUNCTION TEMPERATURE

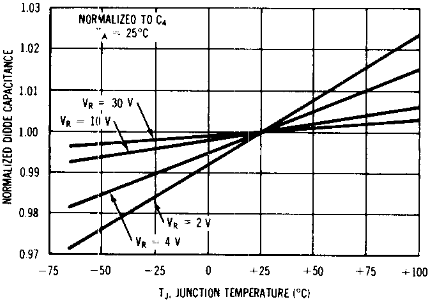


FIGURE 4 — NORMALIZED FIGURE OF MERIT versus JUNCTION TEMPERATURE

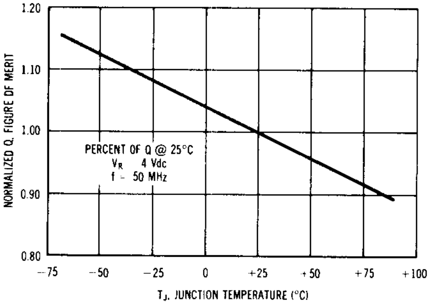


FIGURE 5 — REVERSE CURRENT versus REVERSE BIAS VOLTAGE

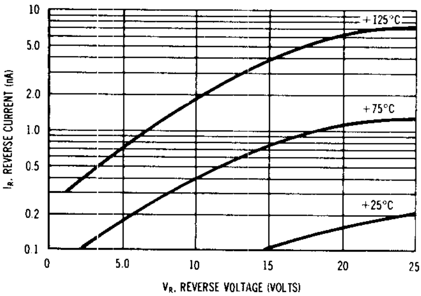
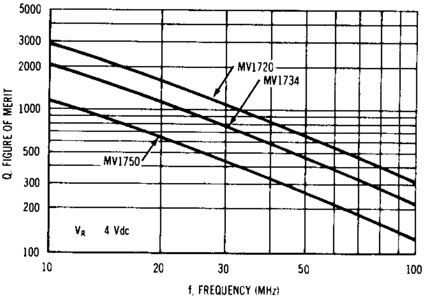


FIGURE 6 — FIGURE OF MERIT versus FREQUENCY



MV1720 thru MV1750 (continued)

EPICAP VOLTAGE-VARIABLE CAPACITANCE DIODE DEVICE CONSIDERATIONS

A. EPICAP NETWORK PRESENTATION

The equivalent circuit in Figure 7 shows the voltage capacitance and parasitic elements of an EPICAP diode. For design purposes at all but very high and very low frequencies, L_S, R_J, and C_C can be neglected. The simplified equivalent circuit of Figure 8 represents the diode under these conditions.

Definitions:

- C_J — Voltage-Variable Junction Capacitance
- R_S — Series Resistance (semiconductor bulk, contact, and lead resistance)
- C_C — Case Capacitance
- L_S — Series Inductance
- R_J — Voltage-Variable Junction Resistance (negligible above 100 kHz)

FIGURE 7

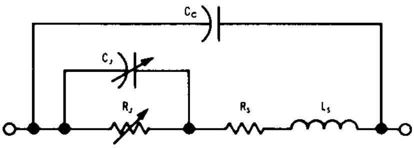
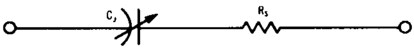


FIGURE 8



B. EPICAP CAPACITANCE vs REVERSE BIAS VOLTAGE

The most important design characteristic of an EPICAP diode is the C_T versus V_R variation as shown in equations 1 and 2. Since the designer is primarily interested in the slope of C_T versus V_R, the C_C, C_O, ϕ, and γ characteristics have been encompassed by the simplified equation 3. Min/max limits on α can be guaranteed over a specified V_R range.

$$C_T = C_C + C_J \quad (1)$$

$$C_T = C_C + \frac{C_o}{\left(1 + \frac{V_R}{\phi}\right)^{\gamma}} \quad (2)$$

$C_o = C_J$ at $V_R = 0$ — V_R = Reverse Bias

ϕ = Contact Potential, $\phi \approx 0.6$ Volt — $\gamma = C_J$ slope, $\gamma \approx 0.5$

$$C_T = \frac{K}{V_R{}^{\alpha}} \quad (3)$$

C. EPICAP CAPACITANCE vs FREQUENCY

Variations in EPICAP effective capacitance, as a function of operating frequency, can be derived from a simplified equivalent circuit similar to that of Figure 7, but neglecting R_S and R_J. The admittance expression for such a circuit is given in equation 4. Examination of equation 4 yields the following information:

At low frequencies, $C_{eq} \approx C_J$; at very high frequencies ($f \approx \infty$) $C_{eq} \approx C_C$.

As frequency is increased from 1 MHz, C_{eq} increases until it is maximum at $\omega^2 = 1/L_S C_J$; and as ω^2 is increased from $1/L_S C_J$ toward infinity, C_{eq} increases from a very negative capacitance (inductance) toward $C_{eq} = C_C$, a positive capacitance.

Very simple calculations for C_{eq} at higher frequencies indicate the problems encountered when capacity measurements are made above 1 MHz. As ω approaches $\omega_o = 1/\sqrt{L_S C_J}$, small variations in L_S cause extreme variations in measured diode capacitance.

$$Y = j\omega C_{eq} = j\omega C_c + \frac{j\omega C_J}{1 - \omega^2 L_S C_J} \quad (4)$$

D. EPICAP FIGURE OF MERIT (Q) AND CUTOFF FREQUENCY (f_{co})

The efficiency of EPICAP response to an input frequency is related to the Figure of Merit of the device as defined in equation 5. For very low frequencies, equation 6 applies whereas at high frequencies, where R_J can be neglected, equation 5 may be rewritten into the familiar form of equation 7.

Another useful parameter for EPICAP devices is the cutoff frequency (f_{co}), and is the frequency point where Q is equal to 1. Equation 8 gives this relationship.

$$Q = \frac{X_{Seq}}{R_{Seq}} \quad (5)$$

$$Q_{LF} = \frac{\omega C_J R_J{}^2}{R_J + R_S(1 + \omega^2 C_J{}^2 R_J{}^2)} \quad (6)$$

$$Q_{HF} = \frac{1}{\omega R_S C_{eq}} \quad (7)$$

$$f_{co} = Qf_{meas} \approx \frac{1}{2\pi R_S C_{VR}} \quad (8)$$

E. HARMONIC GENERATION USING EPICAPS

Efficient harmonic generation is possible with Motorola EPICAPS because of their high cutoff frequency and breakdown voltage. Since EPICAP junction capacitance varies inversely with the square root of the breakdown voltage, harmonic generator performance can be accurately predicted from various idealized models. Equation 9 gives the level of maximum input power for the EPICAP and equation 10 gives the relationships governing EPICAP circuit efficiency. In these equations, adequate heat sinking has been assumed.

$$P_{in(max)} = \frac{M(BV_R + \phi)^2}{R_S} \frac{f_{in}}{f_{co}} \quad (9)$$

$M(x2) = 0.0285$; $M(x3) = 0.0241$; $M(x4) = 0.196$

$$Eff = 1 - N\frac{f_{out}}{f_{co}} \quad (10)$$

$N(x2) = 20.8$; $N(x3) = 34.8$; $N(x4) = 62.5$

M and N are Constants

INTEGRATED CIRCUITS

THE FOLLOWING INTEGRATED CIRCUITS ARE INCLUDED IN THIS SECTION

MECL MC300 SERIES INTEGRATED CIRCUITS

The following five pages contain specifications for the most recent additions to the MECL MC300 series integrated circuits.

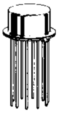
These are:

MC312A	Dual 3-Input Gate
MC316	Lamp Driver
MC317	MECL-to-Saturated Logic Translator
MC318	Saturated Logic-to-MECL Dual Translator

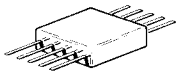
The entire line is completely characterized in the latest MECL MC300 Series (DS 9044 R2) brochure or can be found in the Integrated Circuits Section or the Late Addition Section of the 2nd Edition Data Book.

MC312A

DUAL 3-INPUT GATE

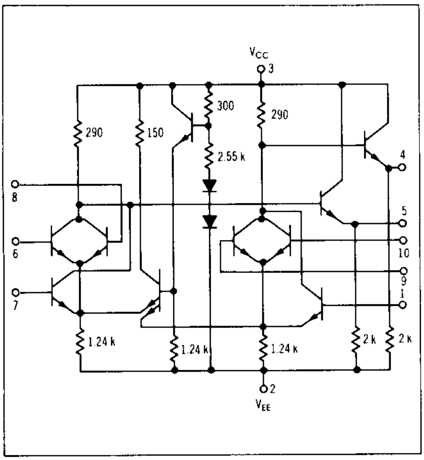


CASE 71
SUFFIX G

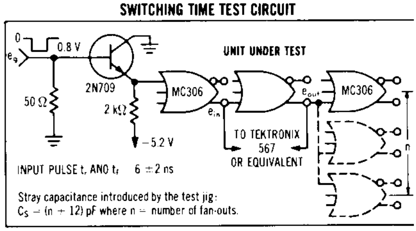


(TO-91)
CASE 72
SUFFIX F

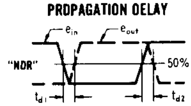
Dual 3-input gate that provides the positive logic "NOR" function, and features an internal bias driver.



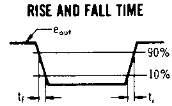
SWITCHING TIME TEST CIRCUIT



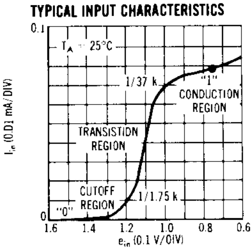
PROPAGATION DELAY



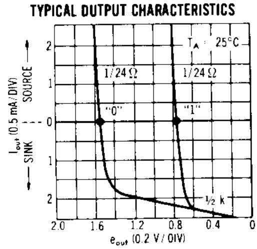
RISE AND FALL TIME



TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



MC312A (Continued)

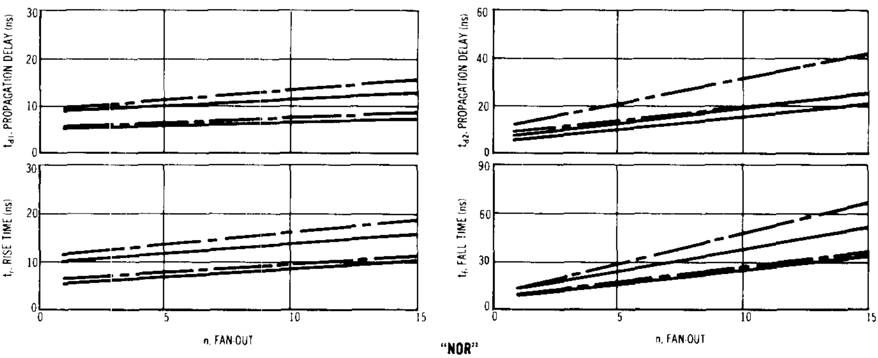
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
−55°C	—	−0.945	−1.450	−5.20
+25°C	−0.690	−0.795	−1.350	−5.20
+125°C	—	−0.655	−1.300	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	—	1,2,6,7,8,9,10	—	—	3	I_E (2)	—	17.7	—	17.0	—	16.4	mAdc
Input Current	1	—	—	2,6,7,8,9,18	—	—	3	I_{in} (1)	—	—	—	100	—	—	µAdc
	6	—	—	1,2,7,8,9,10	—	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	6	1,2,7,8,9,18	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	7	1,2,6,8,9,10	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	1,2,6,7,9,18	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	1	2,6,7,8,9,10	—	—	3	V_1 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	1,2,6,7,8,10	—	—	3	V_1 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	10	1,2,6,7,8,9	—	—	3	V_1 (4)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltage	—	6	—	1,2,7,8,9,10	—	—	3	V_4 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	7	—	1,2,6,8,9,10	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	1,2,6,7,9,10	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	1	—	2,6,7,8,9,10	—	—	3	V_4 (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	1,2,6,7,8,10	—	—	3	V_4 (4)	↓	↓	↓	↓	↓	↓	↓
	—	10	—	1,2,6,7,8,9	—	—	3	V_4 (4)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change	—	—	6	1,2,7,8,9,10	—	5②	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.060	Volts
	—	—	1	2,6,7,8,9,10	—	4②	3	ΔV_1 (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,18	6①	—	3	V_3 (5)	—	−0.40	—	−0.55	—	−0.60	Vdc
	—	—	—	1,2,6,8,9,10	7①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,2,6,7,9,10	8①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7,8,9,10	1①	—	3	V_3 (4)	—	↓	—	↓	—	↓	↓
	—	—	—	1,2,6,7,8,10	9①	—	3	V_3 (4)	—	↓	—	↓	—	↓	↓
	—	—	—	1,2,6,7,8,9	10①	—	3	V_3 (4)	—	↓	—	↓	—	↓	↓
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	5	—	1,2,7,8,9,10	—	—	3	t_{d1} (5)	6.5	10.5	6.5	10.5	7.5	11.5	ns
	1	4	—	2,6,7,8,9,10	—	—	3	t_{d1} (4)	6.5	10.5	6.5	10.5	7.5	11.5	↓
	6	5	—	1,2,7,X,9,10	—	—	3	t_{d2} (5)	0.5	11.5	0.5	11.5	10.0	15.0	↓
	1	4	—	2,6,7,8,9,10	—	—	3	t_{d2} (4)	8.5	11.5	8.5	11.5	18.0	15.0	↓
Rise Time	6	5	—	1,2,7,8,9,10	—	—	3	t_r (5)	9.0	12.5	9.5	12.5	11.5	15.5	↓
	1	4	—	2,6,7,8,9,10	—	—	3	t_r (4)	9.0	12.5	9.5	12.5	11.5	15.5	↓
Fall Time	6	5	—	1,2,7,8,9,10	—	—	3	t_f (5)	8.5	14.8	9.0	14.0	11.5	17.0	↓
	1	4	—	2,6,7,X,9,10	—	—	3	t_f (4)	0.5	14.0	9.0	14.0	11.5	17.8	

Pins not listed are left open.
① Input voltage is adjusted to obtain dv "NOR"/dV_{in} = 0. ② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

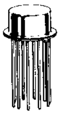
SWITCHING CHARACTERISTICS (10% to 90% distribution)



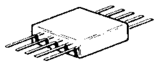
"NOR"

——— −55°C and +25°C
— — +125°C

MC316
LAMP DRIVER

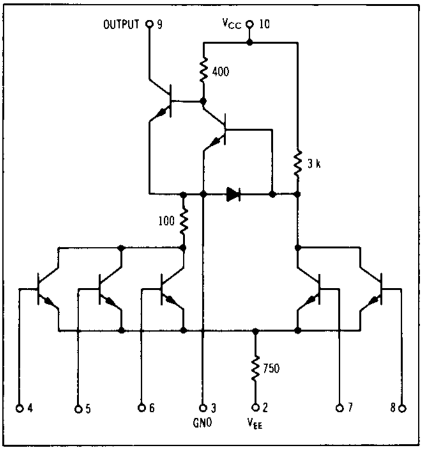


CASE 71
SUFFIX G



(TO-91)
CASE 72
SUFFIX F

Lamp driver that provides "OR" or "NOR" logic depending on the bias arrangement used and is capable of driving 6 V lamps.



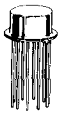
ELECTRICAL CHARACTERISTICS

Characteristic	V_H Pin No	$V_{i\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	I_L ② Pin No	Ground Pin No	Symbol Pin No in ( )	−55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Test Conditions (Vdc ± 1%; I_L in mAdc)																
@ Test Temperature −55°C	—	−0.945	−1.450	−5.20	−1.25	+6.0	100									
@ Test Temperature +25°C	−0.670	−0.795	−1.350	−5.20	−1.15	+6.0	100									
@ Test Temperature +125°C	—	−0.655	−1.300	−5.20	−1.00	+6.0	50									
Power Supply Drain Current	—	4,5,6	—	2,7	8	10	—	3	I_C (10)	—	21.0	—	21.0	—	20.5	
	—	4,5,6	—	2,7	8	18	—	3	I_E (2)	—	8.0	—	8.8	—	7.7	mAdc
Input Current	4	—	—	2,5,6,7	8	10	—	3	I_{in} (4)	—	—	—	200	—	—	μAdc
	5	—	—	2,4,6,7	8	18	—	3	I_{in} (5)	—	—	—		—	—	
	6	—	—	2,4,5,7	8	10	—	3	I_{in} (6)	—	—	—		—	—	
	7	—	—	2,4,5,6	8	10	—	3	I_{in} (7)	—	—	—		—	—	
	8	—	—	2,4,5,7	6	18	—	3	I_{in} (8)	—	—	—		—	—	
Output Voltage, Low	—	—	6	2,4,5,7	8	10	9	3	V_{OL} (9)	—	0.9	—	1.0	—	0.8	
	—	—	6	2,4,5,8	7	18	9	3	V_{OL} (9)	—	0.9	—	1.0	—	0.8	
Output Voltage, High	—	4	—	2,5,6,7	8	18,9①	—	3	V_{OH} (4)	—	—	—	5.8	—	5.8	Vdc
	—	5	—	2,4,6,7	8	18,9①	—	3	V_{OH} (5)	—	—	—		—		
	—	6	—	2,4,5,7	8	18,9①	—	3	V_{OH} (6)	—	—	—		—		
	—	6	—	2,4,5,8	7	10,9①	—	3	V_{OH} (6)	—	—	—		—		

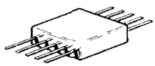
Pins not listed are left open. ① Pin 9 is connected to V_{CC} through a 18 k-ohm resistor.
② I_L specified for ambient temperature conditions. I_L = 100 mAdc at T_C = +125°C is acceptable, requiring a heat sink.

MC317

MECL-TO-SATURATED LOGIC TRANSLATOR

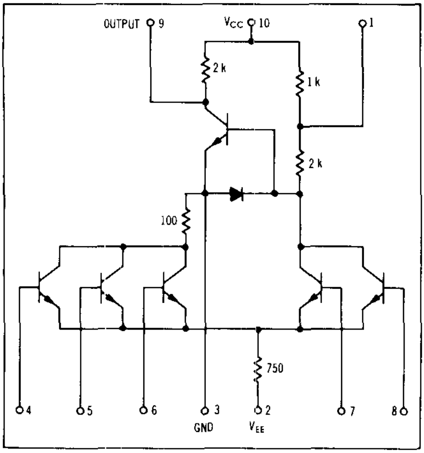


CASE 71
SUFFIX G

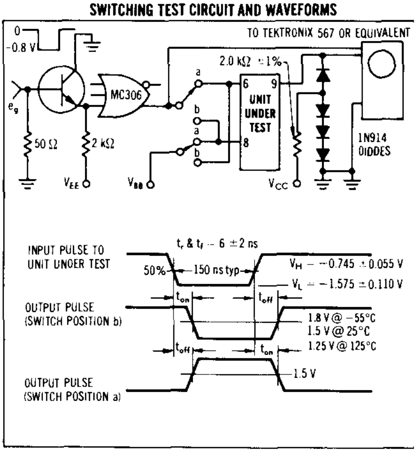


(TO-91)
CASE 72
SUFFIX F

Level translator intended for converting non-saturated MECL signal levels to saturated logic levels; provides "OR" or "NOR" logic depending on the bias arrangement used.



SWITCHING TEST CIRCUIT AND WAVEFORMS

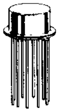


ELECTRICAL CHARACTERISTICS

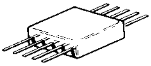
Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	−55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Test Conditions (Vdc ±1%; I_L mAdc) @ Test Temperature −55°C	—	−0.945	−1.450	−5.20	−1.25	+6.0	10									
@ Test Temperature +25°C	−0.690	−0.795	−1.350	−5.20	−1.15	+6.0	10									
@ Test Temperature +125°C	—	−0.655	−1.300	−5.20	−1.00	+6.0	10									
Power Supply Drain Current	—	6	—	2,4,5,7	8	10	—	3	I_C (10)	—	7.0	—	7.0	—	6.8	mAdc
	—	—	—	2,4,5,6,7	8	10	—	3	I_E (2)	—	7.0	—	7.0	—	6.8	mAdc
Input Current	4	—	—	2,5,6,7	8	10	—	3	I_{in} (4)	—	—	—	200	—	—	µAdc
	5	—	—	2,4,6,7	8	10	—	3	I_{in} (5)	—	—	—	↓	—	—	↓
	6	—	—	2,4,5,7	8	10	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	2,0,5,X	6	10	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,4,5,7	6	10	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
Output Voltage, High	—	—	—	2,4,5,6,7	8	10	—	3	V_{OH} (9)	—	—	5.X	—	—	—	Vdc
	—	—	—	2,4,5,6,X	7	10	—	3	V_{OH} (9)	—	—	5.8	—	—	—	Vdc
Output Voltage, Low	—	4	—	2,5,6,7	8	10	9	3	V_{OL} (9)	—	0.45	—	0.45	—	0.50	Vdc
	—	5	—	2,4,6,7	8	10	9	3	V_{OL} (9)	—	↓	—	↓	—	↓	↓
	—	6	—	2,4,5,7	8	10	9	3	V_{OL} (9)	—	↓	—	↓	—	↓	↓
	—	6	—	2,4,5,X	7	10	9	3	V_{OL} (9)	—	↓	—	↓	—	↓	↓
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Turn-On Time	6	9	—	2,4,5,7	8	10	—	3	t_{on}	27.5	40.0	27.5	35.0	29.5	35.8	ns
	8	9	—	2,4,5,7	6	10	—	3	t_{on}	27.5	40.0	27.5	35.0	29.5	35.0	↓
Turn-Off Time	6	9	—	2,4,5,7	8	10	—	3	t_{off}	25.0	40.0	26.0	35.0	27.0	40.0	↓
	8	9	—	2,4,5,7	6	10	—	3	t_{off}	25.0	40.0	26.0	35.0	27.0	40.0	↓

MC318

SATURATED LOGIC-TO-MECL DUAL TRANSLATOR
(Additions to MC300 Series)

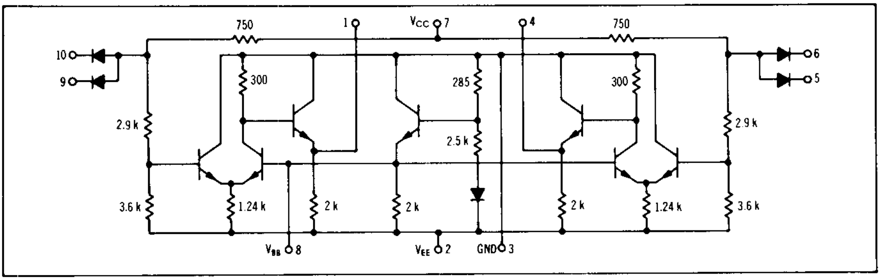


CASE 71
SUFFIX G

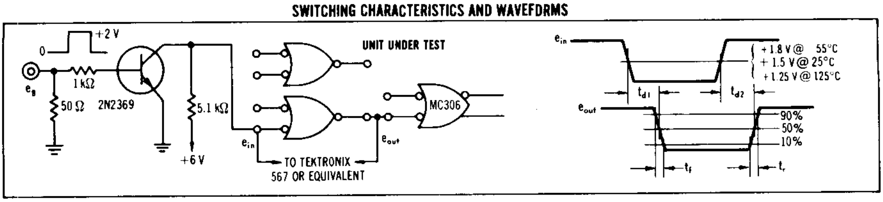


(TO-91)
CASE 72
SUFFIX F

Level translator intended for converting saturated logic levels to non-saturated MECL signal levels.



SWITCHING CHARACTERISTICS AND WAVEFORMS



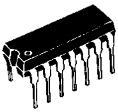
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
−55°C	+0.45	+5.0	−5.20	+6.0
+25°C	+0.45	+5.0	−5.20	+6.0
+125°C	+0.45	+5.0	−5.20	+6.0

Characteristic	V Pin No	V Pin No	V_{EE} Pin No	V_{CC} Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	— —	— —	2 2	7 7	3 3	I_C (7) I_E (2)	— —	4.0 24.8	— —	4.0 24.0	— —	3.9 23.3	mAdc mAdc
Input Load Current	— — — —	— — — —	2 2 2 2	7 7 7 7	3,5 3,6 3,9 3,10	I_L (5) I_L (6) I_L (9) I_L (10)	— — — —	— — — —	— — — —	8.0 ↓	— — — —	— — — —	mAdc ↓
Input Reverse Current	— — — —	— — — —	2 2 2 2	5,7 6,7 7,9 7,10	3,6 3,5 3,18 3,9	I_R (5) I_R (6) I_R (9) I_R (18)	— — — —	— — — —	— — — —	8.5 ↓	— — — —	2.0 ↓	μAdc ↓
"OR" Logical "1" Output Voltage	— — — —	5 6 9 18	2 2 2 2	7 7 7 7	3 3 3 3	V_5 (4) V_5 (4) V_5 (1) V_5 (1)	−8.825 ↓	−0.945 ↓	−0.698 ↓	−0.795 ↓	−8.525 ↓	0.655 ↓	Vdc ↓
"OR" Logical "0" Output Voltage	5 6 9 18	— — — —	2 2 2 2	7 7 7 7	3 3 3 3	V_2 (4) V_2 (4) V_2 (1) V_2 (1)	−1.560 ↓	−1.850 ↓	−1.465 ↓	−1.750 ↓	−1.340 ↓	1.675 ↓	Vdc ↓
Bias Voltage Output Current	—	—	2	7	3	V_{BB} (8)	−1.19 ↓	−1.32 ↓	−1.09 ↓	−1.22 ↓	−0.95 ↓	−1.08 ↓	Vdc ↓
Switching Times	Pulse In	Pulse Out					Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	5 9	4 1	2 2	7 7	3 3	t_{d1} (4) t_{d1} (1)	16.5 16.5	27.0 27.8	15.8 15.0	23.0 23.0	19.0 19.8	20.8 28.0	ns
	5 9	4 1	2 2	7 7	3 3	t_{d2} (4) t_{d2} (1)	13.0 13.0	20.0 20.0	15.5 15.5	23.0 23.0	20.0 20.0	31.0 31.0	↓
Rise Time	5 9	4 1	2 2	7 7	3 3	t_r (4) t_r (1)	8.0 8.0	15.0 15.0	7.8 7.0	13.0 13.0	9.5 9.5	16.0 16.0	↓
Fall Time	5 9	4 1	2 2	7 7	3 3	t_f (4) t_f (1)	8.0 8.0	14.0 14.0	7.5 7.5	13.0 13.0	10.0 10.0	17.0 17.0	↓

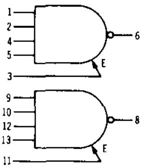
Pins not listed are left open.

MC660P
MC661P
MHTL DUAL 4-INPUT GATES



UNIBLOC
PLASTIC PACKAGE
CASE 93

Expandable dual 4-input "NAND/NOR" gates - high-noise-immunity industrial logic circuits for medium-speed digital applications in environments with a high level of electrical noise. Type MC660P has an active output pull-up transistor.



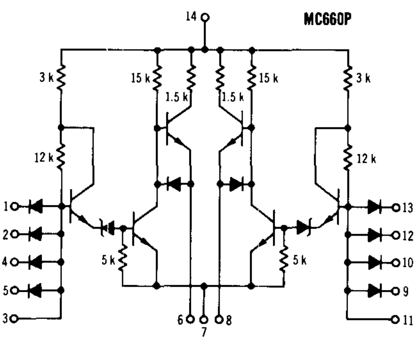
NOISE IMMUNITY = 5 V
TYPICAL LOGIC SWING = 13 V
POWER DISSIPATION — 60 mW TYP

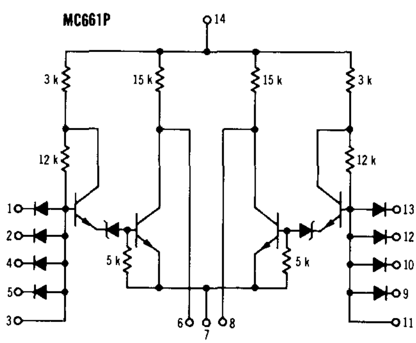
Input Loading Factor = 1, Output Loading Factor = 10
Loading factors are valid from −30 to +75°C
with V_{CC} = 15 ± 1 Vdc.

MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage - Continuous Pulsed, < 1 second	18 20	Vdc
Input Voltage	-1.0/+18.0	Vdc
Output Current (into Outputs)	30	mAdc
Input Reverse Current @ 20 V	0.5	mAdc
Operating Temperature Range	-30 to +75	°C
Storage Temperature Range	-55 to +125	°C

CIRCUIT SCHEMATICS





MC660P, MC661P (continued)

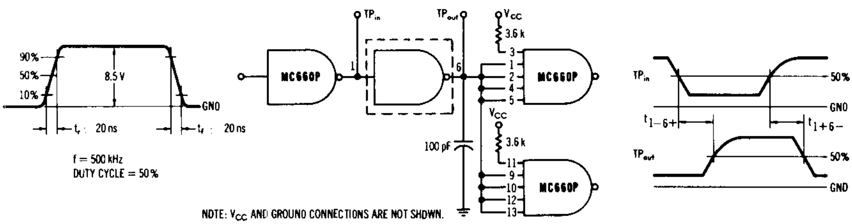
ELECTRICAL CHARACTERISTICS

Unless otherwise noted, tests are shown for only one gate of each device. The other gate is tested in a similar manner.

Characteristic	Symbol	Pin Under Test	TEST LIMITS −30 ±3°C Min	−30 ±3°C Max	+25 ±3°C Min	+25 ±3°C Max	+75 ±3°C Min	+75 ±3°C Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_X	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Ground
TEST CURRENT / VOLTAGE VALUES (All Temperatures)										mA	mA	Volts	Volts	Volts	Volts	Volts	Volts	Volts	Volts	Volts	
										12.0	-0.02	6.50	0.50	0	10.0	7.20	10.0	15.0	14.0	16.0	
										TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:											
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	1, 2, 4, 5	-	-	-	-	-	-	14	7
	V_{OH}	6	-	-	12.5	-	12.5	-	↓	-	6	1	-	-	-	-	-	2, 4, 5	14	-	7
	↓	6	-	-	↓	-	↓	-	↓	-	6	2	-	-	-	-	-	1, 4, 5	14	-	7
	↓	6	-	-	↓	-	↓	-	↓	-	6	4	-	-	-	-	-	1, 2, 5	14	-	7
	↓	6	-	-	↓	-	↓	-	↓	-	6	5	-	-	-	-	-	1, 2, 4	14	-	7
	↓	6	-	-	↓	-	-	-	↓	-	6	-	-	-	-	3	-	-	14	-	7
Short-Circuit Current MC660P	I_{SC}	6	-	-	-6.5	-15.0	-6.5	-15.0	mAdc	-	-	-	-	-	-	-	-	-	-	14	t, 6, 7
MC661P	I_{SC}	6	-	-	-0.6	-1.5	-0.6	-1.5	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 6, 7
Reverse Current	I_R	1	-	-	-	2.0	-	2.0	µAdc	-	-	-	-	-	1	-	-	-	14	-	2, 3, 4, 5, 7
	↓	2	-	-	-	↓	-	↓	↓	-	-	-	-	-	2	-	-	-	14	-	1, 3, 4, 5, 7
	↓	4	-	-	-	↓	-	↓	↓	-	-	-	-	-	4	-	-	-	14	-	1, 2, 3, 5, 7
	↓	5	-	-	-	↓	-	↓	↓	-	-	-	-	-	5	-	-	-	14	-	1, 2, 3, 4, 7
Output Leakage Current	I_{CEX}	6	-	-	-	100	-	100	µAdc	-	-	-	-	-	-	-	6, 14	-	-	-	1, 7
Forward Current	I_F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2, 4, 5	-	-	-	-	14	7
	↓	2	-	-	-	↓	-	↓	↓	-	-	-	-	2	1, 4, 5	-	-	-	-	14	7
	↓	4	-	-	-	↓	-	↓	↓	-	-	-	-	4	1, 2, 5	-	-	-	-	14	7
	↓	5	-	-	-	↓	-	↓	↓	-	-	-	-	5	1, 2, 4	-	-	-	-	14	7
Power Drain Current (Both Gates)	I_{CCL}	14	-	-	-	3.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 2, 4, 5, 7, 9, 10, 12, 13
	I_{CCH}	14	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out										
MC660P	t_{1-6+}	6	-	-	-	200	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7
MC661P		6	-	-	-	250	-	-	↓	1	6	-	-	-	-	-	-	14	-	-	7
Both Types	t_{1+6-}	6	-	-	-	100	-	-	↓	1	6	-	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

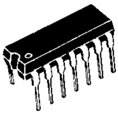


DEFINITIONS

- I_{CCH} — V_{CC} current drain when all gate inputs are high
- I_{CCL} — V_{CC} current drain when all gate inputs are low
- I_{CEX} — Collector-to-emitter leakage of the output transistor
- I_F — Forward current of input diodes which are equal to standard load
- I_{OH} — Current flowing out of the output pin (negative current) at V_{OH}
- I_{OL} — Output current at V_{OL} for rated fan-out
- I_R — Reverse current of input diodes with V_R applied
- I_{SC} — Short-circuit current obtained from device output when one or more inputs are in the low condition
- t_{pd+} — Propagation delay time for a positive-going output pulse
- t_{pd-} — Propagation delay time for a negative-going output pulse
- V_{CC} — Device power supply voltage
- V_{CCH} — High power supply voltage
- V_{CCL} — Low power supply voltage
- V_{CEX} — Collector-to-emitter voltage of the output transistor
- V_F — Forward voltage of input diodes
- V_{IH} — Threshold voltage for high input voltage state
- V_{IL} — Threshold voltage for low input voltage state
- V_{OH} — Output high voltage state with I_{OH} flowing out of pin
- V_{OL} — Output low voltage state with I_{OL} flowing into pin
- V_R — Reverse voltage for input diode leakage test
- V_X — Threshold voltage for low input voltage state on expander unit

MC663P
MC664P

MHTL FLIP-FLOPS

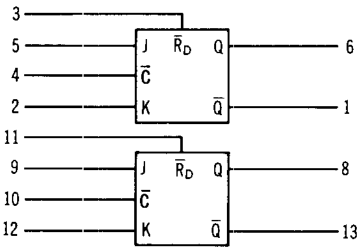


UNIBLOC
PLASTIC PACKAGE
CASE 93

MHTL flip-flops – high-noise-immunity industrial logic circuits for medium-speed digital applications in environments with a high level of electrical noise.

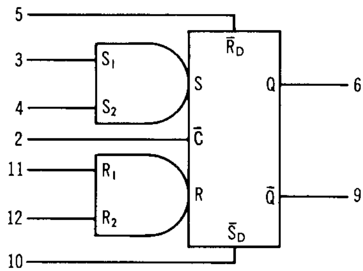
NOISE IMMUNITY = 5 V
TYPICAL LOGIC SWING 13 V
POWER DISSIPATION = 225 mW TYP – MC663P
= 160 mW TYP – MC664P

MC663P
DUAL J-K FLIP-FLOP



Input Loading Factor:
$\bar{C}$ Input = 2
Other Inputs = 1
Output Loading Factor = 9

MC664P
MASTER-SLAVE R-S FLIP-FLOP



Input Loading Factor:
$\bar{C}$ Input = 4
Other Inputs = 1
Output Loading Factor = 8

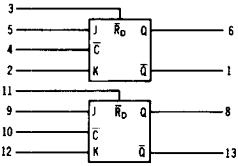
Loading factors are valid from −30°C to +75°C with V_{CC} = 15 ±1 Vdc.

MAXIMUM RATINGS

Rating		Value	Unit
Supply Voltage - Continuous Pulsed, < 1 second		18 20	Vdc
Input Voltage		-1.0/+18.0	Vdc
Output Current (into Outputs)	MC663P MC664P	28 26	mAdc
Input Reverse Current @ 20 V		0.5	mAdc
Operating Temperature Range		-30 to +75	°C
Storage Temperature Range		-55 to +125	°C

MC663P, MC664P (continued)

MC663P



TRUTH TABLE

t_n		t_{n+1}	
J	K	Q	$\bar{Q}$
0	0	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
1	1	$\bar{Q}_n$	Q_n

Direct input ($\bar{R}_D$) must be high.
- 0 = low state
- 1 = high state
- t_n = time period prior to negative transition of clock pulse
- t_{n+1} = time period subsequent to negative transition of clock pulse
- Q_n = state of Q output in time period t_n

NOTE: Clock ($\bar{C}$) input must be low when using direct reset input.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, tests are shown for one flip-flop only. The other flip-flop is tested in a similar manner.

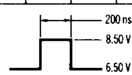
TEST CURRENT / VOLTAGE VALUES (All Temperatures)

mA: I_{OL}	mA: I_{OH}	Volts: V_{IL}	Volts: V_{IH}	Volts: V_F	Volts: V_R	Volts: V_{CCL}	Volts: V_{CCH}
10.8	-0.018	6.50	8.50	0	16.0	14.0	16.0

Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CCL}	V_{CCH}	CP	Ground
Output Voltage	V_{OL}	1	-	1.5	-	1.5	-	1.5	Vdc	1	-	2	3, 5	-	-	-	14	4	7
	V_{OL}	6	-	1.5	-	1.5	-	1.5		6	-	5	2, 3	-	-	-	14	4	7
	V_{OH}	1	-	-	12.5	-	12.5	-		-	1	2, 3	5	-	-	14	-	4	7
	V_{OH}	1	-	-	12.5	-	12.5	-		-	1	5	2, 3	-	-	14	-	4	7
	V_{OH}	6	-	-	12.5	-	12.5	-		-	6	2	3, 5	-	-	14	-	4	7
Short-Circuit Current	I_{SC}	1	-	-	-6.5	-15	-6.5	-15	mAdc	-	-	3, 4	-	-	-	-	14	-	1, 7
Reverse Current	I_R	2	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	2	14	-	-	3, 4, 5, 7
	I_R	3	-	-	-	2.0	-	2.0		-	-	-	-	-	3	2, 4, 5, 14	-	-	7
	$2I_R$	4	-	-	-	4.0	-	4.0		-	-	-	-	-	4	14	-	-	2, 3, 5, 7
	I_R	5	-	-	-	2.0	-	2.0		-	-	-	-	-	5	14	-	-	2, 3, 4, 7
Forward Current	I_F	2	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	2	-	-	4, 14	-	7
	I_F	3	-	-	-	-1.20	-	-1.20		-	-	-	-	3	-	-	14	-	2, 4, 5, 7
	$2I_F$	4	-	-	-	-2.40	-	-2.40		-	-	-	-	4	-	-	2, 5, 14	-	7
	I_F	5	-	-	-	-1.20	-	-1.20		-	-	-	-	5	-	-	4, 14	-	7
Power Drain Current (Both Flip-Flops)	I_{CCL}	14	-	-	-	16.7	-	-	mAdc	-	-	-	-	-	-	-	14	-	2, 3, 4, 5, 7, 9, 10, 11, 12
	I_{CCH}	14	-	-	-	16.7	-	-	mAdc	-	-	-	-	-	-	-	14	-	7

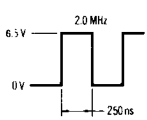
Pins not listed are left open.

Clock Pulse:

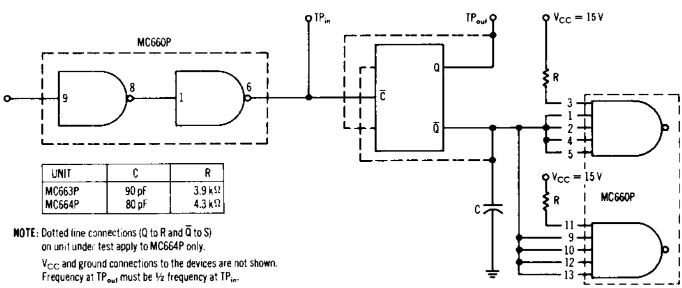


$t_r \leq 1.0\ \mu s$ (10% to 90%)
$t_f \leq 1.0\ \mu s$ (90% to 10%)

TOGGLE MODE TEST CIRCUIT – BOTH TYPES



t_r < 20 ns (10% to 90%)
t_f < 20 ns (90% to 10%)
DUTY CYCLE = 50%

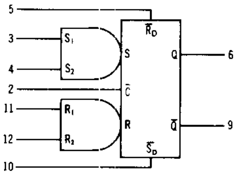


UNIT	C	R
MC663P	90 pF	3.9 kΩ
MC664P	80 pF	4.3 kΩ

NOTE: Dotted line connections (Q to R and $\bar{Q}$ to S) on unit under test apply to MC664P only.
V_{CC} and ground connections to the devices are not shown.
Frequency at TP_{out} must be ½ frequency at TP_{in}.

MC663P, MC664P (continued)

MC664P



DIRECT INPUT OPERATION

$\bar{R}_D$	$\bar{S}_D$	Q	$\bar{Q}$
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	NA	NA

Clock ($\bar{C}$) input must be low
NC = No change
NA = Not allowed

CLOCKED OPERATION

t_n				t_{n+1}
S_1	S_2	R_1	R_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

NOTES FOR CLOCKED-OPERATION TRUTH TABLE:

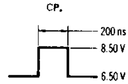
Direct inputs ($\bar{R}_D$, $\bar{S}_D$) must be high.
0 = low state
1 = high state
X = state of input does not affect state of the circuit
U = indeterminate state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	I_{OL} (mA)	I_{OH} (mA)	V_{IL} (Volts)	V_{IH}	V_F	V_R	V_{CCL}	V_{CCH}	CP_a	CP_b	Ground
									TEST CURRENT / VOLTAGE VALUES (All Temperatures)	9.6	-0.016	6.50	8.50	0	16.0	14.0	16.0			
									TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:											
Output Voltage	V_{OL}	6*	-	1.5	-	1.5	-	1.5	Vdc	6	-	2	3, 4, 11, 12	-	-	-	14	-	5	7
	↓	6*	-	↓	-	↓	-	↓	↓	6	-	4	3, 5, 11, 12	-	-	-	14	2	-	7
	↓	6*	-	↓	-	↓	-	↓	↓	6	-	3	4, 5, 11, 12	-	-	-	14	2	-	7
	↓	9‡	-	↓	-	↓	-	↓	↓	9	-	2	3, 4, 11, 12	-	-	-	14	-	10	7
	↓	9‡	-	↓	-	↓	-	↓	↓	9	-	11	3, 4, 10, 12	-	-	-	14	2	-	7
	↓	9‡	-	↓	-	↓	-	↓	↓	9	-	12	3, 4, 10, 11	-	-	-	14	2	-	7
	V_{OH}	6	-	-	12.5	-	12.5	-	↓	-	6	-	5	-	-	14	-	-	-	2, 3, 4, 7, 10, 11, 12
	V_{OH}	9	-	-	12.5	-	12.5	-	↓	-	9	-	10	-	-	14	-	-	-	2, 3, 4, 5, 7, 11, 12
Short-Circuit Current	I_{SC}	6	-	-	-6.5	-15	-6.5	-15	mAdc	-	-	2, 5	10	-	-	-	14	-	-	6, 7, 9
	I_{SC}	9	-	-	-6.5	-15	-6.5	-15	mAdc	-	-	2, 10	5	-	-	-	14	-	-	6, 7, 9
Reverse Current	$4I_R$	2§	-	-	-	8.0	-	8.0	μAdc	-	-	-	5	-	2	14	-	-	-	3, 4, 7, 10, 11, 12
	$4I_R$	2†	-	-	-	8.0	-	8.0	↓	-	-	-	10	-	2	14	-	-	-	3, 4, 5, 7, 11, 12
	I_R	3	-	-	-	2.0	-	2.0	↓	-	-	-	-	-	3	14	-	-	-	2, 4, 7
	↓	4	-	-	-	↓	-	↓	↓	-	-	-	-	-	4	14	-	-	-	2, 3, 7
	↓	5	-	-	-	↓	-	↓	↓	-	-	-	2, 11, 12	-	5	14	-	-	-	7
	↓	10	-	-	-	↓	-	↓	↓	-	-	-	2, 3, 4	-	10	14	-	-	-	7
	↓	11	-	-	-	↓	-	↓	↓	-	-	-	-	-	11	14	-	-	-	2, 7, 12
	↓	12	-	-	-	↓	-	↓	↓	-	-	-	-	-	12	14	-	-	-	2, 7, 11
Forward Current	$4I_F$	2	-	-	-	-4.80	-	-4.80	mAdc	-	-	-	5	2	3, 4, 11, 12	-	14	-	-	7, 10
	$4I_F$	2	-	-	-	-4.80	-	-4.80	↓	-	-	-	10	2	3, 4, 11, 12	-	14	-	-	5, 7
	I_F	3	-	-	-	-1.20	-	-1.20	↓	-	-	-	-	3	2, 4	-	14	-	-	7
	↓	4	-	-	-	↓	-	↓	↓	-	-	-	-	4	2, 3	-	14	-	-	7
	↓	5	-	-	-	↓	-	↓	↓	-	-	-	-	5	-	-	14	-	-	2, 7, 10, 11, 12
	↓	10	-	-	-	↓	-	↓	↓	-	-	-	-	10	-	-	14	-	-	2, 3, 4, 5, 7
	↓	11	-	-	-	↓	-	↓	↓	-	-	-	-	11	2, 12	-	14	-	-	7
	↓	12	-	-	-	↓	-	↓	↓	-	-	-	-	12	2, 11	-	14	-	-	7
Power Drain Current	I_{CCL}	14	-	-	-	14.5	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	2, 3, 4, 5, 7, 10, 11, 12
	I_{CCH}	14	-	-	-	14.5	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	7

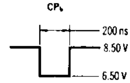
Pins not listed are left open.
*Apply momentary ground to pins 9 and 10 prior to clock pulse
‡Apply momentary ground to pins 5 and 6 prior to clock pulse
§Apply momentary ground to pin 9
†Apply momentary ground to pin 6

CP_a



$t_r \leq 1.0\ \mu s$ (10% to 90%)
$t_f \leq 1.0\ \mu s$ (90% to 10%)

CP_b



$t_r \leq 1.0\ \mu s$ (10% to 90%)
$t_f < 1.0\ \mu s$ (90% to 10%)

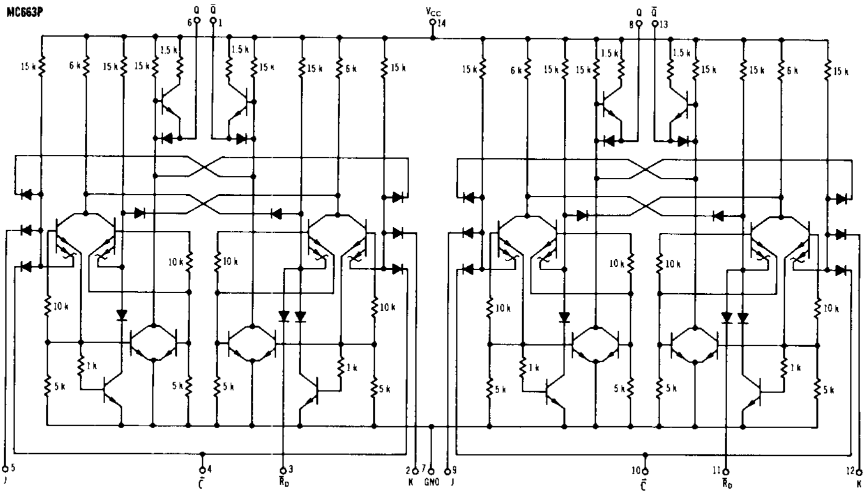
DEFINITIONS

CP	Clock Pulse
I_{CCH}	V_{CC} current drain when all flip-flop inputs are high
I_{CCL}	V_{CC} current drain when all flip-flop inputs are low
I_F	Forward current of input diodes which are equal to standard load
$2\ I_F$	Forward current of input diodes which are equal to twice standard load
I_{OH}	Current flowing out of the output pin (negative current) at V_{OH}
I_{OL}	Output current at V_{OL} for rated fan-out
I_R	Reverse current of input diodes with V_R applied
$2\ I_R$	Reverse current of input diodes which are equal to twice standard load, with V_R applied
I_{SC}	Short-circuit current obtained from device output. Flip-flop is set and held to keep output sinking transistor off during the test.
V_{CC}	Device power supply voltage
V_{CCH}	High power supply voltage
V_{CCL}	Low power supply voltage
V_F	Forward voltage of input diodes
V_{IH}	Threshold voltage for high input voltage state
V_{IL}	Threshold voltage for low input voltage state
V_{OH}	Output high voltage state with I_{OH} flowing out of pin
V_{OL}	Output low voltage state with I_{OL} flowing into pin
V_R	Reverse voltage for input diode leakage test

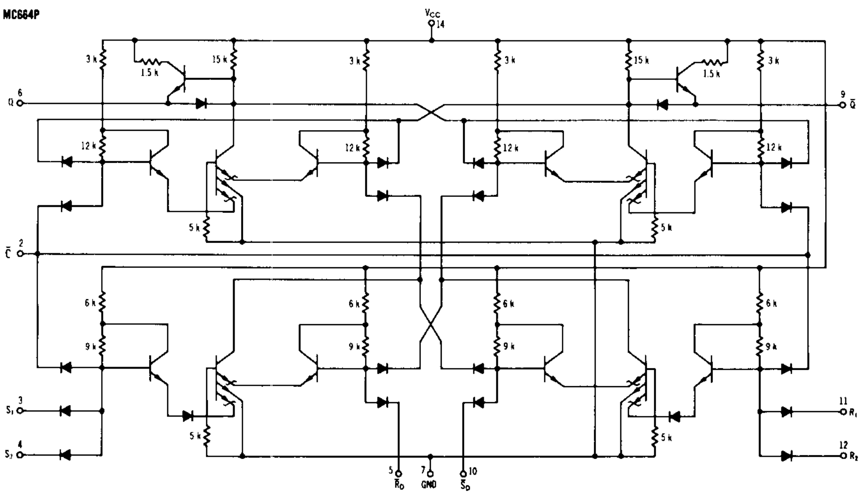
MC663P, MC664P (continued)

CIRCUIT SCHEMATICS

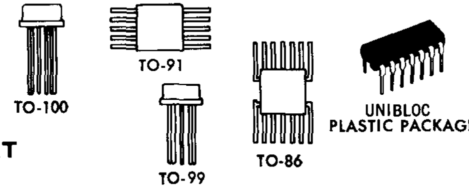
MC663P



MC664P



MRTL
INTEGRATED CIRCUITS



PACKAGE CROSS REFERENCE CHART

Introduction of the MRTL line of integrated circuits in flat packages makes this device line available in three basic housings – metal can, plastic, and flat packages. The following charts permit conversion of information published on devices in metal can or plastic packages to the pin configuration of the flat packages.

Flat Package Type Number			Description		Refer to Conversion Chart
MC700F	MC800F	MC900F	Medium Power	Buffer	A
MC703F	MC803F	MC903F	Medium Power	3-Input Gate	A
MC704F	MC804F	MC904F	Medium Power	Half Adder	A
MC705F	MC805F	MC905F	Medium Power	Half Shift Register, w/ Inverter	A
MC706F	MC806F	MC906F	Medium Power	Half Shift Register, w/o Inverter	A
MC707F	MC807F	MC907F	Medium Power	4-Input Gate	A
MC708F	MC808F	MC908F	Milliwatt	Half Adder	C
MC709F	MC809F	MC909F	Milliwatt	Buffer	C
MC710F	MC810F	MC910F	Milliwatt	Dual 2-Input Gate	C
MC711F	MC811F	MC911F	Milliwatt	4-Input Gate, w/ Inverter	C
MC712F	MC812F	MC912F	Milliwatt	Half Adder	C
MC713F	MC813F	MC913F	Milliwatt	Type D Flip Flop	C
MC714F	MC814F	MC914F	Medium Power	Dual 2-Input Gate	A
MC715F	MC815F	MC915F	Medium Power	Dual 3-Input Gate	B
-	MC816F	MC916F	Medium Power	J-K Flip Flop	A
MC717F	MC817F	MC917F	Milliwatt	Quad 2-Input Gate	E
MC716F	MC818F	MC918F	Milliwatt	Dual 3-Input Gate	D
MC719F	MC619F	MC919F	Milliwatt	Dual 4-Input Gate	E
MC720F	MC820F	MC920F	Milliwatt	J-K Flip Flop	C
MC721F	MC821F	MC921F	Milliwatt	Gate Expander	C
MC722F	MC622F	MC922F	Milliwatt	J-K Flip Flop	B
MC723F	-	-	Medium Power	J-K Flip Flop	A
MC724F	MC824F	MC924F	Medium Power	Quad 2-Input Gate	E
MC725F	MC825F	MC925F	Medium Power	Dual 4-Input Gate	E
MC726F	MC826F	MC926F	Medium Power	J-K Flip Flop	B
MC727F	MC827F	MC927F	Medium Power	Quad Inverter	B
MC726F	MC628F	MC928F	Milliwatt	5-Input Gate	C
MC729F	MC829F	MC929F	Medium Power	5-Input Gate	A
MC776F	MC676F	MC976F	Milliwatt	Dual J-K Flip Flop	E
MC776F	MC878F	MC978F	Milliwatt	Dual Type D Flip Flop	E
MC765F	MC885F	MC985F	Medium Power	Quad 2-Input Expander	E
MC786F	MC886F	MC986F	Medium Power	Dual 4-Input Expander	E
MC788F	MC888F	MC968F	Medium Power	Dual 3-Input Buffer	E
MC769F	MC889F	MC989F	Medium Power	Hex Inverter	E
MC790F	MC890F	MC990F	Medium Power	Dual J-K Flip Flop	E
MC792F	MC892F	MC992F	Medium Power	Triple 3-Input Gate	E
MC793F	MC893F	MC993F	Milliwatt	Triple 3-Input Gate	E
MC798F	MC898F	MC998F	Milliwatt	Dual Buffer	E
MC799F	MC899F	MC999F	Medium Power	Dual Buffer	B

CONVERSION CHARTS

A

TO-99 Pin No.	1	2	3	4	5	6	7	9
TO-91 Pin No.	2	3	4	5	7	6	9	18

B

TO-100 Pin No.	1	2	3	4	5	8	7	8	9	18
TO-91 Pin No.	1	2	3	4	5	6	7	8	9	18

C

TO-99 Pin No.	1	2	3	4	5	6	7	8
TO-91 Pin No.	1	2	4	5	6	7	9	10

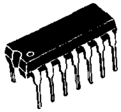
D

TO-100 Pin No.	1	2	3	4	5	6	7	8	9	10
TO-91 Pin No.	1	2	3	9	5	4	6	7	6	10

E

Unibloc Pin No.	1	2	3	4	5	8	7	8	9	18	11	12	13	14
TO-88 Pin No.	4	5	6	7	8	9	18	11	12	13	14	1	2	3

MC700P SERIES
MRTL (milliwatt and medium power)



UNIBLOC
PLASTIC PACKAGE
CASE 93

Both milliwatt MRTL (low power) and MRTL (medium power) devices designed for use in commercial-industrial applications. Circuit loading is guaranteed over a temperature range of +15°C to +55°C. Features dual in-line pin arrangement for automatic insertion and one-piece, injection-molded plastic Unibloc package.

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Logic Input Voltage		±4	Vdc
Power Supply Voltage (Pulsed ≤ 1 second)		+12	Vdc
Operating Temperature Range	T_A	+15 to +55	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Milliwatt MRTL			MRTL			Unit
	+15°C	+25°C	+55°C	+15°C	+25°C	+55°C	
I_{A3}	0.420	0.420	0.420	—	—	—	mAdc min
I_{A4}	0.570	0.570	0.570	—	—	—	mAdc min
I_{A10}	—	—	—	1.65	1.65	1.56	mAdc min
I_{A13}	—	—	—	2.15	2.15	2.03	mAdc min
I_{A16}	—	—	—	2.65	2.65	2.5	mAdc min
I_{AB}	5.0	5.0	5.0	13.5	13.75	12.5	mAdc min
I_{CEX}	50	50	100	225	225	250	μAdc max
I_{in}	0.150	0.150	0.150	0.500	0.500	0.470	mAdc max
$2 I_{in}$	0.300	0.300	0.300	1.0	1.0	0.94	mAdc max
V_{out}	0.400	0.300	0.320	0.400	0.300	0.320	Vdc max
V_{CE}	0.220	0.230	0.320	0.300	0.290	0.320	Vdc max

TEST CONDITIONS

V_{BOT}	1.8	1.8	1.8	1.8	1.8	1.8	Vdc
V_{CC}	3.6	3.6	3.6	3.6	3.6	3.6	Vdc
V_{in}	0.865	0.850	0.800	0.865	0.850	0.800	Vdc
V_{off}	0.475	0.460	0.430	0.475	0.460	0.430	Vdc
V_{on}	0.865	0.850	0.800	0.865	0.850	0.800	Vdc
V_R*	4600	4800	5000	640	640	640	Ohms

*Resistor value to V_{CC}

MC700P SERIES (continued)

MEDIUM POWER MRTL

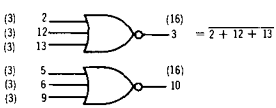
LOGIC DESCRIPTION

The logic diagrams shown describe the MC700P Series of medium-power resistor-transistor logic integrated circuits and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (if on the circuit input terminal) or load driving ability — fan-out — (if on the circuit output terminal).

Using the indicated loading factors, these medium-power MRTL circuits are compatible with the low-power mW MRTL circuits shown on page 19 The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. The loading data is valid over the temperature range of +15 to +55°C with V_{CC} = 3.6 V ±10%.

All elements in the MC700P Series operate with V_{CC} applied to pin 11 and ground connected to pin 4.

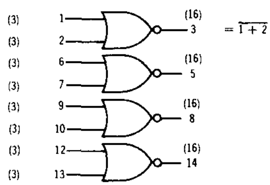
MC715P — DUAL 3-INPUT GATE



t_{pd} = 12 ns

P_D = 55 mW (Inputs High)
15 mW (Inputs Low)

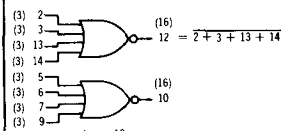
MC724P — QUAD 2-INPUT GATE



t_{pd} = 12 ns

P_D = 100 mW (Inputs High)
30 mW (Inputs Low)

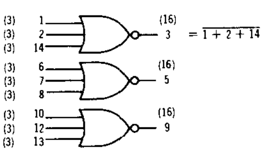
MC725P DUAL 4-INPUT GATE



t_{pd} = 12 ns

P_D = 60 mW (Inputs High)
15 mW (Inputs Low)

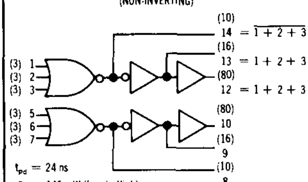
MC792P — TRIPLE 3-INPUT GATE



t_{pd} = 12 ns

P_D = 82 mW (Inputs High)
24 mW (Inputs Low)

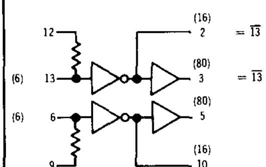
MC788P — DUAL 3-INPUT DUFFER
(NON-INVERTING)



t_{pd} = 24 ns
P_D = 145 mW (Inputs High)
56 mW (Inputs Low)

Outputs 12, 13, or 14 may not be used simultaneously.
Outputs 8,9, or 10 may not be used simultaneously.

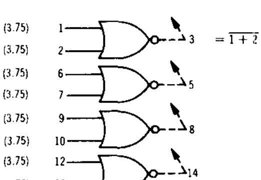
MC799P — DUAL BUFFER



t_{pd} = 15 ns
P_D = 50 mW (Inputs High)
90 mW (Inputs Low)

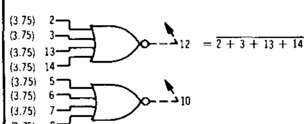
Outputs 2 and 3 may not be used simultaneously.
Outputs 5 and 10 may not be used simultaneously.

MC785P — QUAD 2-INPUT EXPANDER



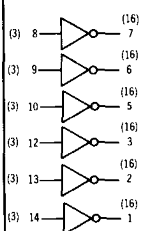
t_{pd} = 12 ns
P_D = 20 mW (Inputs High)
Negligible (Inputs Low)

MC786P — DUAL 4-INPUT EXPANDER



t_{pd} = 12 ns
P_D = 20 mW (Inputs High)
Negligible (Inputs Low)

MC789P — HEX INVERTER

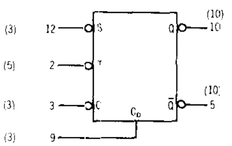


t_{pd} = 12 ns
P_D = 130 mW (Inputs High)
15 mW (Inputs Low)

MC700P SERIES (continued)

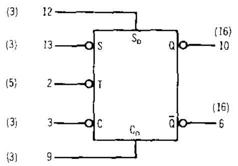
MEDIUM POWER MRTL (continued)

MC723P — J-K FLIP-FLOP



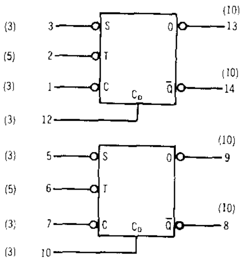
f_{Tog} = 4 MHz
P_D = 91 mW (Only Clock Input High)
79 mW (Inputs Low)

MC726P — J-K FLIP-FLOP



f_{Tog} = 4 MHz
P_D = 100 mW (Only Clock Input High)
86 mW (Inputs Low)

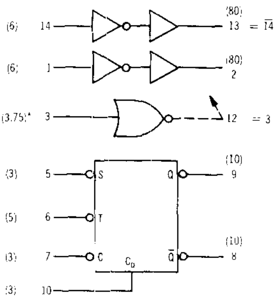
MC790P — DUAL J-K FLIP-FLOP



f_{Tog} = 4 MHz
P_D = 182 mW (Only Clock Input High)
158 (Inputs Low)

MC779P — MULTIFUNCTION

(1 J-K FLIP-FLOP, 1 EXPANDER, 2 BUFFERS)



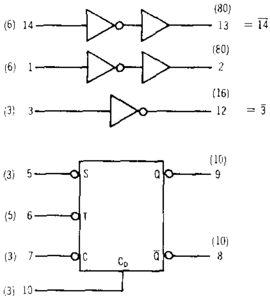
	f_{Tog} MHz	t_{pd} ns	P_D mW	
			(Inputs High)	(Inputs Low)
FLIP-FLOP	4	—	91‡	79
EACH BUFFER	—	15	25	45
EXPANDER	—	12	2.5	Negligible

*Input loading factor 3.75 if pin 12 is tied to pin 8 or pin 9 on the same package.

‡Only Clock Input High

MC787P — MULTIFUNCTION

(1 J-K FLIP-FLOP, 1 INVERTER, 2 BUFFERS)



	f_{Tog} MHz	t_{pd} ns	P_D mW	
			(Inputs High)	(Inputs Low)
FLIP-FLOP	4	—	91‡	79
EACH BUFFER	—	15	25	45
INVERTER	—	12	22	8

‡Only Clock Input High

J-K FLIP-FLOP TRUTH TABLES

DIRECT INPUT OPERATION (MC726P only)

S_D	C_D	Q	$\bar{Q}$
0	0	[illegible]	[illegible]
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION (all types)

t_n		t_{n+1}	
S	C	Q	$\bar{Q}$
1	1	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.

MC700P SERIES (continued)

MILLIWATT MRTL

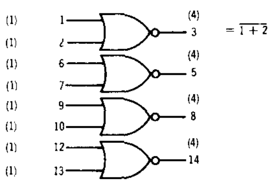
LOGIC DESCRIPTION

The logic diagrams shown describe the MC700P Series of low-power resistor-transistor logic integrated circuits and permit quick selection of those circuits required for the implementation of a system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (if on the circuit input terminal) or load driving ability — fan-out — (if on the circuit output terminal).

Using the indicated loading factors, these low-power mW MRTL circuits are compatible with the medium-power MRTL circuits shown on pages 17 and 18. The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output. The loading data is valid over the temperature range of +15 to +55°C with V_{CC} = 3.6 V ±10%.

All elements in the MC700P Series operate with V_{CC} applied to pin 11 and ground connected to pin 4.

MC717P — QUAD 2-INPUT GATE

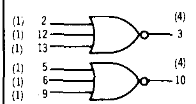


$= \overline{1+2}$

t_{pd} = 27 ns

P_D = 20 mW (Inputs High)
12 mW (Inputs Low)

MC718P — DUAL 3-INPUT GATE

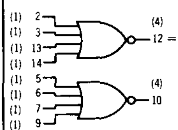


$= \overline{2+12+13}$

t_{pd} = 27 ns

P_D = 12 mW (Inputs High)
6 mW (Inputs Low)

MC719P — DUAL 4-INPUT GATE

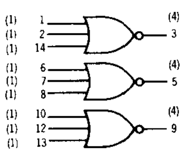


$12 = \overline{2+3+13+14}$

t_{pd} = 27 ns

P_D = 13 mW (Inputs High)
6 mW (Inputs Low)

MC793P — TRIPLE 3-INPUT GATE

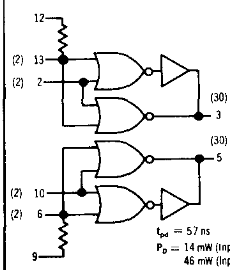


$= \overline{1+2+14}$

t_{pd} = 27 ns

P_D = 18 mW (Inputs High)
9 mW (Inputs Low)

MC798P — DUAL 2-INPUT BUFFER

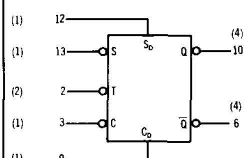


$3 = \overline{2+13}$

t_{pd} = 57 ns

P_D = 14 mW (Inputs High)
46 mW (Inputs Low)

MC722P — J-K FLIP-FLOP



f_{Tog} = 1 MHz

P_D = 35 mW (Only Clock Input High)
18 mW (Inputs Low)

DIRECT INPUT OPERATION(1)

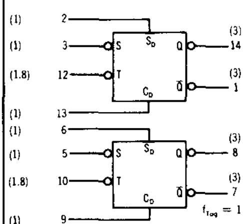
S_D	C_D	Q	$\bar{Q}$
0	0	(2)	(2)
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION(3)

t_n(4)		t_{n+1}(4)	
S	C	Q	$\bar{Q}$
1	1	Q_n(5)	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n(5)

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (S_D and C_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.

MC778P — DUAL TYPE "D" FLIP-FLOP



f_{Tog} = 1 MHz

P_D = 40 mW (Direct Set, S_D, and Direct Clear, C_D, Low; all other inputs high)
35 mW (All Inputs Low)

DIRECT INPUT OPERATION(1)

S_D	C_D	Q	$\bar{Q}$
0	0	(2)	(2)
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION(3)

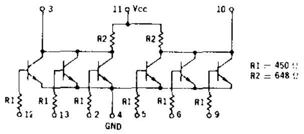
t_n(4)	t_{n+1}(4)	
S	Q	$\bar{Q}$
1	1	0
0	0	1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (S_D and C_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.

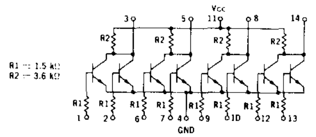
MC700P SERIES (continued)

CIRCUIT SCHEMATICS

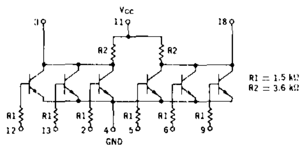
MC715P — DUAL 3-INPUT GATE



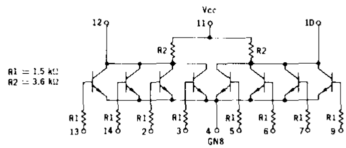
MC717P — QUAD 2-INPUT GATE



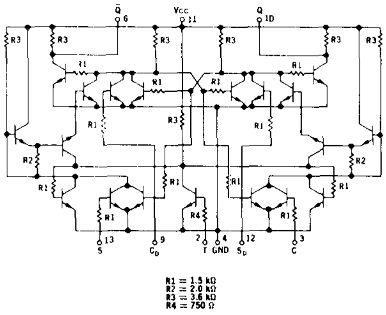
MC718P — DUAL 3-INPUT GATE



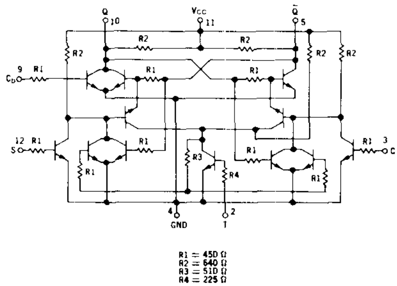
MC719P — DUAL 4-INPUT GATE



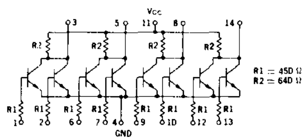
MC722P — J-K FLIP-FLOP



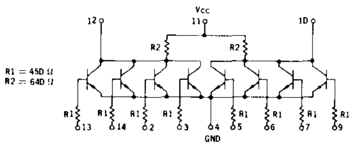
MC723P — J-K FLIP-FLOP



MC724P — QUAD 2-INPUT GATE



MC725P DUAL 4-INPUT GATE

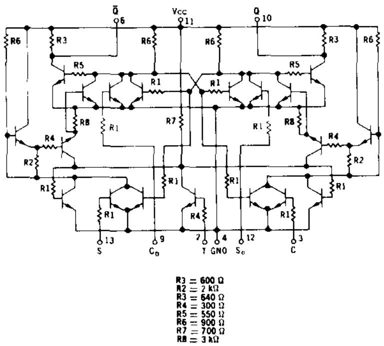


RESISTOR VALUES ARE TYPICAL.

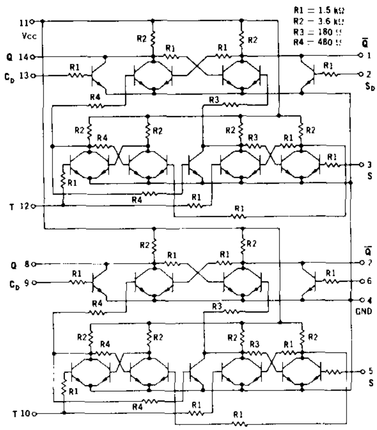
MC700P SERIES (continued)

CIRCUIT SCHEMATICS

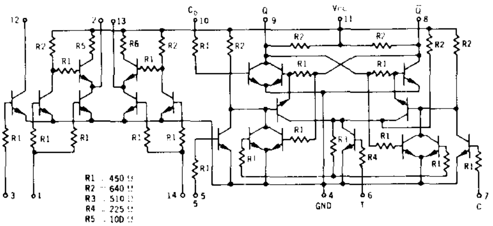
MC726P — J-K FLIP-FLOP



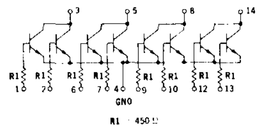
MC778P — DUAL TYPE "D" FLIP-FLOP



MC779P — MULTIFUNCTION (1 J-K FLIP-FLOP, 1 EXPANDER, 2 BUFFERS)

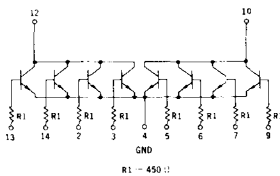


MC785P — QUAD 2-INPUT EXPANDER



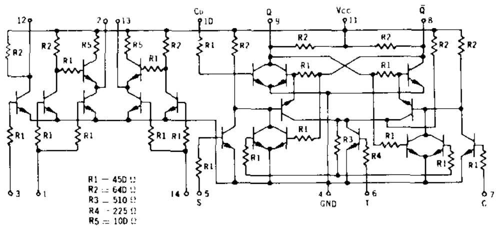
V_{CC} connection to pin 11 not shown

MC786P — DUAL 4-INPUT EXPANDER



V_{CC} connection to pin 11 not shown

MC787P — MULTIFUNCTION (1 J-K FLIP-FLOP, 1 INVERTER, 2 BUFFERS)

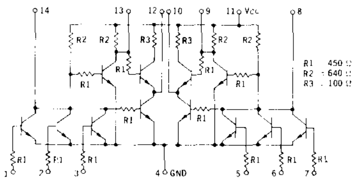


RESISTOR VALUES ARE TYPICAL.

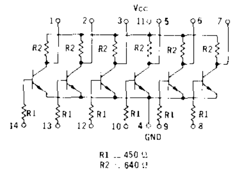
MC700P SERIES (continued)

CIRCUIT SCHEMATICS

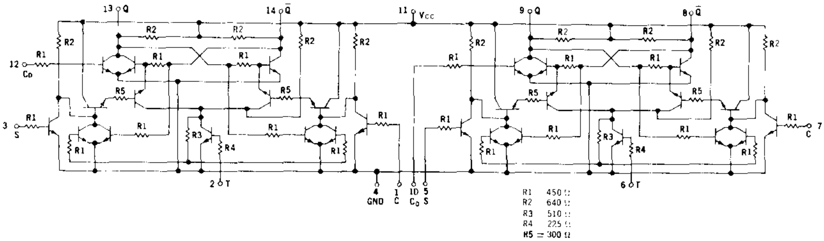
MC788P — DUAL 3-INPUT BUFFER
(NON-INVERTING)



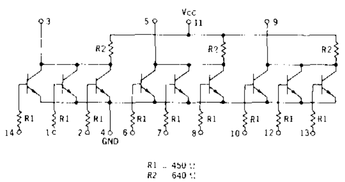
MC789P — HEX INVERTER



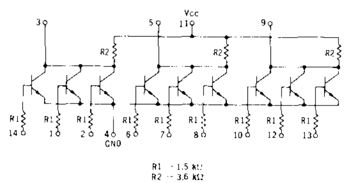
MC790P — DUAL J-K FLIP-FLOP



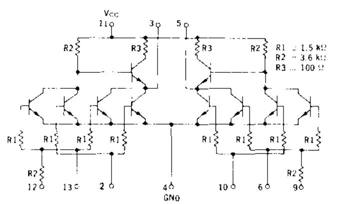
MC792P — TRIPLE 3-INPUT GATE



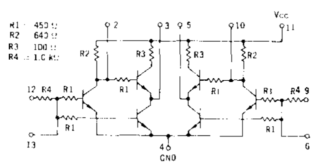
MC793P — TRIPLE 3-INPUT GATE



MC798P — DUAL 2-INPUT BUFFER



MC799P — DUAL BUFFER



RESISTOR VALUES ARE TYPICAL.

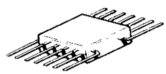
DEFINITIONS

I_{A3}, I_{A4}, I_{A10}, I_{A13}, I_{A16}	Minimum available output current from a device with an output loading factor of 3, 4, 10, 13, and 16 respectively. Output voltage not to fall below the value of V_{in}.
I_{AB}	Minimum available output current from a buffer. Output voltage not to fall below the value of V_{in}.
I_{CEX}	Collector current of gate expander when V_{in} is applied to the output pin and V_{off} is applied to the input pins.
I_{in}	Maximum input current drawn by one input of a gate with V_{in} applied. All other gate inputs are returned to V_{BOT}.
$2\ I_{in}$	Maximum input current drawn by one input of the MC798P or MC799P buffers with V_{in} applied. The other input is returned to V_{BOT}.
V_{BOT}	A high-value voltage applied to an input of a device to insure saturation of the driven transistor.
V_{CC}	Supply voltage.
V_{CE}	Maximum saturation voltage with V_{BOT} applied to the input.
V_{in}	Minimum high-level voltage applied to the input of a device.
V_{off}	The maximum voltage which may be applied to an input terminal without turning the transistor on.
V_{on}	The minimum voltage which may be applied to an input terminal that will turn the transistor on.
V_{out}	The maximum output voltage with V_{on} applied to the input.
V_R	Value of external resistor connected to V_{CC} for test purposes.

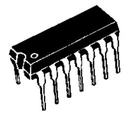
GENERAL RULES

1. The number of load circuits that may be driven from an output is determined by the input loading factor. The summation of input loading should not exceed the drive capability of the output.
2. All unused inputs should be returned to ground.
3. Expander Rules:
   (1) The MC785P and MC786P MRTL expanders can be used to expand medium-power MRTL output nodes only.
   (2) Subtract 2 from the output loading factor of the MRTL expanded gate for each expander node that is connected.
   (3) The input loading factor of the MRTL expanded gate must be increased to 3.75.
4. Clock pulse (T) inputs to flip-flops must have a fall time within the range of 10 ns to 100 ns. Fall time is a straight-line function from 1 V to ground. (Not applicable to MC778P.)

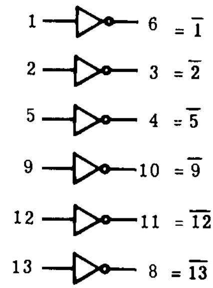
MC934F
MC834F, P



TO-86
CASE 83
SUFFIX F

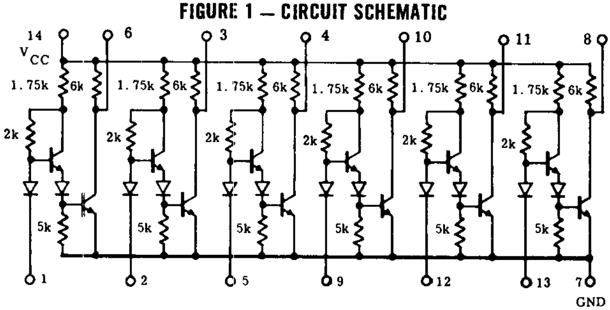


UNIBLOC
PLASTIC PACKAGE
CASE 93
SUFFIX P



MDTL HEX INVERTER (Additions to MC930/MC830 Series)

FIGURE 1 — CIRCUIT SCHEMATIC



t_{pd} = 30 ns Typ.
P_D = 66 mW Typ.
Input Loading Factor = Fan-Out = 8

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one inverter only.

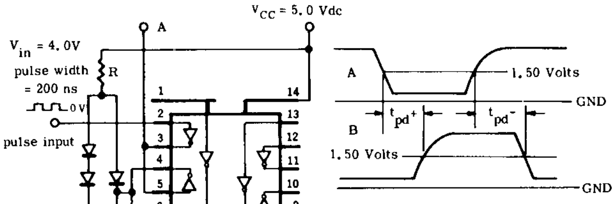
Other inverters are tested in the same manner.

CHARACTERISTIC	SYMBOL PIN IN ( )	MC934F TEST LIMITS -55°C MIN	MC934F -55°C MAX	MC934F +25°C MIN	MC934F +25°C MAX	MC934F +125°C MIN	MC934F +125°C MAX	UNIT	MC834F, P TEST LIMITS 0°C MIN	MC834F, P 0°C MAX	MC834F, P +25°C MIN	MC834F, P +25°C MAX	MC834F, P +75°C MIN	MC834F, P +75°C MAX	UNIT
Output Voltage	$V_{OL(4)}$	—	0.40	—	0.40	—	0.45	Vdc	—	0.45	—	0.45	—	0.50	Vdc
	$V_{OH(4)}$	2.50	—	2.60	—	2.50	—	Vdc	2.60	—	2.60	—	2.50	—	Vdc
Short-Circuit Current	$I_{SC(4)}$	—	-1.34	—	-1.34	—	-1.30	mAdc	—	-1.30	—	-1.30	—	-1.25	mAdc
Reverse Current	$I_{R(5)}$	—	2.0	—	2.0	—	5.0	µAdc	—	5.0	—	5.0	—	10.0	µAdc
Output Leakage Current	$I_{CEX(4)}$	—	—	—	50	—	—	µAdc	—	—	—	100	—	—	µAdc
Forward Current	$I_{F(5)}$	—	-1.60	—	-1.60	—	-1.50	mAdc	—	-1.40	—	-1.40	—	-1.33	mAdc
Power Drain Current	$I_{PDH(14)}$	—	—	—	19.5	—	—	mAdc	—	—	—	24	—	—	mAdc
	$I_{MAX(14)}$	—	—	—	16.5	—	—	mAdc	—	—	—	24	—	—	mAdc
Switching Time (Pin 3 connected to Pin 5)	t_{pd+}	—	—	25	80	—	—	ns	—	—	25	80	—	—	ns
	t_{pd-}	—	—	10	30	—	—	ns	—	—	10	30	—	—	ns

Pins not listed are left open.

MC934/MC834 (continued)

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



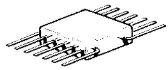
TEST	R	C
t_{pd}^{+}	3.90k ohms	30 pf
t_{pd}^{-}	400 ohms	50 pf

NOTE: All diodes are MC833 or equivalent

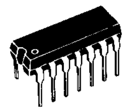
	@ Test Temperature	TEST CONDITIONS mA		Volts										
MC934F	-55°C	11.4	-0.12	1.40	2.10	0	4.00	---	---	4.50	5.50	--	---	
	+25°C	12.0	-0.12	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	5.00	8.00	
	+125°C	10.8	-0.12	0.80	2.00	0	4.00	---	---	4.50	5.50	---	---	
MC834F,P	0°C	12.0	-0.12	1.20	2.00	0.45	4.00	---	---	5.00	5.00	---	---	
	+25°C	12.0	-0.12	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	5.00	8.00	
	+75°C	11.4	-0.12	0.95	1.80	0.50	4.00	---	---	5.00	5.00	---	---	
CHARACTERISTIC	**SYMBOL PIN IN ( )**	I_{DL} PIN	I_{OH} PIN	V_{IL} PIN	V_{IH} PIN	V_F PIN	V_R PIN	V_{CEX} PIN	V_{CC} PIN	V_{CCL} PIN	V_{CCH} PIN	V_{PD} PIN	V_{MAX} PIN	**GROUNDED PIN**
Output Voltage	$V_{OL(4)}$	4			5					14				7
	$V_{OH(4)}$		4	5						14				7
Short-Circuit Current	$I_{SC(4)}$										14			4,5,7
Reverse Current	$I_{R(5)}$						5				14			7
Output Leakage Current	$I_{CEX(4)}$							4,14						5,7
Forward Current	$I_{F(5)}$					5					14			7
Power Drain Current	$I_{PDH(14)}$											14		7
	$I_{MAX(14)}$												14	1,2,5,7,9,12,13
Switching Time (Pin 3 connected to Pin 5)		Pulse In	Pulse Out											
	t_{pd+}	5	4						14					7
	t_{pd-}	5	4						14					7

Pins not listed are left open.

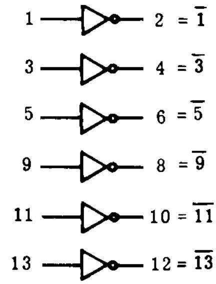
MC936F
MC836F, P



TO-86
CASE 83
SUFFIX F



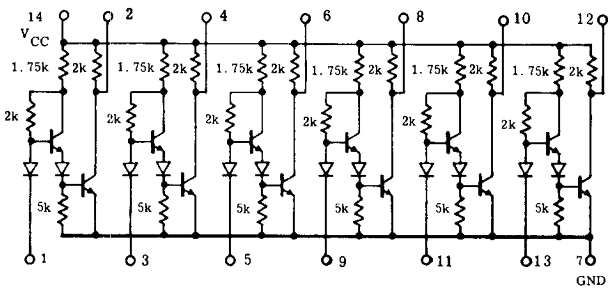
UNIBLOC
PLASTIC PACKAGE
CASE 93
SUFFIX P



MDTL HEX INVERTER (Additions to MC930/ MC830 Series)

t_{pd} = 30 ns Typ.
P_D = 66 mW Typ.
Input Loading Factor = 1
Fan-Out = 8

FIGURE 1 — CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

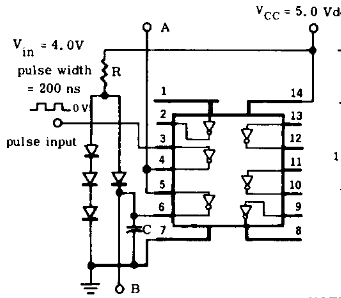
Test procedures are shown for one inverter only.
Other inverters are tested in the same manner.

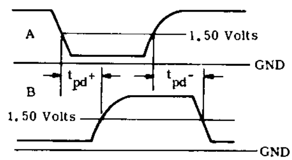
CHARACTERISTIC	SYMBOL PIN IN ( )	MC936F TEST LIMITS -55°C MIN	-55°C MAX	+25°C MIN	+25°C MAX	+125°C MIN	+125°C MAX	UNIT	MC836F, P TEST LIMITS 0°C MIN	0°C MAX	+25°C MIN	+25°C MAX	+75°C MIN	+75°C MAX	UNIT
Output Voltage	$V_{OL(6)}$	---	0.40	---	0.40	---	0.45	Vdc	---	0.45	---	0.45	---	0.50	Vdc
	$V_{OH(6)}$	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
Short-Circuit Current	$I_{SC(6)}$	---	-1.34	---	-1.34	---	-1.30	mAdc	---	-1.30	---	-1.30	---	-1.25	mAdc
Reverse Current	$I_{R(5)}$	---	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10.0	μAdc
Output Leakage Current	$I_{CEX(6)}$	---	---	---	50	---	---	μAdc	---	---	---	100	---	---	μAdc
Forward Current	$I_{F(5)}$	---	-1.60	---	-1.60	---	-1.50	mAdc	---	-1.40	---	-1.40	---	-1.33	mAdc
Power Drain Current	$I_{PDH(14)}$	---	---	---	19.5	---	---	mAdc	---	---	---	24	---	---	mAdc
	$I_{MAX(14)}$	---	---	---	16.5	---	---	mAdc	---	---	---	24	---	---	mAdc
Switching Time (Pin 4 connected to Pin 5)	t_{pd+}	---	---	25	80	---	---	ns	---	---	25	80	---	---	ns
	t_{pd-}	---	---	10	30	---	---	ns	---	---	10	30	---	---	ns

Pins not listed are left open.

MC936F/MC836F, P (continued)

FIGURE 2 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





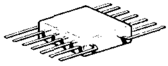
TEST	R	C
t_{pd}^{+}	3.90k ohms	30 pf
t_{pd}^{-}	400 ohms	50 pf

NOTE: All diodes are MC833 or equivalent

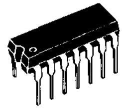
@ Test Temperature		TEST CONDITIONS mA		VOLTS										
MC936F	-55°C	11.4	-0.12	1.40	2.10	0	4.00	---	---	4.50	5.50	---	---	
	+25°C	12.0	-0.12	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	5.00	8.00	
	+125°C	10.8	-0.12	0.80	2.00	0	4.00	---	---	4.50	5.50	---	---	
MC836F,P	0°C	12.0	-0.12	1.20	2.00	0.45	4.00	---	---	5.00	5.00	---	---	
	+25°C	12.0	-0.12	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	5.00	8.00	
	+75°C	11.4	-0.12	0.95	1.80	0.50	4.00	---	---	5.00	5.00	---	---	
CHARACTERISTIC	**SYMBOL PIN IN ( )**	I_{OL} PIN	I_{OH} PIN	V_{IL} PIN	V_{IH} PIN	V_F PIN	V_R PIN	V_{CEX} PIN	V_{CC} PIN	V_{CCL} PIN	V_{CCH} PIN	V_{PD} PIN	V_{MAX} PIN	**GROUNDED PIN**
Output Voltage	$V_{OL(6)}$	6			5					14				7
	$V_{OH(6)}$		6	5						14				7
Short-Circuit Current	$I_{SC(6)}$										14			5,6,7
Reverse Current	$I_{R(5)}$						5				14			7
Output Leakage Current	$I_{CEX(6)}$							6,14						5,7
Forward Current	$I_{F(5)}$					5					14			7
Power Drain Current	$I_{PDH(14)}$											14		7
	$I_{MAX(14)}$												14	1,3,5,7,9,11,13
Switching Time		Pulse In	Pulse Out											
(Pin 4 connected to Pin 5)	t_{pd+}	5	6						14					7
	t_{pd-}	5	6						14					7

Pins not listed are left open.

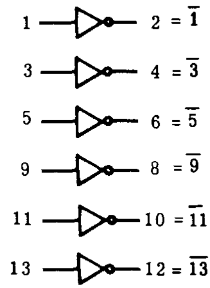
MC937F
MC837F, P



TO-86
CASE 83
SUFFIX F



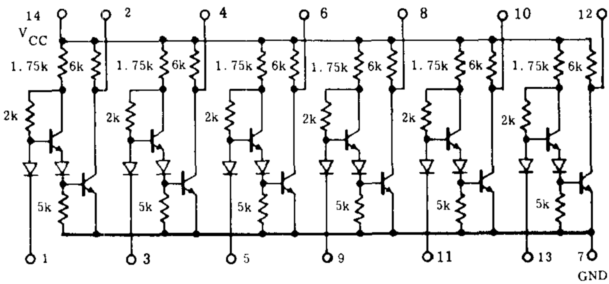
UNIBLOC
PLASTIC PACKAGE
CASE 93
SUFFIX P



MDTL HEX INVERTER (Additions to MC930/ MC830 Series)

t_{pd} = 25 ns Typ.
P_D = 90 mW Typ.
Input Loading Factor = 1
Fan-Out = 7

FIGURE 1 — CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

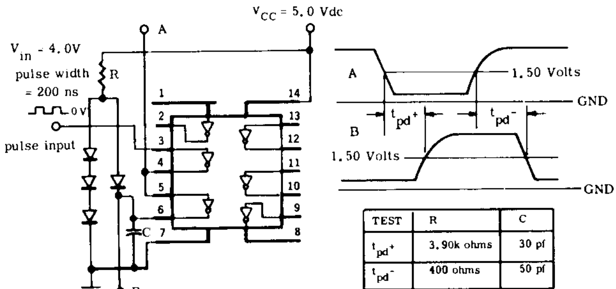
Test procedures are shown for one inverter only.
Other inverters are tested in the same manner.

CHARACTERISTIC	SYMBOL PIN IN ( )	MC937F TEST LIMITS -55°C MIN	-55°C MAX	+25°C MIN	+25°C MAX	+125°C MIN	+125°C MAX	UNIT	MC837F,P TEST LIMITS 0°C MIN	0°C MAX	+25°C MIN	+25°C MAX	+75°C MIN	+75°C MAX	UNIT
Output Voltage	$V_{OL(6)}$	---	0.40	---	0.40	---	0.45	Vdc	---	0.45	---	0.45	---	0.50	Vdc
	$V_{OH(6)}$	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
Short-Circuit Current	$I_{SC(6)}$	---	-4.0	---	-4.0	---	-3.9	mAdc	---	-3.9	---	-3.9	---	-3.75	mAdc
Reverse Current	$I_{R(5)}$	---	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10.0	μAdc
Output Leakage Current	$I_{CEX(6)}$	---	---	---	50	---	---	μAdc	---	---	---	100	---	---	μAdc
Forward Current	$I_{F(5)}$	---	-1.60	---	-1.60	---	-1.50	mAdc	---	-1.40	---	-1.40	---	-1.33	mAdc
Power Drain Current	$I_{PDH(14)}$	---	---	---	32.0	---	---	mAdc	---	---	---	39	---	---	mAdc
	$I_{MAX(14)}$	---	---	---	16.5	---	---	mAdc	---	---	---	24	---	---	mAdc
Switching Time (Pin 4 connected to Pin 5)	t_{pd+}	---	---	15	60	---	---	ns	---	---	15	60	---	---	ns
	t_{pd-}	---	---	10	30	---	---	ns	---	---	10	30	---	---	ns

Pins not listed are left open.

MC937F/MC837F, P (continued)

FIGURE 2 — SWITCHING TIME TEST CIRCUIT AND WAVEFDRMS

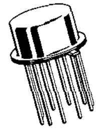


NOTE: All diodes are MC833 or equivalent

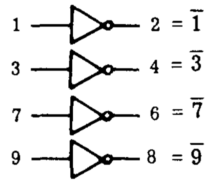
@ Test Temperature		TEST CONDITIONS mA		VOLTS										
MC937F	-55°C	10.4	-0.12	1.40	2.10	0	4.00	---	---	4.50	5.50	---	---	
	+25°C	11.0	-0.12	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	5.00	8.00	
	+125°C	9.8	-0.12	0.80	2.00	0	4.00	---	---	4.50	5.50	---	---	
MC837F, P	0°C	11.0	-0.12	1.20	2.00	0.45	4.00	---	---	5.00	5.00	---	---	
	+25°C	11.0	-0.12	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	5.00	8.00	
	+75°C	10.4	-0.12	0.95	1.80	0.50	4.00	---	---	5.00	5.00	---	---	
CHARACTERISTIC	SYMBOL PIN IN ( )	I_{OL} PIN	I_{OH} PIN	V_{IL} PIN	V_{IH} PIN	V_F PIN	V_R PIN	V_{CEX} PIN	V_{CC} PIN	V_{CCL} PIN	V_{CCH} PIN	V_{PD} PIN	V_{MAX} PIN	GROUNDED PIN
Output Voltage	$V_{OL(6)}$	6			5					14				7
	$V_{OH(6)}$		6	5						14				7
Short-Circuit Current	$I_{SC(6)}$										14			5,6,7
Reverse Current	$I_{R(5)}$						5				14			7
Output Leakage Current	$I_{CEX(6)}$							6,14						5,7
Forward Current	$I_{F(5)}$					5						14		7
Power Drain Current	$I_{PDH(14)}$											14		7
	$I_{MAX(14)}$												14	1,3,5,7,9,11,13
Switching Time		Pulse In	Pulse Out											
(Pin 4 connected to Pin 5)	t_{pd+}	5	6						14					7
	t_{pd-}	5	6						14					7

Pins not listed are left open.

MC946G
MC846G



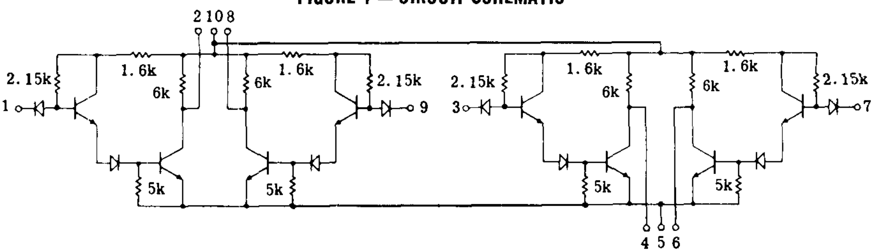
CASE 96A
TO-100



MDTL QUAD INVERTER (Additions to MC930/ MC830 Series)

t_{pd} = 30 ns typ
P_D = 44 mW typ
Input Loading Factor = 1
Fan-Out = 8

FIGURE 1 — CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one inverter only.

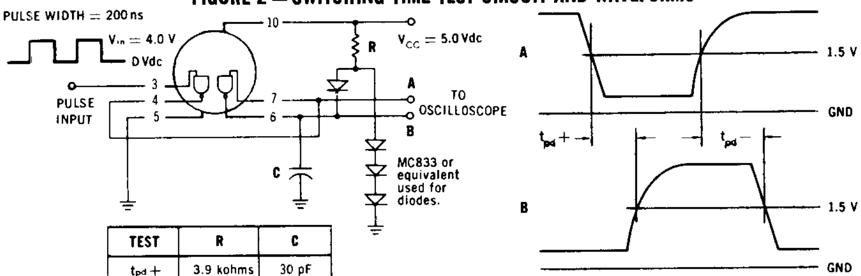
Other inverters are tested in the same manner.

CHARACTERISTIC	SYMBOL PIN IN ( )	MC946G TEST LIMITS -55°C MIN	MAX	+25°C MIN	MAX	+125°C MIN	MAX	UNIT	MC846G TEST LIMITS 0°C MIN	MAX	+25°C MIN	MAX	+75°C MIN	MAX	UNI
Output Voltage	$V_{OL(4)}$	---	0.40	---	0.40	---	0.45	Vdc	---	0.45	---	0.45	---	0.50	Vdc
	$V_{OH(4)}$	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
Short-Circuit Current	$I_{SC(4)}$	---	-1.34	---	-1.34	---	-1.30	mAdc	---	-1.30	---	-1.30	---	-1.25	mAd
Reverse Current	$I_{R(3)}$	---	2.0	---	2.0	---	5.0	µAdc	---	5.0	---	5.0	---	10	µAd
Output Leakage Current	$I_{CEX(4)}$	---	---	---	50	---	---	µAdc	---	---	---	100	---	---	µAd
Forward Current	$I_{F(3)}$	---	-1.60	---	-1.60	---	-1.50	mAdc	---	-1.40	---	-1.40	---	-1.33	mAd
Power Drain Current	$I_{PDH(10)}$	---	---	---	13	---	---	mAdc	---	---	---	16	---	---	mAd
	$I_{MAX(10)}$	---	---	---	11	---	---	mAdc	---	---	---	16	---	---	mAd
Switching Time (Fig. 2) (Pin 4 connected to Pin 7)	t_{pd+}	---	---	25	80	---	---	ns	---	---	25	80	---	---	ns
	t_{pd-}	---	---	10	30	---	---	ns	---	---	10	30	---	---	ns

Pins not listed are left open.

MC946G/MC846G (continued)

FIGURE 2 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



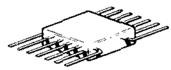
TEST	R	C
tpd +	3.9 kohms	30 pF
tpd −	400 ohms	50 pF

Only connected pins are shown.
All others are open

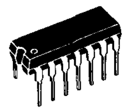
@ Test Temperature		TEST CONDITIONS mA		VOLTS										
MC946G -55°C		11.4	-0.12	1.40	2.10	0	4.00	---	---	4.50	5.50	---	---	
MC946G +25°C		12.0	-0.12	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	5.00	8.00	
MC946G +125°C		10.8	-0.12	0.80	2.00	0	4.00	---	---	4.50	5.50	---	---	
MC846C 0°C		12.0	-0.12	1.20	2.00	0.45	4.00	---	---	5.00	5.00	---	---	
MC846C +25°C		12.0	-0.12	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	5.00	8.00	
MC846C +75°C		11.4	-0.12	0.95	1.80	0.50	4.00	---	---	5.00	5.00	---	---	
CHARACTERISTIC	**SYMBOL PIN IN ( )**	I_{DL} PIN	I_{DH} PIN	V_{IL} PIN	V_{IH} PIN	V_F PIN	V_R PIN	V_{CEX} PIN	V_{CC} PIN	V_{CCL} PIN	V_{CCH} PIN	V_{PD} PIN	V_{MAX} PIN	**GROUND PIN**
Output Voltage	$V_{OL(4)}$	4			3					10				5
	$V_{OH(4)}$		4	3						10				5
Short-Circuit Current	$I_{SC(4)}$										10			3,4,5
Reverse Current	$I_{R(3)}$						3				10			5
Output Leakage Current	$I_{CEX(4)}$							4,10						3,5
Forward Current	$I_{F(3)}$					3					10			5
Power Drain Current	$I_{PDH(10)}$											10		5
	$I_{MAX(10)}$												10	1,3,5,7,9
Switching Time (Fig. 2) (Pin 4 connected to Pin 7)		Pulse In	Pulse Out											
	t_{pd+}	7	6						10					5
	t_{pd-}	7	6						10					5

Pins not listed are left open.

MC949F
MC849F, P



TO-86
CASE 83
SUFFIX F



UNIBLOC
PLASTIC PACKAGE
CASE 93
SUFFIX P

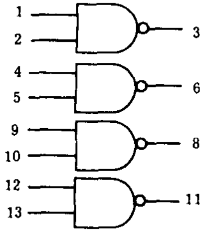
MDTL QUAD 2-INPUT "NAND/NOR" GATES
(Additions to MC930/MC830 Series)

t_{pd} = 25 ns typ

P_D = 66 mW typ

Input Loading Factor = 1

Fan-Out = 7

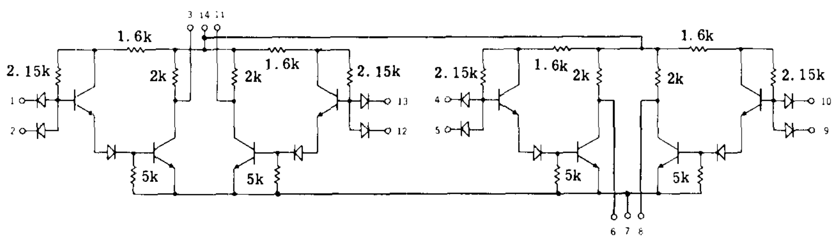


Positive Logic:

$3 = \overline{1 \cdot 2}$ $8 = \overline{9 \cdot 10}$

$6 = \overline{4 \cdot 5}$ $11 = \overline{12 \cdot 13}$

FIGURE 1 — CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

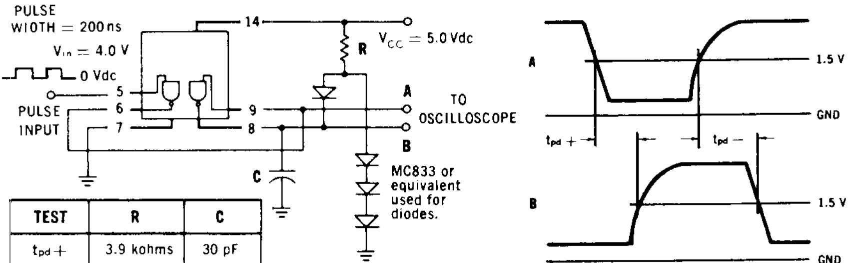
Test procedures are shown for one gate only.
Other gates are tested in the same manner.

Characteristic	Symbol Pin No in ( )	MC949 Test Limits -55°C Min	Max	+25°C Min	Max	+125°C Min	Max	Unit	MC849 Test Limits 0°C Min	Max	+25°C Min	Max	+75°C Min	Max	Unit
Output Voltage	V_{OL}(6)	---	0.40	---	0.40	---	0.45	Vdc	---	0.45	---	0.45	---	0.50	Vdc
	V_{OH}(6)	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
	V_{OH}(6)	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
Short-Circuit Current	I_{SC}(6)	---	-4.0	---	-4.0	---	-3.9	mAdc	---	-3.9	---	-3.9	---	-3.75	mAdc
Reverse Current	I_R(4)	---	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10	μAdc
	I_R(5)	---	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10	μAdc
Output Leakage Current	I_{CEX}(6)	---	---	---	50	---	---	μAdc	---	---	---	100	---	---	μAdc
Forward Current	I_F(4)	---	-1.60	---	-1.60	---	-1.50	mAdc	---	-1.40	---	-1.40	---	-1.33	mAdc
	I_F(5)	---	-1.60	---	-1.60	---	-1.50	mAdc	---	-1.40	---	-1.40	---	-1.33	mAdc
Power Drain Current	I_{PDH}(14)	---	---	---	21.4	---	---	mAdc	---	---	---	26.2	---	---	mAdc
	I_{MAX}(14)	---	---	---	11.0	---	---	mAdc	---	---	---	16.0	---	---	mAdc
Switching Time (Pin 6 connected to Pin 9)	t_{pd}^+	---	---	15	60	---	---	ns	---	---	15	60	---	---	ns
	t_{pd}^-	---	---	10	30	---	---	ns	---	---	10	30	---	---	ns

Pins not listed are left open.

MC949F/MC849F, P (continued)

FIGURE 2 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



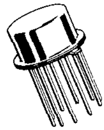
TEST	R	C
$t_{pd}+$	3.9 kohms	30 pF
$t_{pd}-$	400 ohms	50 pF

Only connected pins are shown.
All others are open

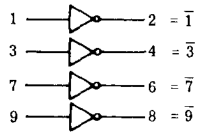
@Test Temperature		TEST CONDITIONS (mA)		(Volts)										
MC949	-55°C	10.4	-0.12	1.40	2.10	0	4.00	---	---	4.50	5.50	---	---	
	+25°C	11.0	-0.12	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	5.00	8.00	
	+125°C	9.8	-0.12	0.80	2.00	0	4.00	---	---	4.50	5.50	---	---	
MC849	0°C	11.0	-0.12	1.20	2.00	0.45	4.00	---	---	5.00	5.00	---	---	
	+25°C	11.0	-0.12	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	5.00	8.00	
	+75°C	10.4	-0.12	0.95	1.80	0.50	4.00	---	---	5.00	5.00	---	---	
Characteristic	**Symbol Pin No in ( )**	I_{OL} Pin No	I_{OH} Pin No	V_{IL} Pin No	V_{IH} Pin No	V_F Pin No	V_R Pin No	V_{CEX} Pin No	V_{CC} Pin No	V_{CCL} Pin No	V_{CCH} Pin No	V_{PD} Pin No	V_{MAX} Pin No	**Grounded Pin No**
Output Voltage	V_{OL}(6)	6	---	---	4,5	---	---	---	---	14	---	---	---	7
	V_{OH}(6)	---	6	5	---	---	---	---	---	14	---	---	---	7
	V_{OH}(6)	---	6	4	---	---	---	---	---	14	---	---	---	7
Short-Circuit Current	I_{SC}(6)	---	---	---	---	---	---	---	---	---	14	---	---	4,6,7
Reverse Current	I_R(4)	---	---	---	---	---	4	---	---	---	14	---	---	5,7
	I_R(5)	---	---	---	---	---	5	---	---	---	14	---	---	4,7
Output Leakage Current	I_{CEX}(6)	---	---	---	---	---	---	6,14	---	---	---	---	---	4,7
Forward Current	I_F(4)	---	---	---	---	4	5	---	---	---	14	---	---	7
	I_F(5)	---	---	---	---	5	4	---	---	---	14	---	---	7
Power Drain Current	I_{PDH}(14)	---	---	---	---	---	---	---	---	---	---	14	---	7
	I_{MAX}(14)	---	---	---	---	---	---	---	---	---	---	---	14	1,4,7,9,12
Switching Time (Pin 6 connected to Pin 9)		Pulse In	Pulse Out											
	$t_{pd}+$	9	8	---	---	---	---	---	14	---	---	---	---	7
	$t_{pd}-$	9	8	---	---	---	---	---	14	---	---	---	---	7

Pins not listed are left open.

MC949G
MC849G



TO-100
CASE 96A



MDTL QUAD INVERTER
(Additions to MC930/MC830 Series)

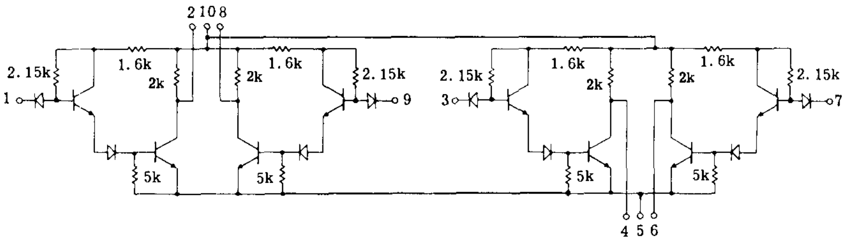
t_{pd} = 25 ns typ

P_D = 60 mW typ

Input Loading Factor = 1

Fan-Out = 7

FIGURE 1 — CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Test procedures are shown for one inverter only.

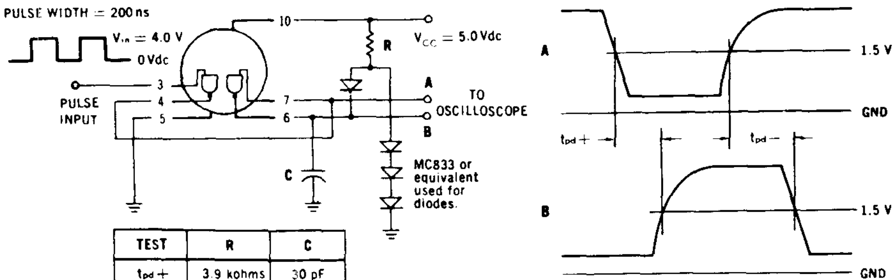
Other inverters are tested in the same manner.

CHARACTERISTIC	SYMBOL PIN IN ( )	MC949G TEST LIMITS -55°C MIN	-55°C MAX	+25°C MIN	+25°C MAX	+125°C MIN	+125°C MAX	UNIT	MC849G TEST LIMITS 0°C MIN	0°C MAX	+25°C MIN	+25°C MAX	+75°C MIN	+75°C MAX	UNIT
Output Voltage	$V_{OL(4)}$	---	0.40	---	0.40	---	0.45	Vdc	---	0.45	---	0.45	---	0.50	Vdc
	$V_{OH(4)}$	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
Short-Circuit Current	$I_{SC(4)}$	---	-4.0	---	-4.0	---	-3.9	mAdc	---	-3.9	---	-3.9	---	-3.75	mAdc
Reverse Current	$I_{R(3)}$	---	2.0	---	2.0	---	5.0	µAdc	---	5.0	---	5.0	---	10	µAdc
Output Leakage Current	$I_{CEX(4)}$	---	---	---	50	---	---	µAdc	---	---	---	100	---	---	µAdc
Forward Current	$I_{F(3)}$	---	-1.60	---	-1.60	---	-1.50	mAdc	---	-1.40	---	-1.40	---	-1.33	mAdc
Power Drain Current	$I_{PDH(10)}$	---	---	---	21.4	---	---	mAdc	---	---	---	26.2	---	---	mAdc
	$I_{MAX(10)}$	---	---	---	11.0	---	---	mAdc	---	---	---	16.0	---	---	mAdc
Switching Time (Fig.2) (Pin 4 connected to Pin 7)	t_{pd+}	---	---	15	60	---	---	ns	---	---	15	60	---	---	ns
	t_{pd-}	---	---	10	30	---	---	ns	---	---	10	30	---	---	ns

Pins not listed are left open.

MC949G/MC849G (continued)

FIGURE 2 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST	R	C
tpd +	3.9 kohms	30 pF
tpd −	400 ohms	50 pF

Only connected pins are shown. All others are open

@ Test Temperature		I_{OL} (mA)	I_{OH} (mA)	V_{IL} (VOLTS)	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{PD}	V_{MAX}	
MC949G	-55°C	10.4	-0.12	1.40	2.10	0	4.00	---	---	4.50	5.50	---	---	
	+25°C	11.0	-0.12	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	5.00	8.00	
	+125°C	9.8	-0.12	0.80	2.00	0	4.00	---	---	4.50	5.50	---	---	
MC849G	0°C	11.0	-0.12	1.20	2.00	0.45	4.00	---	---	5.00	5.00	---	---	
	+25°C	11.0	-0.12	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	5.00	8.00	
	+75°C	10.4	-0.12	0.95	1.80	0.50	4.00	---	---	5.00	5.00	---	---	
CHARACTERISTIC	**SYMBOL PIN IN ( )**	I_{OL} PIN	I_{OH} PIN	V_{IL} PIN	V_{IH} PIN	V_F PIN	V_R PIN	V_{CEX} PIN	V_{CC} PIN	V_{CCL} PIN	V_{CCH} PIN	V_{PD} PIN	V_{MAX} PIN	**GROUND PIN**
Output Voltage	$V_{OL(4)}$	4			3					10				5
	$V_{OH(4)}$		4	3						10				5
Short-Circuit Current	$I_{SC(4)}$										10			3,4,5
Reverse Current	$I_{R(3)}$						3				10			5
Output Leakage Current	$I_{CEX(4)}$							4,10						3,5
Forward Current	$I_{F(3)}$					3					10			5
Power Drain Current	$I_{PDH(10)}$											10		5
	$I_{MAX(10)}$												10	1,3,5,7,9
Switching Time (Fig.2)		Pulse In	Pulse Out											
(Pin 4 connected to Pin 7)	t_{pd+}	7	6						10					5
	t_{pd-}	7	6						10					5

Pins not listed are left open.

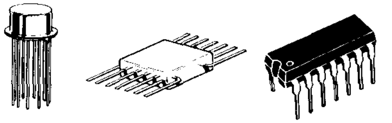
MC950F, G
MC850F, G, P

MDTL PULSE TRIGGERED BINARY
(Additions to MC930/MC830 Series)

The MC950/MC850 is a high-speed gated flip-flop which utilizes capacitive coupling of the pulse-triggered set and clear inputs. Directly coupled set and clear inputs are available as well as direct set and clear inputs that respond to dc levels and override the clocked inputs. Separate clock signals may be applied to the capacitively coupled inputs or they may be tied together to obtain single-channel triggering operation. Maximum toggle frequency is typically 40 MHz at 25°C with power dissipation on the order of 30 mW.

Typical applications include binary ripple counters, shift registers, and similar applications. It may be used to advantage in high-speed portions of digital systems that are presently using MDTL circuitry.

$t_{pd} = 15$ ns
$P_D = 50$ mW

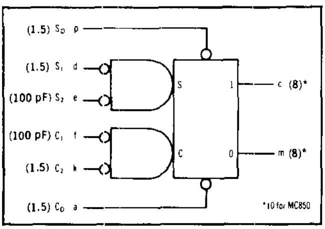


TO-100
CASE 96A
SUFFIX G

TO-86
CASE 83
SUFFIX F

UNIBLOC
PLASTIC PACKAGE
CASE 93
SUFFIX P

The numbers in parentheses indicate loading at each terminal.



SYNCHRONOUS TRUTH TABLE

t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	0	0	0	U
1	X	1	X	Q_n
X	1	X	1	Q_n
0	1	1	0	Q_n
0	0	X	1	1
0	0	1	X	1
1	X	0	0	0
X	1	0	0	0

ASYNCHRONOUS TRUTH TABLE

S_D	C_D	Q	$\overline{Q}$
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

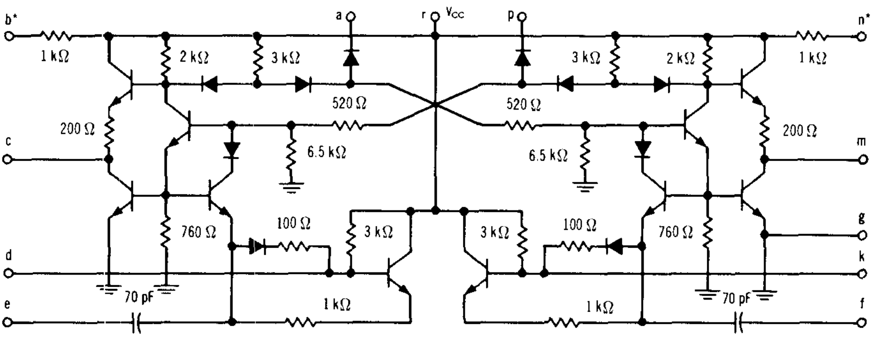
SINGLE TRIGGER TRUTH TABLE
(Pins S_2 and C_1 tied together)

t_n		t_{n+1}
S_1	C_2	Q
0	0	U
1	0	0
0	1	1
1	1	Q_n

0 = low state (more negative) 1 = high state (more positive)

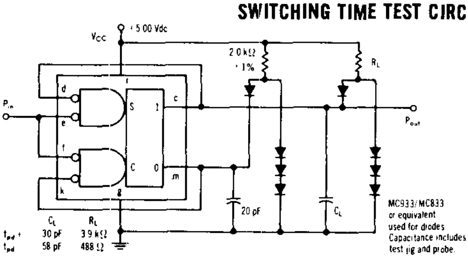
X = don't care U = indeterminate state NC = no change

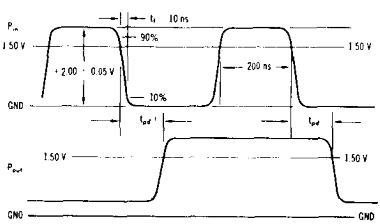
CIRCUIT SCHEMATIC



*Available with Flat and Plastic-Packaged devices only.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





MC950F, G/MC850F, G, P (continued)

ELECTRICAL CHARACTERISTICS

PIN CONNECTIONS												
Schematic	a	b	c	d	e	f	g	k	m	n	p	r
"F" and "P" Packages	1	2	3	4	5	6	7	10	11	12	13	14
"G" Package	1	—	2	3	4	5	6	7	8	—	9	10

	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES: mA I_{OL}	mA I_{OH}	Volts V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{PD}	V_{max}
MC950	−55°C	11.4	−1.50	0	4.00	—	—	4.50	5.50	—	—
MC950	+25°C	12.0	−1.50	0	4.00	4.50	5.00	4.50	5.50	5.08	8.00
MC950	+125°C	10.8	−1.50	0	4.00	—	—	4.50	5.50	—	—
MC850	0°C	14.0	−1.50	0.45	4.00	—	—	5.00	5.00	—	—
MC850	+25°C	14.0	−1.50	8.45	4.00	5.00	5.00	5.00	5.80	5.00	8.00
MC850	+75°C	13.3	−1.50	0.50	4.00	—	—	5.00	5.00	—	—

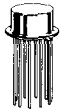
Characteristic	Symbol	Pin Under Test	MC950 −55°C Min	MC950 −55°C Max	MC950 +25°C Min	MC950 +25°C Max	MC950 +125°C Min	MC950 +125°C Max	Unit	MC850 0°C Min	MC850 0°C Max	MC850 +25°C Min	MC850 +25°C Max	MC850 +75°C Min	MC850 +75°C Max
Output Voltage	V_{OL}	c	—	0.40	—	0.40	—	0.45	Vdc	—	0.45	—	0.45	—	0.50
	V_{OL}	m	—	0.40	—	0.40	—	0.45	Vdc	—	0.45	—	0.45	—	0.50
	V_{OH}	c	2.50	—	2.60	—	2.50	—	Vdc	2.60	—	2.60	—	2.50	—
	V_{OH}	m	2.50	—	2.60	—	2.50	—	Vdc	2.60	—	2.60	—	2.50	—
Short-Circuit Current	I_{SC}	c	−11.5	—	−14.0	—	−13.0	—	mAdc	−12.6	—	−13.7	—	−12.6	—
	I_{SC}	m	−11.5	—	−14.0	—	−13.0	—	mAdc	−12.6	—	−13.7	—	−12.6	—
Reverse Current	I_R	a	—	2.0	—	2.0	—	5.0	µAdc	—	5.0	—	5.0	—	10
	I_R	p	—	2.0	—	2.0	—	5.0	µAdc	—	5.0	—	5.0	—	10
	I_{RCP}	e	—	20	—	20	—	30	µAdc	—	30	—	30	—	40
	I_{RCP}	f	—	20	—	20	—	30	µAdc	—	30	—	30	—	40
Output Leakage Current	I_{CEX}	c	—	—	—	50	—	—	µAdc	—	—	—	100	—	—
	I_{CEX}	m	—	—	—	50	—	—	µAdc	—	—	—	100	—	—
Forward Current	$1.5\,I_F$	a	—	−2.40	—	−2.40	—	−2.25	mAdc	—	−2.2	—	−2.2	—	−2.1
	$1.5\,I_F$	p	—	−2.40	—	−2.40	—	−2.25	mAdc	—	−2.2	—	−2.2	—	−2.1
	$1.5\,I_F$	d	—	−2.40	—	−2.40	—	−2.25	mAdc	—	−2.2	—	−2.2	—	−2.1
	$1.5\,I_F$	k	—	−2.40	—	−2.40	—	−2.25	mAdc	—	−2.2	—	−2.2	—	−2.1
	I_Z ②	b	—	—	−4.60	−6.90	—	—	mAdc	—	—	−3.85	−7.15	—	—
	I_{1Z} ②	n	—	—	−4.60	−6.90	—	—	mAdc	—	—	−3.85	−7.15	—	—
Power Drain Current	I_{PDH}	r	—	—	—	9	—	—	mAdc	—	—	—	10	—	—
	I_{max}	r	—	—	—	14	—	—	mAdc	—	—	—	16	—	—
Switching Time (Pin e connected to Pin f, d to c, h to j)	$t_{pd}+$	c	—	—	—	50	—	—	ns	—	—	—	50	—	—
	$t_{pd}-$	c	—	—	—	50	—	—	ns	—	—	—	50	—	—

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:

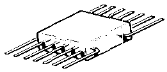
Characteristic	Symbol	Pin Under Test	I_{OL}	I_{OH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{PD}	V_{max}	Gnd
Output Voltage	V_{OL}	c	c	—	—	—	—	—	r	—	—	—	a, g
	V_{OL}	m	m	—	—	—	—	—	r	—	—	—	g, p
	V_{OH}	c	—	c	—	—	—	—	r	—	—	—	g, p①
	V_{OH}	m	—	m	—	—	—	—	r	—	—	—	a①, g
Short-Circuit Current	I_{SC}	c	—	—	—	—	—	—	—	r	—	—	c, g, p
	I_{SC}	m	—	—	—	—	—	—	—	r	—	—	a, g, m
Reverse Current	I_R	a	—	—	—	a	—	—	—	r	—	—	g
	I_R	p	—	—	—	p	—	—	—	r	—	—	g
	I_{RCP}	e	—	—	—	e	—	—	—	r	—	—	d, g, j
	I_{RCP}	f	—	—	—	f	—	—	—	r	—	—	d, g, j
Output Leakage Current	I_{CEX}	c	—	—	—	—	c, r	—	—	—	—	—	g, p①
	I_{CEX}	m	—	—	—	—	m, r	—	—	—	—	—	a①, g
Forward Current	$1.5\,I_F$	a	—	—	a	p	—	—	—	r	—	—	g
	$1.5\,I_F$	p	—	—	p	a	—	—	—	r	—	—	g
	$1.5\,I_F$	d	—	—	d	k	—	—	—	r	—	—	g
	$1.5\,I_F$	k	—	—	k	d	—	—	—	r	—	—	g
	I_Z ②	b	—	—	—	—	—	—	—	r	—	—	b, g
	I_{1Z} ②	n	—	—	—	—	—	—	—	r	—	—	g, n
Power Drain Current	I_{PDH}	r	—	—	—	—	—	—	—	—	r	—	g
	I_{max}	r	—	—	—	—	—	—	—	—	—	r	a, g, p
Switching Time (Pin e connected to Pin f, d to c, h to j)			Pulse In	Pulse Out									
	$t_{pd}+$	c	e	c	—	—	—	r	—	—	—	—	g
	$t_{pd}-$	c	e	c	—	—	—	r	—	—	—	—	g

Pins not listed are left open. ① Momentarily ground this terminal before taking measurement. ② Test applies to devices in Flat and Plastic packages only.

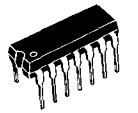
MC951F, G
MC851F, G, P
MDTL MONOSTABLE MULTIVIBRATOR (Additions to MC930/MC830 Series)



TO-100
CASE 96A
SUFFIX G



TO-86
CASE 83
SUFFIX F

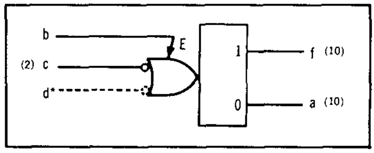


UNIBLOC PLASTIC PACKAGE
CASE 93
SUFFIX P

The MC951/MC851 is a monolithic monostable multivibrator circuit which gives complementary output pulses upon the dynamic zero transition of the input waveform. The output pulse width is determined by an R-C timing circuit and, due to differentiation of the input, is essentially independent of the input pulse width. With internal components, nominal pulse width is 120 ns.

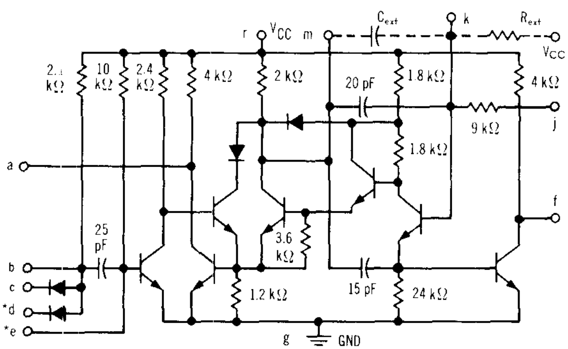
Provisions are available to increase the pulse width by adding external capacitance and to increase pulse width stability by utilizing a precision external resistor in place of the internal charging resistor.

Typical applications include analog comparators, elimination of transients on pulse waveforms, and provision for delays to insure the proper sequence of digital operations in computer applications.



t_{pd} = 40 ns
P_D = 30 mW

CIRCUIT SCHEMATIC



NOTE: When the internal timing resistor (9 kΩ) is to be used, connect Pin j to Pin r. DO NDT MAKE THIS CONNECTION IF USING THE EXTERNAL CAPACITOR AND RESISTOR.

*Available with Flat and Plastic-Packaged devices only.

APPLICATIONS INFORMATION

Output Pulse Width

External Components Used	Internal Resistor Connection	Pulse Width ns (approx)
None	Pin j to Vcc	100
C_{ext} (between Pins k & m)	Pin j to Vcc	4.5 (C_{ext} + 20)
R_{ext} (between Pin k & Vcc) (9 kΩ min, 15 kΩ max)	Pin j open	0.5 R_{ext} (C_{ext} + 20)

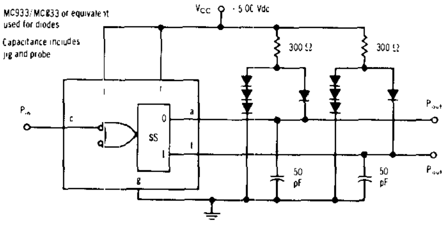
Capacitance values in pF

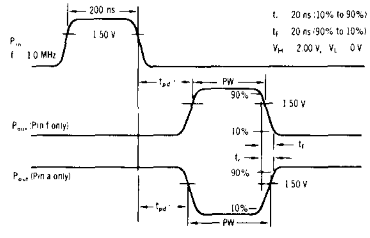
Maximum Input Fall Time to Trigger

t_f ns	Voltage Swing Volts
25	1.0
50	2.0
100	4.0

Output duty cycle ≤ 40%. Higher duty cycles obtainable at a possible decrease of performance.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





MC951F, G/MC851F, G, P (continued)

ELECTRICAL CHARACTERISTICS

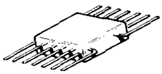
PIN CONNECTIONS											
Schematic	a	b	c	d	e	f	g	j	k	m	r
"F" and "P" Packages	1	2	3	4	5	6	7	9	10	11	14
"G" Package	7	8	9	—	—	10	1	2	3	4	6

	@ Test Temperature	TEST CURRENT/VOLTAGE VALUES mA		Volts						
		I_{OL}	I_{OH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{PD}	V_{max}
MC951	−55°C	15.0	−0.180	0	4.00	—	4.50	5.50	—	—
	+25°C	15.0	−0.180	0	4.00	5.00	4.50	5.50	5.00	8.00
	+125°C	14.8	−0.180	0	4.00	—	4.50	5.50	—	—
MC851	0°C	15.0	−0.180	0.45	4.00	—	5.88	5.08	—	—
	+25°C	15.0	−0.180	8.45	4.00	5.00	5.80	5.00	5.00	8.00
	+75°C	14.0	−0.180	0.50	4.80	—	5.80	5.00	—	—

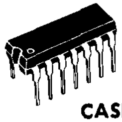
Characteristic	Symbol	Pin Under Test	MC951 TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC851 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	V_{PD}	V_{max}	Gnd
Output Voltage	V_{OL}	a	—	0.40	—	0.40	—	0.45	Vdc	—	0.45	—	0.45	—	0.50	a	—	—	—	—	r	—	—	—	g,k
	V_{OL} ①	a	—	0.40	—	0.40	—	0.45	Vdc	—	0.45	—	0.45	—	0.50	a	—	—	—	—	r	—	—	—	e, g
	V_{OL}	f	—	0.40	—	0.40	—	4.45	Vdc	—	0.45	—	0.45	—	0.50	f	—	—	—	—	j,r	—	—	—	g
	V_{OH}	a	2.50	—	2.60	—	2.50	—	Vdc	2.60	—	2.60	—	2.50	—	—	a	—	—	—	j,r	—	—	—	g
	V_{OH}	f	2.50	—	2.60	—	2.50	—	Vdc	2.60	—	2.60	—	2.50	—	—	f	—	—	—	r	—	—	—	g,k
Reverse Current	I_R	c	—	2.0	—	2.0	—	5.0	µAdc	—	5.0	—	5.0	—	10	—	—	—	c	—	—	r	—	—	b,g
	I_R ①	d	—	2.0	—	2.0	—	5.0	µAdc	—	5.0	—	5.0	—	10	—	—	—	d	—	—	r	—	—	b,g
Forward Current	$0.5\,I_F$	b	−0.80	—	−0.80	—	−0.75	—	mAdc	−0.70	—	−0.70	—	−0.67	—	—	—	b	—	—	—	r	—	—	g
	$0.5\,I_F/2\,I_F$ ②③	c	−0.80	−3.20	−0.80	−3.20	−0.75	−3.00	mAdc	−0.70	−2.80	−0.70	−2.80	−0.67	−2.67	—	—	c	d	—	—	r	—	—	g
	$0.5\,I_F/2\,I_F$ ①③	d	−0.80	−3.20	−0.80	−3.20	−0.75	−3.00	mAdc	−0.70	−2.80	−0.70	−2.80	−0.67	−2.67	—	—	d	c	—	—	r	—	—	g
	$0.5\,I_F$	m	−0.80	—	−0.80	—	−0.75	—	mAdc	−0.70	—	−0.70	—	−0.67	—	—	—	k	—	—	—	r	—	—	g
	I_j	j	—	—	0.50	0.75	—	—	mAdc	—	—	0.45	0.80	—	—	—	—	—	—	—	—	j,r	—	—	g,k
Power Drain Current	I_{PDL} ②	④	—	—	—	9	—	—	mAdc	—	—	—	12	—	—	—	—	—	—	—	—	—	j, r	—	c,d,g
	I_{max} ②	r	—	—	—	22	—	—	mAdc	—	—	—	25	—	—	—	—	—	—	—	—	—	—	r	c,d,g
Switching Times																Pulse In	Pulse Out								
	$t_{pd}+$	f	—	—	—	50	—	—	ns	—	—	—	50	—	—	c	f	—	—	j,r	—	—	—	—	g
	$t_{pd}-$	a	—	—	—	50	—	—	ns	—	—	—	50	—	—	c	a	—	—	j,r	—	—	—	—	g
	PW	a	—	—	90	160	—	—	ns	—	—	90	160	—	—	c	a	—	—	j,r	—	—	—	—	g
	PW	f	—	—	90	160	—	—	ns	—	—	90	160	—	—	c	f	—	—	j,r	—	—	—	—	g

① Test applies to devices in Flat and Plastic packages only. ② Test given for all packages; use available pins for applied voltages or ground (i.e., one input missing on Metal Can).
③ Min/Max. ④ I_{PDL} is measured into Pins j and r simultaneously.

MC952, MC852
MC953, MC853
MC955, MC855
MC956, MC856



CASE 83
TO-86
SUFFIX F (all types)



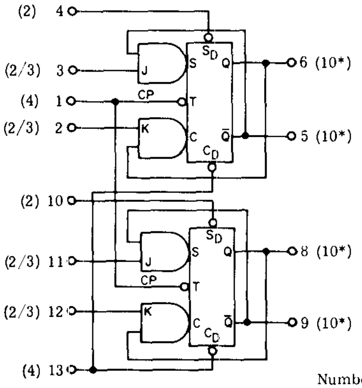
CASE 93
UNIBLOC
PLASTIC PACKAGE
SUFFIX P
(MC852 thru MC856 only)

MDTL DUAL J-K FLIP-FLOPS (Additions to MC930/MC830 Series)

t_{pd} = 40 ns typ (all types)

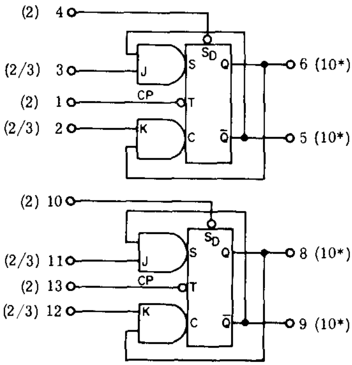
Total P_D = 120 mW typ - MC952/MC852, MC953/MC853
140 mW typ - MC955/MC855, MC956/MC856

MC952/MC852



* 12 for MC852

MC953/MC853



* 12 for MC853

Number in parenthesis indicates loading.

Each section of the MC952/MC852 and MC953/MC853 dual J-K clocked flip-flops consists of two directly-coupled flip-flops operating on the familiar "master-slave" principle. Operation depends only on voltage levels, so the rise and fall times of the input clock are unimportant in determining the state of the flip-flop. Input information is stored in the "master" flip-flop when the clock voltage is high and is transferred to the "slave" when the clock voltage goes low.

The MC952/MC852 has a common clock input which makes this device suitable for clocked counters and shift register applications. A common direct clear (C_D) and separate direct sets (S_D) are available. The direct inputs override all synchronous inputs.

The MC953/MC853 has separate clock inputs to each flip-flop, which makes the device suitable for ripple counter applications. Separate direct set inputs which override the synchronous inputs are also provided.

The outputs of the flip-flops are buffered, thereby reducing the possibility of circuit disturbance from external line noise.

MC952/852, MC953/853, MC955/855, MC956/856 (continued)

ASYNCHRONOUS TRUTH TABLE MC952/MC852 and MC955/MC855

S_D Pin 4 (10)	C_D Pin 13	Q Pin 6 (8)	$\overline{Q}$ Pin 5 (9)
1	1	NC	NC
0	1	1	0
1	0	0	1
0	0	1	1

ASYNCHRONOUS TRUTH TABLE MC953/MC853 and MC956/MC856

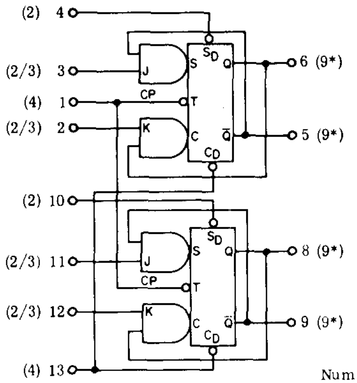
S_D Pin 4 (10)	Q Pin 6 (8)	$\overline{Q}$ Pin 5 (9)
1	NC	NC
0	1	0

J-K TRUTH TABLE – All Types

t_n		t_{n+1}
J Pin 3 (11)	K Pin 2 (12)	Q Pin 6 (8)
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs; they are independent of all other inputs. Number in parenthesis indicates pin number of other side.

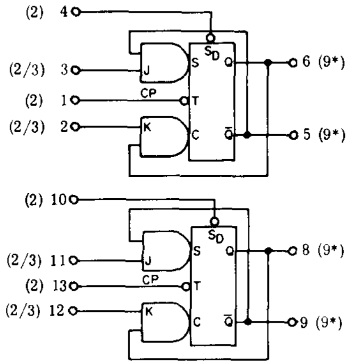
MC955/MC855



* 11 for MC855

Number in parenthesis indicates loading.

MC956/MC856



* 11 for MC856

Each section of the MC955/MC855 and MC956/MC856 dual J-K clocked flip-flops consists of two directly-coupled flip-flops operating on the familiar "master-slave" principle. Input information is stored in the "master" flip-flop when the clock voltage is high and is transferred to the "slave" when the clock voltage goes low.

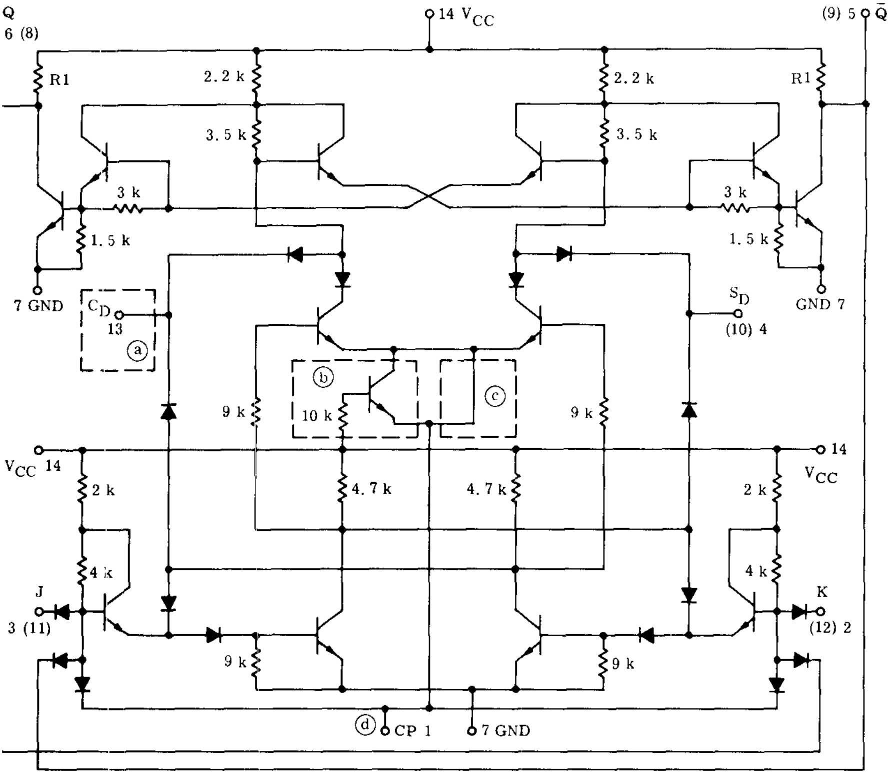
The MC955/MC855 has a common clock input which makes this device suitable for clocked counters and shift register applications. A common direct clear (C_D) and separate direct sets (S_D) are available. The direct inputs override all synchronous inputs.

The MC956/MC856 has separate clock inputs to each flip-flop, which makes the device suitable for ripple counter applications. Separate direct set inputs which override the synchronous inputs are also provided.

The outputs of the flip-flops are buffered, thereby reducing the possibility of circuit disturbance from external line noise. The output pull-up resistor has been changed from that utilized in the MC952/MC852 and MC953/MC853 in order to improve the propagation delay versus capacitance characteristics.

MC952/852, MC953/853, MC955/855, MC956/856 (continued)

CIRCUIT SCHEMATIC (½ of circuit shown)



(a) Used only on MC952/MC852 and MC955/MC855

(b) Used only on MC952/MC852 and MC953/MC853

(c) Used only on MC955/MC855 and MC956 and MC856

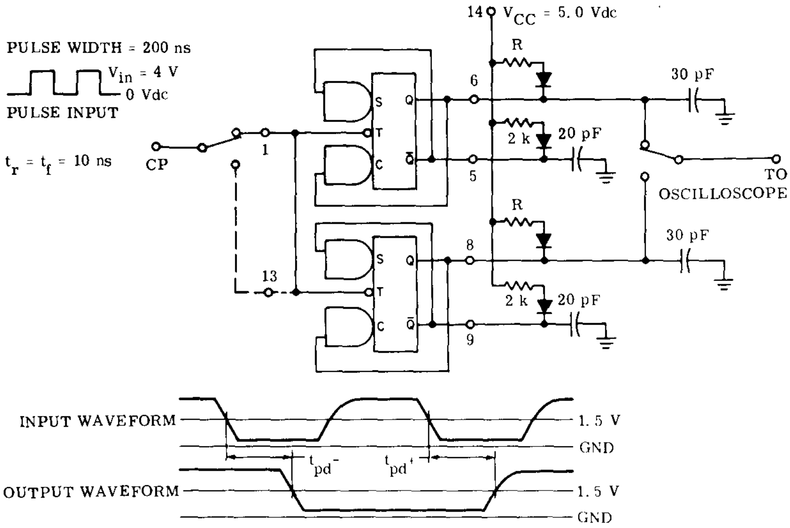
(d) Pin 13 used for other side of MC953/MC853 and MC956/MC856

R1 = 6 k ohms for MC952/MC852 and MC953/MC853
2 k ohms for MC955/MC855 and MC956/MC856

NOTE: Number in parenthesis indicates pin number for other half of the schematic. Ground and V_{CC} pins are common to both sides.

MC952/852, MC953/853, MC955/855, MC956/856 (continued)

PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS



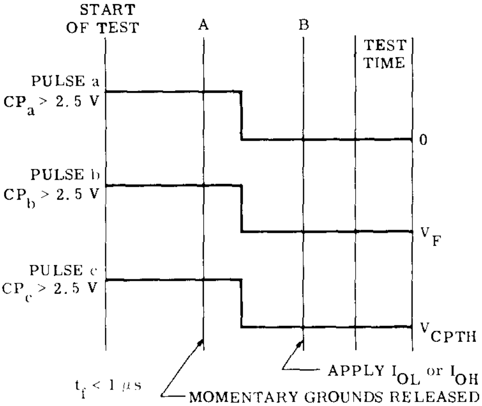
Test circuit shown for MC952/MC852 and MC955/MC855.
Use dotted-line connection for MC953/MC853 and MC956/MC856, which have separate toggle inputs.

Ground pin 7. Only connected inputs are shown. All others are open.

MC833 or equivalent used for diodes.

TEST	R
t_{pd+}	3.9 kohms
t_{pd-}	400 ohms

CLOCK PULSE WAVEFORMS



TEST CONDITIONS

T_A	V_{CPTH}	
	MC952/MC953	MC955/MC956
-55°C	1.15 V	1.30 V
+25°C	0.95 V	1.15 V
+125°C	0.65 V	0.85 V
	MC852/MC853	MC855/MC856
0°C	1.00 V	1.20 V
+25°C	0.95 V	1.15 V
+75°C	0.65 V	0.85 V

ELECTRICAL CHARACTERISTICS MC952/852, MC955/855

CHARACTERISTIC	SYMBOL PIN IN ( )	MC952/MC955 TEST LIMITS -55°C MIN	-55°C MAX	+25°C MIN	+25°C MAX	+125°C MIN	+125°C MAX	UNIT	MC852/MC855 TEST LIMITS 0°C MIN	0°C MAX	+25°C MIN	+25°C MAX	+75°C MIN	+75°C MAX	UNIT
Output Voltage	$V_{OL(5)}$	---	0.40	---	0.40	---	0.45	Vdc	---	0.45	---	0.45	---	0.50	Vdc
	$V_{OL(6)}$	---	0.40	---	0.40	---	0.45	Vdc	---	0.45	---	0.45	---	0.50	Vdc
	$V_{OL(8)}$	---	0.40	---	0.40	---	0.45	Vdc	---	0.45	---	0.45	---	0.50	Vdc
	$V_{OL(9)}$	---	0.40	---	0.40	---	0.45	Vdc	---	0.45	---	0.45	---	0.50	Vdc
	$V_{OH(5)}$	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
	$V_{OH(5)}$	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
	$V_{OH(6)}$	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
	$V_{OH(6)}$	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
	$V_{OH(8)}$	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
	$V_{OH(8)}$	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
	$V_{OH(9)}$	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
	$V_{OH(9)}$	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
Short-Circuit Current MC952/MC852	$I_{SC(5)}$	-1.45	-2.45	-1.30	-2.25	-1.15	-2.00	mAdc	-1.25	-2.50	-1.15	-2.30	-1.05	-2.15	mAdc
	$I_{SC(6)}$	-1.45	-2.45	-1.30	-2.25	-1.15	-2.00	mAdc	-1.25	-2.50	-1.15	-2.30	-1.05	-2.15	mAdc
	$I_{SC(8)}$	-1.45	-2.45	-1.30	-2.25	-1.15	-2.00	mAdc	-1.25	-2.50	-1.15	-2.30	-1.05	-2.15	mAdc
	$I_{SC(9)}$	-1.45	-2.45	-1.30	-2.25	-1.15	-2.00	mAdc	-1.25	-2.50	-1.15	-2.30	-1.05	-2.15	mAdc
MC955/MC855	$I_{SC(5)}$	-3.00	-5.10	-2.70	-4.60	-2.40	-4.10	mAdc	-2.60	-5.20	-2.35	-4.75	-2.20	-4.40	mAdc
	$I_{SC(6)}$	-3.00	-5.10	-2.70	-4.60	-2.40	-4.10	mAdc	-2.60	-5.20	-2.35	-4.75	-2.20	-4.40	mAdc
	$I_{SC(8)}$	-3.00	-5.10	-2.70	-4.60	-2.40	-4.10	mAdc	-2.60	-5.20	-2.35	-4.75	-2.20	-4.40	mAdc
	$I_{SC(9)}$	-3.00	-5.10	-2.70	-4.60	-2.40	-4.10	mAdc	-2.60	-5.20	-2.35	-4.75	-2.20	-4.40	mAdc
Reverse Current All Types	$I_{R(2)}$	---	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10	μAdc
	$I_{R(3)}$	---	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10	μAdc
	$I_{R(4)}$	---	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10	μAdc
	$I_{R(10)}$	---	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10	μAdc
	$I_{R(11)}$	---	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10	μAdc
	$I_{R(12)}$	---	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10	μAdc
	$2I_{R(13)}$	---	4.0	---	4.0	---	10	μAdc	---	10	---	10	---	20	μAdc
MC952/MC852	$2I_{RCP(1)}$	---	20	---	20	---	40	μAdc	---	40	---	40	---	60	μAdc
MC955/MC855	$2I_{RCP(1)}$	---	20	---	20	---	40	μAdc	---	40	---	40	---	60	μAdc
Forward Current	$2/3I_{F(2)}$	---	-1.07	---	-1.07	---	-1.00	mAdc	---	-0.95	---	-0.95	---	-0.90	mAdc
	$2/3I_{F(3)}$	---	-1.07	---	-1.07	---	-1.00	mAdc	---	-0.95	---	-0.95	---	-0.90	mAdc
	$2/3I_{F(11)}$	---	-1.07	---	-1.07	---	-1.00	mAdc	---	-0.95	---	-0.95	---	-0.90	mAdc
	$2/3I_{F(12)}$	---	-1.07	---	-1.07	---	-1.00	mAdc	---	-0.95	---	-0.95	---	-0.90	mAdc
	$2I_{FCP(1)}$	---	-6.40	---	-6.40	---	-6.00	mAdc	---	-5.60	---	-5.60	---	-5.34	mAdc
	$2I_{FCP(1)}$	---	-6.40	---	-6.40	---	-6.00	mAdc	---	-5.60	---	-5.60	---	-5.34	mAdc
	$I_{FS(4)}$	---	-3.20	---	-3.20	---	-3.00	mAdc	---	-2.80	---	-2.80	---	-2.67	mAdc
	$I_{FS(10)}$	---	-3.20	---	-3.20	---	-3.00	mAdc	---	-2.80	---	-2.80	---	-2.67	mAdc
	$2I_{FS(13)}$	---	-6.40	---	-6.40	---	-6.00	mAdc	---	-5.60	---	-5.60	---	-5.34	mAdc
Power Drain Current															
MC952/MC852	$I_{MAX(14)}$	---	---	---	32	---	---	mAdc	---	---	---	36	---	---	mAdc
MC955/MC855	$I_{MAX(14)}$	---	---	---	38	---	---	mAdc	---	---	---	45	---	---	mAdc
MC952/MC852	$I_{PDH(14)}$	---	---	---	22	---	---	mAdc	---	---	---	28	---	---	mAdc
MC955/MC855	$I_{PDH(14)}$	---	---	---	27	---	---	mAdc	---	---	---	34	---	---	mAdc
Switching Time															
MC952/MC852	t_{pd+}	---	---	25	100	---	---	ns	---	---	25	100	---	---	ns
MC955/MC855	t_{pd+}	---	---	25	75	---	---	ns	---	---	25	75	---	---	ns
All Types	t_{pd-}	---	---	15	55	---	---	ns	---	---	15	55	---	---	ns
MC952/MC852	t_{pd+}	---	---	25	100	---	---	ns	---	---	25	100	---	---	ns
MC955/MC855	t_{pd+}	---	---	25	75	---	---	ns	---	---	25	75	---	---	ns
All Types	t_{pd-}	---	---	15	55	---	---	ns	---	---	15	55	---	---	ns

Pins not listed are left open

* Applied after Clock Pulse

† CP_a = Clock Pulse a
†† CP_c = Clock Pulse c
Momentary Ground
} See Clock Pulse Waveforms

MC952/852, MC953/853, MC955/855, MC956/856 (continued)

@ Test Temperature		I_{OL} (mA)	I_{OH} (mA)	V_{IL} (V)	V_{IH} (V)	V_F (V)	V_R (V)	V_{CC} (V)	V_{CCL} (V)	V_{CCH} (V)	V_{PD} (V)	V_{MAX} (V)
		TEST CONDITIONS										
MC952/MC955	-55°C	①	-0.12	1.40	2.10	0	4.00	---	4.50	5.50	---	---
	+25°C	①	-0.12	1.10	2.00	0	4.00	5.00	4.50	5.50	5.00	8.00
	+125°C	①	-0.12	0.80	2.00	0	4.00	---	4.50	5.50	---	---
MC852/MC855	0°C	①	-0.12	1.20	2.00	0.45	4.00	---	5.00	5.00	---	---
	+25°C	①	-0.12	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	8.00
	+75°C	①	-0.12	0.95	1.80	0.50	4.00	---	5.00	5.00	---	---

CHARACTERISTIC	SYMBOL PIN IN ( )	I_{OL} PIN	I_{OH} PIN	V_{IL} PIN	V_{IH} PIN	V_F PIN	V_R PIN	V_{CC} PIN	V_{CCL} PIN	V_{CCH} PIN	V_{PD} PIN	V_{MAX} PIN	CP†a Pin	CP†c Pin	Grounded Pin
Output Voltage	$V_{OL(5)}$	5*		2					14					1	7,13π
	$V_{OL(6)}$	6*		3					14					1	4π,7
	$V_{OL(8)}$	8*		11					14					1	7,10π
	$V_{OL(9)}$	9*		12					14					1	7,13π
	$V_{OH(5)}$		5*	3	2				14				1		4π,7
	$V_{OH(5)}$		5	2,13	4				14				1		7
	$V_{OH(6)}$		6*	2	3				14				1		7,13π
	$V_{OH(6)}$		6	3,4	13				14				1		7
	$V_{OH(8)}$		8*	12	11				14				1		7,13π
	$V_{OH(8)}$		8	10,11	13				14				1		7
	$V_{OH(9)}$		9*	11	12				14				1		7,10π
	$V_{OH(9)}$		9	12,13	10				14				1		7
Short-Circuit Current MC952/MC852	$I_{SC(5)}$									14				1	5,7
	$I_{SC(6)}$									14				1	6,7
	$I_{SC(8)}$									14				1	7,8
	$I_{SC(9)}$									14				1	7,9
MC955/MC855	$I_{SC(5)}$									14				1	5,7
	$I_{SC(6)}$									14				1	6,7
	$I_{SC(8)}$									14				1	7,8
	$I_{SC(9)}$									14				1	7,9
Reverse Current All Types	$I_{R(2)}$						2			14					1,7
	$I_{R(3)}$						3			14					1,7
	$I_{R(4)}$						4			14			1		2,6,7
	$I_{R(10)}$						10			14			1		7,8,12
	$I_{R(11)}$						11			14					1,7
	$I_{R(12)}$						12			14					1,7
	$2I_{R(13)}$						13			14			1		3,5,7,9,11
MC952/MC852	$2I_{RCP(1)}$						1,14								2,3,5,6,7,8,9,11,12
MC955/MC855	$2I_{RCP(1)}$						1			14					2,3,5,6,7,8,9,11,12
Forward Current	$2/3I_{F(2)}$					2				14				1	7
	$2/3I_{F(3)}$					3				14				1	7
	$2/3I_{F(11)}$					11				14				1	7
	$2/3I_{F(12)}$					12				14				1	7
	$2I_{FCP(1)}$			4,10		1				14					7
	$2I_{FCP(1)}$			13		1				14					7
	$I_{FS(4)}$					4				14					2,3,7,13
	$I_{FS(10)}$					10				14					7,11,12,13
	$2I_{FS(13)}$					13				14					2,3,4,7,10,11,12
Power Drain Current MC952/MC852	$I_{MAX(14)}$											14			1,2,3,4,7,10,11,12
MC955/MC855	$I_{MAX(14)}$											14			1,2,3,4,7,10,11,12
MC952/MC852	$I_{PDH(14)}$										14				7
MC955/MC855	$I_{PDH(14)}$										14				7
Switching Time		Pulse In	Pulse Out												
MC952/MC852	t_{pd+}	1	6					14							7
MC955/MC855	t_{pd+}	1	6					14							7
All Types	t_{pd-}	1	6					14							7
MC952/MC852	t_{pd+}	1	8					14							7
MC955/MC855	t_{pd+}	1	8					14							7
All Types	t_{pd-}	1	8					14							7

① I_{OL} Values (mA):

	MC952	MC955
-55°C	14.6	13.0
+25°C	15.2	13.6
+125°C	13.8	12.3

	MC852	MC855
0°C	16.8	15.4
+25°C	16.8	15.4
+75°C	16.0	14.6

ELECTRICAL CHARACTERISTICS MC953/853, MC956/856

CHARACTERISTIC	SYMBOL PIN NO IN ( )	MC953/MC956 TEST LIMITS -55°C MIN	-55°C MAX	+25°C MIN	+25°C MAX	+125°C MIN	+125°C MAX	UNIT	MC853/MC856 TEST LIMITS 0°C MIN	0°C MAX	+25°C MIN	+25°C MAX	+75°C MIN	+75°C MAX	UNIT
Output Voltage	$V_{OL(5)}$	---	0.40	---	0.40	---	0.45	Vdc	---	0.45	---	0.45	---	0.50	Vdc
	$V_{OL(6)}$	---	0.40	---	0.40	---	0.45	Vdc	---	0.45	---	0.45	---	0.50	Vdc
	$V_{OL(8)}$	---	0.40	---	0.40	---	0.45	Vdc	---	0.45	---	0.45	---	0.50	Vdc
	$V_{OL(9)}$	---	0.40	---	0.40	---	0.45	Vdc	---	0.45	---	0.45	---	0.50	Vdc
	$V_{OH(5)}$	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
	$V_{OH(6)}$	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
	$V_{OH(8)}$	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
	$V_{OH(9)}$	2.50	---	2.60	---	2.40	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
Short-Circuit Current MC953/MC853	$I_{SC(5)}$	-1.45	-2.45	-1.30	-2.25	-1.15	-2.00	mAdc	-1.25	-2.50	-1.15	-2.30	-1.05	-2.15	mAdc
	$I_{SC(6)}$	-1.45	-2.45	-1.30	-2.25	-1.15	-2.00	mAdc	-1.25	-2.50	-1.15	-2.30	-1.05	-2.15	mAdc
	$I_{SC(8)}$	-1.45	-2.45	-1.30	-2.25	-1.15	-2.00	mAdc	-1.25	-2.50	-1.15	-2.30	-1.05	-2.15	mAdc
	$I_{SC(9)}$	-1.45	-2.45	-1.30	-2.25	-1.15	-2.00	mAdc	-1.25	-2.50	-1.15	-2.30	-1.05	-2.15	mAdc
MC956/MC856	$I_{SC(5)}$	-3.00	-5.10	-2.70	-4.60	-2.40	-4.10	mAdc	-2.60	-5.20	-2.35	-4.75	-2.20	-4.40	mAdc
	$I_{SC(6)}$	-3.00	-5.10	-2.70	-4.60	-2.40	-4.10	mAdc	-2.60	-5.20	-2.35	-4.75	-2.20	-4.40	mAdc
	$I_{SC(8)}$	-3.00	-5.10	-2.70	-4.60	-2.40	-4.10	mAdc	-2.60	-5.20	-2.35	-4.75	-2.20	-4.40	mAdc
	$I_{SC(9)}$	-3.00	-5.10	-2.70	-4.60	-2.40	-4.10	mAdc	-2.60	-5.20	-2.35	-4.75	-2.20	-4.40	mAdc
Reverse Current All Types	$I_{R(2)}$	---	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10	μAdc
	$I_{R(3)}$	---	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10	μAdc
	$I_{R(4)}$	--	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10	μAdc
	$I_{R(10)}$	---	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10	μAdc
	$I_{R(11)}$	---	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10	μAdc
	$I_{R(12)}$	---	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10	μAdc
	$I_{RCP(1)}$	---	10	---	10	---	20	μAdc	---	20	---	20	---	30	μAdc
MC953/MC853	$I_{RCP(13)}$	---	10	---	10	---	20	μAdc	---	20	---	20	---	30	μAdc
MC956/MC856	$I_{RCP(13)}$	---	10	---	10	---	20	μAdc	---	20	---	20	---	30	μAdc
Forward Current	$2/3I_{F(2)}$	---	-1.07	---	-1.07	---	-1.00	mAdc	---	-0.95	---	-0.95	---	-0.90	mAdc
	$2/3I_{F(3)}$	---	-1.07	---	-1.07	---	-1.00	mAdc	---	-0.95	---	-0.95	---	-0.90	mAdc
	$2/3I_{F(11)}$	---	-1.07	---	-1.07	---	-1.00	mAdc	---	-0.95	---	-0.95	---	-0.90	mAdc
	$2/3I_{F(12)}$	---	-1.07	---	-1.07	---	-1.00	mAdc	---	-0.95	---	-0.95	---	-0.90	mAdc
	$I_{FCP(1)}$	---	-3.20	---	-3.20	---	-3.00	mAdc	---	-2.80	---	-2.80	---	-2.67	mAdc
	$I_{FCP(13)}$	---	-3.20	---	-3.20	---	-3.00	mAdc	---	-2.80	---	-2.80	---	-2.67	mAdc
	$I_{FS(4)}$	---	-3.20	---	-3.20	---	-3.00	mAdc	---	-2.80	---	-2.80	---	-2.67	mAdc
	$I_{FS(10)}$	---	-3.20	---	-3.20	---	-3.00	mAdc	---	-2.80	---	-2.80	---	-2.67	mAdc
Power Drain Current															
MC953/MC853	$I_{MAX(14)}$	---	---	---	32	---	---	mAdc	---	---	---	36	---	---	mAdc
MC956/MC856	$I_{MAX(14)}$	---	---	---	38	---	---	mAdc	---	---	---	45	---	---	mAdc
MC953/MC853	$I_{PDH(14)}$	---	---	---	22	---	---	mAdc	---	---	---	28	---	---	mAdc
MC956/MC856	$I_{PDH(14)}$	---	---	---	27	---	---	mAdc	---	---	---	34	---	---	mAdc
Switching Time															
MC953/MC853	t_{pd+}	---	---	25	100	---	---	ns	---	---	25	100	---	---	ns
MC956/MC856	t_{pd+}	---	---	25	75	---	---	ns	---	---	25	75	---	---	ns
All Types	t_{pd-}	---	---	15	55	---	---	ns	---	---	15	55	---	---	ns
MC953/MC853	t_{pd+}	---	---	25	100	---	---	ns	---	---	25	100	---	---	ns
MC956/MC856	t_{pd+}	---	---	25	75	---	---	ns	---	---	25	75	---	---	ns
All Types	t_{pd-}	---	---	15	55	---	---	ns	---	---	15	55	---	---	ns

Pins not listed are left open

* * Applied after Clock Pulse

† CP_a - Clock Pulse a
†† CP_c - Clock Pulse c
Momentary Ground
} See Clock Pulse Waveforms

MC952/852, MC953/853, MC955/855, MC956/856 (continued)

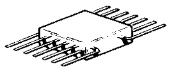
CHARACTERISTIC	SYMBOL PIN NO IN ( )	I_{OL} PIN	I_{OH} PIN	V_{IL} PIN	V_{IH} PIN	V_F PIN	V_R PIN	V_{CC} PIN	V_{CCL} PIN	V_{CCH} PIN	V_{PO} PIN	V_{MAX} PIN	CP_a^T Pin	CP_c^T Pin	Grounded Pin
TEST CONDITIONS		mA		VOLTS											
MC953/MC956 -55°C		①	-0.12	1.40	2.10	0	4.00	---	4.50	5.50	---	---			
MC953/MC956 +25°C		①	-0.12	1.10	2.00	0	4.00	5.00	4.50	5.50	5.00	8.00			
MC953/MC956 +125°C		①	-0.12	0.80	2.00	0	4.00	---	4.50	5.50	---	---			
MC853/MC856 0°C		①	-0.12	1.20	2.00	0.45	4.00	---	5.00	5.00	---	---			
MC853/MC856 +25°C		①	-0.12	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	8.00			
MC853/MC856 +75°C		①	-0.12	0.95	1.80	0.50	4.00	---	5.00	5.00	---	---			
Output Voltage	$V_{OL(5)}$	5		4					14						7
	$V_{OL(6)}$	6*		3					14					1	4^{π},7
	$V_{OL(8)}$	8*		11					14					13	7,10^{π}
	$V_{OL(9)}$	9		10					14						7
	$V_{OH(5)}$		5*	3	2				14				1		4^{π},7
	$V_{OH(6)}$		6	3,4					14				1		7
	$V_{OH(8)}$		8	10,11					14				13		7
	$V_{OH(9)}$		9*	11	12				14				13		7, 10^{π}
Short-Circuit Current MC953/MC853	$I_{SC(5)}$									14				1	5,7
	$I_{SC(6)}$									14				1	6,7
	$I_{SC(8)}$									14				13	7,8
	$I_{SC(9)}$									14				13	7,9
MC956/MC856	$I_{SC(5)}$									14				1	5,7
	$I_{SC(6)}$									14				1	6,7
	$I_{SC(8)}$									14				13	7,8
	$I_{SC(9)}$									14				13	7,9
Reverse Current All Types	$I_{R(2)}$						2			14					1,7
	$I_{R(3)}$						3			14					1,7
	$I_{R(4)}$						4			14					2,6,7
	$I_{R(10)}$						10			14					7,8,12
	$I_{R(11)}$						11			14					7,13
	$I_{R(12)}$						12			14					7,13
	$I_{RCP(1)}$						1,14								2,3,5,6,7
MC953/MC853	$I_{RCP(13)}$						13,14								7,8,9,11,12
MC956/MC856	$I_{RCP(13)}$						13			14					7,8,9,11,12
Forward Current	$2/3I_{F(2)}$					2				14				1	7
	$2/3I_{F(3)}$					3				14				1	7
	$2/3I_{F(11)}$					11				14				13	7
	$2/3I_{F(12)}$					12				14				13	7
	$I_{FCP(1)}$			4		1				14					7
	$I_{FCP(13)}$			10		13				14					7
	$I_{FS(4)}$					4				14					3,7
	$I_{FS(10)}$					10				14					7,11
Power Drain Current															
MC953/MC853	$I_{MAX(14)}$											14			1,2,3,4,7,10,11,12,13
MC956/MC856	$I_{MAX(14)}$											14			1,2,3,4,7,10,11,12,13
MC953/MC853	$I_{PDH(14)}$										14				7
MC956/MC856	$I_{PDH(14)}$										14				7
Switching Time		Pulse In	Pulse Out												
MC953/MC853	t_{pd+}	1	6					14							7
MC956/MC856	t_{pd+}	1	6					14							7
All Types	t_{pd-}	1	6					14							7
MC953/MC853	t_{pd+}	13	8					14							7
MC956/MC856	t_{pd+}	13	8					14							7
All Types	t_{pd-}	13	8					14							7

①I_{OL} Values (mA):

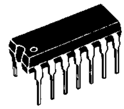
	MC953	MC956
-55°C	14.6	13.0
+25°C	15.2	13.6
+125°C	13.8	12.3

	MC853	MC856
0°C	16.8	15.4
+25°C	16.8	15.4
+75°C	16.0	14.6

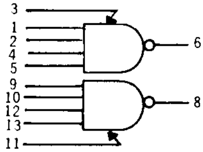
MC961F
MC861F, P



TO-86
CASE 83
SUFFIX F



UNIBLOC
PLASTIC PACKAGE
CASE 93
SUFFIX P

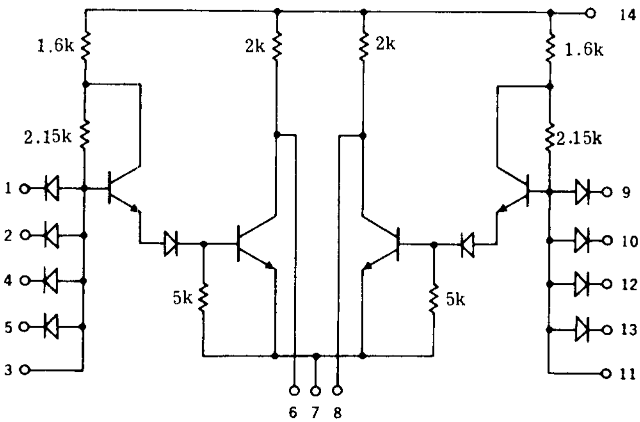


MDTL EXPANDABLE DUAL 4-INPUT "NAND/NOR" GATES (Additions to MC930/MC830 Series)

t_{pd} = 25 ns typ
P_D = 33 mW typ
Input Loading Factor = 1
Fan-Out = 7

Positive Logic:
$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot (3)}$
$8 = \overline{9 \cdot 10 \cdot 12 \cdot 13 \cdot (11)}$

FIGURE 1 — CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

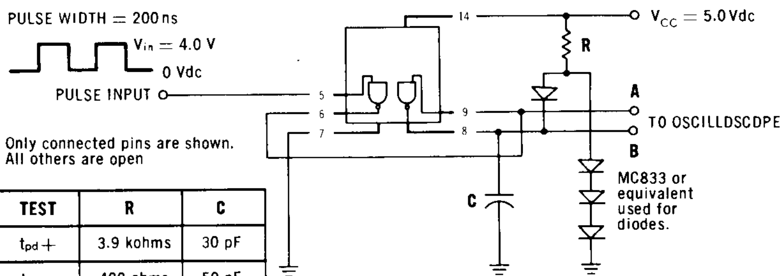
Test procedures are shown for one gate only. The other gate is tested in the same manner.

Characteristic	Symbol Pin No in( )	MC961 Test Limits −55°C Min	Max	+25°C Min	Max	+125°C Min	Max	Unit	MC861 Test Limits 0°C Min	Max	+25°C Min	Max	+75°C Min	Max
Output Voltage	V_{OL}(6)	—	0.40	—	0.40	—	0.45	Vdc	—	0.45	—	0.45	—	0.50
	V_{OH}(6)	2.50	—	2.60	—	2.50	—	Vdc	2.60	—	2.60	—	2.50	—
	V_{OH}(6)	2.50	—	2.60	—	2.50	—	Vdc	2.60	—	2.60	—	2.50	—
	V_{OH}(6)	2.50	—	2.60	—	2.50	—	Vdc	2.60	—	2.60	—	2.50	—
	V_{OH}(6)	2.50	—	2.60	—	2.50	—	Vdc	2.60	—	2.60	—	2.50	—
	V_{OH}(6)	2.50	—	2.60	—	2.50	—	Vdc	2.60	—	2.60	—	2.50	—
Short-Circuit Current	I_{SC}(6)	—	−4.0	—	−4.0	—	−3.9	mAdc	—	−3.9	—	−3.9	—	−3.75
Reverse Current	I_R(1)	—	2.0	—	2.0	—	5.0	µAdc	—	5.0	—	5.0	—	10
	I_R(2)	—	2.0	—	2.0	—	5.0	µAdc	—	5.0	—	5.0	—	10
	I_R(4)	—	2.0	—	2.0	—	5.0	µAdc	—	5.0	—	5.0	—	10
	I_R(5)	—	2.0	—	2.0	—	5.0	µAdc	—	5.0	—	5.0	—	10
Output Leakage Current	I_{CEX}(6)	—	—	—	50	—	—	µAdc	—	—	—	100	—	—
Forward Current	I_F(1)	—	−1.60	—	−1.60	—	−1.50	mAdc	—	−1.40	—	−1.40	—	−1.33
	I_F(2)	—	−1.60	—	−1.60	—	−1.50	mAdc	—	−1.40	—	−1.40	—	−1.33
	I_F(4)	—	−1.60	—	−1.60	—	−1.50	mAdc	—	−1.40	—	−1.40	—	−1.33
	I_F(5)	—	−1.60	—	−1.60	—	−1.50	mAdc	—	−1.40	—	−1.40	—	−1.33
Power Drain Current	I_{PDH}(14)	—	—	—	10.7	—	—	mAdc	—	—	—	13.1	—	—
	I_{max}(14)	—	—	—	5.50	—	—	mAdc	—	—	—	8.0	—	—
Switching Time (Pin 6 connected to Pin 9)	$t_{pd}+$	—	—	15	60	—	—	ns	—	—	15	60	—	—
	$t_{pd}-$	—	—	10	30	—	—	ns	—	—	10	30	—	—

Pins not listed are left open

MC961F/MC861F, P (continued)

FIGURE 2 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

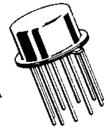


TEST	R	C
$t_{pd}+$	3.9 kohms	30 pF
$t_{pd}-$	400 ohms	50 pF

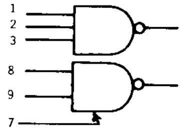
@ Test Temperature		Test Conditions: mA		Volts											
MC961	−55°C	10.4	−0.12	1.40	2.10	—	0	4.00	—	—	4.50	5.50	—	—	
	+25°C	11.0	−0.12	1.10	2.00	1.80	0	4.00	4.50	5.00	4.50	5.50	5.00	8.00	
	+125°C	9.8	−0.12	0.00	2.00	—	0	4.00	—	—	4.50	5.50	—	—	
MC061	0°C	11.0	−0.12	1.20	2.00	—	0.45	4.00	—	—	5.00	5.00	—	—	
	+25°C	11.0	−0.12	1.10	1.90	1.80	0.45	4.00	5.00	5.00	5.00	5.00	5.00	8.00	
	+75°C	10.4	−0.12	0.95	1.80	—	0.50	4.00	—	—	5.00	5.00	—	—	
Characteristic	**Symbol** Pin No in ( )	I_{OL} Pin No	I_{OH} Pin No	V_{IL} Pin No	V_{IH} Pin No	V_X Pin No	V_F Pin No	V_R Pin No	V_{CEX} Pin No	V_{CC} Pin No	V_{CCL} Pin No	V_{CCH} Pin No	V_{PD} Pin No	V_{max} Pin No	**Grounded** Pin No
Output Voltage	V_{OL}(6)	6	—	—	1, 2, 4, 5	—	—	—	—	—	14	—	—	—	7
	V_{OH}(6)	—	6	1	—	—	—	—	—	—	14	—	—	—	7
	V_{OH}(6)	—	6	2	—	—	—	—	—	—	14	—	—	—	7
	V_{OH}(6)	—	6	4	—	—	—	—	—	—	14	—	—	—	7
	V_{OH}(6)	—	6	5	—	—	—	—	—	—	14	—	—	—	7
	V_{OH}(6)	—	6	—	—	3	—	—	—	—	14	—	—	—	7
Short-Circuit Current	I_{SC}(6)	—	—	—	—	—	—	—	—	—	—	14	—	—	1, 6, 7
Reverse Current	I_R(1)	—	—	—	—	—	—	1	—	—	—	14	—	—	2, 4, 5, 7
	I_R(2)	—	—	—	—	—	—	2	—	—	—	14	—	—	1, 4, 5, 7
	I_R(4)	—	—	—	—	—	—	4	—	—	—	14	—	—	1, 2, 5, 7
	I_R(5)	—	—	—	—	—	—	5	—	—	—	14	—	—	1, 2, 4, 7
Output Leakage Current	I_{CEX}(6)	—	—	—	—	—	—	—	6, 14	—	—	—	—	—	1, 7
Forward Current	I_F(1)	—	—	—	—	—	1	2, 4, 5	—	—	—	14	—	—	7
	I_F(2)	—	—	—	—	—	2	1, 4, 5	—	—	—	14	—	—	7
	I_F(4)	—	—	—	—	—	4	1, 2, 5	—	—	—	14	—	—	7
	I_F(5)	—	—	—	—	—	5	1, 2, 4	—	—	—	14	—	—	7
Power Drain Current	I_{PDH}(14)	—	—	—	—	—	—	—	—	—	—	—	14	—	7
	I_{max}(14)	—	—	—	—	—	—	—	—	—	—	—	—	14	1, 7, 9
Switching Time (Pin 6 connected to Pin 9)		Pulse In	Pulse Out												
	$t_{pd}+$	9	8	—	—	—	—	—	—	14	—	—	—	—	7
	$t_{pd}-$	9	8	—	—	—	—	—	—	14	—	—	—	—	7

Pins not listed are left open

MC961G
MC861G



CASE 96A
TO-100

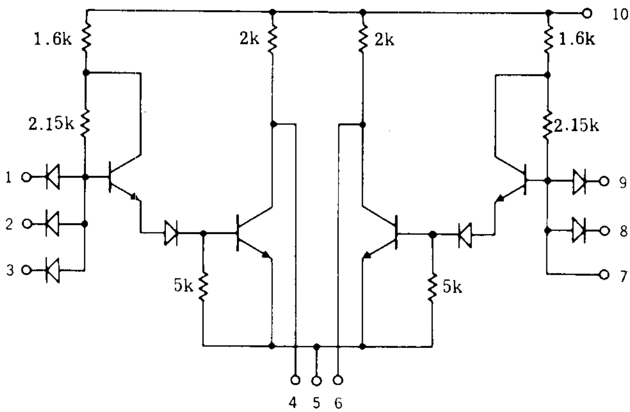


MDTL EXPANDABLE DUAL 2-3 INPUT "NAND/NOR" GATES (Additions to MC930/MC830 Series)

t_{pd} = 25 ns typ
P_D = 33 mW typ
Input Loading Factor = 1
Fan-Out = 7

Positive Logic:
$4 = \overline{1 \cdot 2 \cdot 3}$
$6 = \overline{8 \cdot 9 \cdot (7)}$

FIGURE 1 — CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

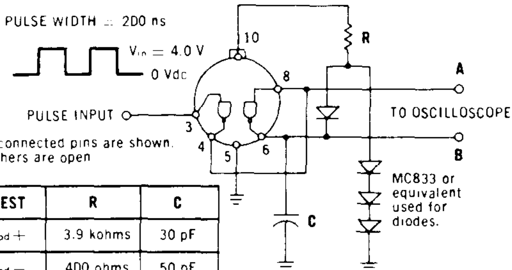
Test procedures are shown for one gate only. The other gate is tested in the same manner.

Characteristic	Symbol Pin No in ( )	MC961 Test Limits −55°C Min	Max	+25°C Min	Max	+125°C Min	Max	Unit	MC861 Test Limits 0°C Min	Max	+25°C Min	Max	+75°C Min	Max
Output Voltage	V_{OL}(6)	—	0.40	—	0.40	—	0.45	Vdc	—	0.45	—	0.45	—	0.50
	V_{OH}(6)	2.50	—	2.60	—	2.50	—	Vdc	2.60	—	2.60	—	2.50	—
	V_{OH}(6)	2.50	—	2.60	—	2.50	—	Vdc	2.60	—	2.60	—	2.50	—
	V_{OH}(6)	—	—	2.60	—	—	—	Vdc	—	—	2.60	—	—	—
Short-Circuit Current	I_{SC}(6)	—	−4.0	—	−4.0	—	−3.9	mAdc	—	−3.9	—	−3.9	—	−3.75
Reverse Current	I_R(8)	—	2.0	—	2.0	—	5.0	μAdc	—	5.0	—	5.0	—	10
	I_R(9)	—	2.0	—	2.0	—	5.0	μAdc	—	5.0	—	5.0	—	10
Output Leakage Current	I_{CEX}(6)	—	—	—	50	—	—	μAdc	—	—	—	100	—	—
Forward Current	I_F(8)	—	−1.60	—	−1.60	—	−1.50	mAdc	—	−1.40	—	−1.40	—	−1.33
	I_F(9)	—	−1.60	—	−1.60	—	−1.50	mAdc	—	−1.40	—	−1.40	—	−1.33
Power Drain Current	I_{PDH}(10)	—	—	—	10.7	—	—	mAdc	—	—	—	13.1	—	—
	I_{max}(10)	—	—	—	5.5	—	—	mAdc	—	—	—	8.0	—	—
Switching Time (Pin 4 connected to Pin 8)	$t_{pd}+$	—	—	15	60	—	—	ns	—	—	15	60	—	—
	$t_{pd}-$	—	—	10	30	—	—	ns	—	—	10	30	—	—

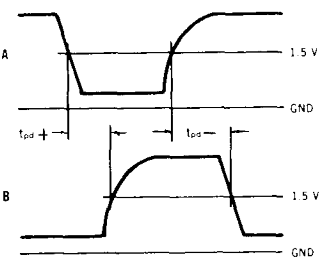
Pins not listed are left open

MC961G/MC861G (continued)

FIGURE 2 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST	R	C
$t_{pd}+$	3.9 kohms	30 pF
$t_{pd}-$	400 ohms	50 pF

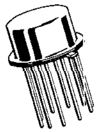


Characteristic	Symbol Pin No in ( )	I_{OL} Pin No	I_{OH} Pin No	V_{IL} Pin No	V_{IH} Pin No	V_X Pin No	V_F Pin No	V_R Pin No	V_{CEX} Pin No	V_{CC} Pin No	V_{CCL} Pin No	V_{CCH} Pin No	V_{PD} Pin No	V_{max} Pin No	Grounded Pin No
@ Test Temperature		**Test Conditions** mA		Volts											
MC961	−55°C	10.4	−0.12	1.40	2.10	—	0	4.00	—	—	4.50	5.50	—	—	
	+25°C	11.0	−0.12	1.18	2.08	1.88	0	4.00	4.50	5.00	4.50	5.50	5.08	8.00	
	+125°C	9.8	−0.12	0.80	2.08	—	0	4.00	—	—	4.50	5.58	—	—	
MC861	8°C	11.0	−8.12	1.28	2.00	—	0.45	—	5.00	—	5.80	5.88	—	—	
	+25°C	11.0	−8.12	1.18	1.98	1.80	8.45	5.00	5.00	5.80	5.08	5.88	5.88	8.88	
	+75°C	10.4	−0.12	8.95	1.88	—	8.58	—	5.80	—	5.00	5.88	—	—	
Output Voltage	V_{OL}(6)	6	—	—	8, 9	—	—	—	—	—	10	—	—	—	5
	V_{OH}(6)	—	6	8	—	—	—	—	—	—	10	—	—	—	5
	V_{OH}(6)	—	6	9	—	—	—	—	—	—	10	—	—	—	5
	V_{OH}(6)	—	6	—	—	7	—	—	—	—	10	—	—	—	5
Short-Circuit Current	I_{SC}(6)								—	—	—	10	—	—	5, 6, 8
Reverse Current	I_R(8)	—	—	—	—	—	—	8	—	—	—	10	—	—	5, 9
	I_R(9)	—	—	—	—	—	—	9	—	—	—	10	—	—	5, 8
Output Leakage Current	I_{CEX}(6)	—	—	—	—	—	—	—	6, 10	—	—	—	—	—	5, 8
Forward Current	I_F(8)	—	—	—	—	—	8	9	—	—	—	10	—	—	5
	I_F(9)	—	—	—	—	—	9	8	—	—	—	10	—	—	5
Power Drain Current	I_{PDH}(10)	—	—	—	—	—	—	—	—	—	—	—	10	—	5
	I_{max}(10)	—	—	—	—	—	—	—	—	—	—	—	—	10	1, 5, 8
Switching Time (Pin 4 connected to Pin 8)		Pulse In	Pulse Out												
	$t_{pd}+$	8	6	—	—	—	—	—	—	10	—	—	—	—	5
	$t_{pd}-$	8	6	—	—	—	—	—	—	10	—	—	—	—	5

Pins not listed are left open

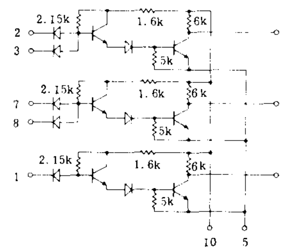
MC962G
MC862G

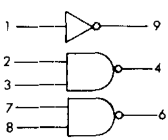
MDTL DUAL 2-INPUT "NAND/NOR" GATE PLUS INVERTER (Additions to MC930/MC830 Series)



CASE 96A
TO-100

FIGURE 1 — CIRCUIT SCHEMATIC





t_{pd} = 30 ns typ
P_D = 30 mW typ
Input Loading Factor = 1
Fan-Out = 8

Positive Logic:
$4 = \overline{2 \cdot 3}$
$6 = \overline{7 \cdot 8}$
$9 = \overline{1}$

ELECTRICAL CHARACTERISTICS

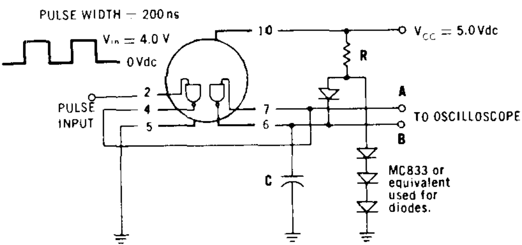
Test procedures are shown for inverter and one gate only. The other gate is tested in the same manner.

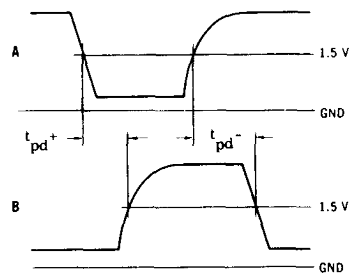
CHARACTERISTIC	SYMBOL PIN IN ( )	MC962G TEST LIMITS -55°C MIN	MAX	+25°C MIN	MAX	+125°C MIN	MAX	UNIT	MC862G TEST LIMITS 0°C MIN	MAX	+25°C MIN	MAX	+75°C MIN	MAX	UNIT
Output Voltage	$V_{OL(4)}$	---	0.40	---	0.40	---	0.45	Vdc	---	0.45	---	0.45	---	0.50	Vdc
	$V_{OL(9)}$	---	0.40	---	0.40	---	0.45	Vdc	---	0.45	---	0.45	---	0.50	Vdc
	$V_{OH(4)}$	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
	$V_{OH(4)}$	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
	$V_{OH(9)}$	2.50	---	2.60	---	2.50	---	Vdc	2.60	---	2.60	---	2.50	---	Vdc
Short-Circuit Current	$I_{SC(4)}$	---	-1.34	---	-1.34	---	-1.30	mAdc	---	-1.30	---	-1.30	---	-1.25	mAdc
	$I_{SC(9)}$	---	-1.34	---	-1.34	---	-1.30	mAdc	---	-1.30	---	-1.30	---	-1.25	mAdc
Reverse Current	$I_{R(1)}$	---	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10	μAdc
	$I_{R(2)}$	---	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10	μAdc
	$I_{R(3)}$	---	2.0	---	2.0	---	5.0	μAdc	---	5.0	---	5.0	---	10	μAdc
Output Leakage Current	$I_{CEX(4)}$	---	---	---	50	---	---	μAdc	---	---	---	100	---	---	μAdc
	$I_{CEX(9)}$	---	---	---	50	---	---	μAdc	---	---	---	100	---	---	μAdc
Forward Current	$I_{F(1)}$	---	-1.60	---	-1.60	---	-1.50	mAdc	---	-1.40	---	-1.40	---	-1.33	mAdc
	$I_{F(2)}$	---	-1.60	---	-1.60	---	-1.50	mAdc	---	-1.40	---	-1.40	---	-1.33	mAdc
	$I_{F(3)}$	---	-1.60	---	-1.60	---	-1.50	mAdc	---	-1.40	---	-1.40	---	-1.33	mAdc
Power Drain Current	$I_{PDH(10)}$	---	---	---	9.75	---	---	mAdc	---	---	---	12	---	---	mAdc
	$I_{MAX(10)}$	---	---	---	8.25	---	---	mAdc	---	---	---	12	---	---	mAdc
Switching Time (Fig.2) (Pin 4 connected to Pin 7)	t_{pd+}	---	---	25	80	---	---	ns	---	---	25	80	---	---	ns
	t_{pd-}	---	---	10	30	---	---	ns	---	---	10	30	---	---	ns

Pins not listed are left open.

MC962G/MC862G (continued)

FIGURE 2 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





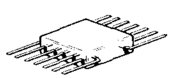
TEST	R	C
$t_{pd}+$	3.9 kohms	30 pF
$t_{pd}-$	400 ohms	50 pF

Only connected pins are shown. All others are open

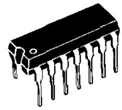
@ Test Temperature		TEST CONDITIONS mA		VOLTS									
MC962G	-55°C	11.4	-0.12	1.40	2.10	0	4.00	---	---	4.50	5.50	----	----
	+25°C	12.0	-0.12	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	5.00	8.00
	+125°C	10.8	-0.12	0.80	2.00	0	4.00	---	---	4.50	5.50	---	---
MC862G	0°C	12.0	-0.12	1.20	2.00	0.45	4.00	---	---	5.00	5.00	---	---
	+25°C	12.0	-0.12	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	5.00	8.00
	+75°C	11.4	-0.12	0.95	1.80	0.50	4.00	---	---	5.00	5.00	---	---

CHARACTERISTIC	SYMBOL PIN IN ( )	I_{OL} PIN	I_{OH} PIN	V_{IL} PIN	V_{IH} PIN	V_F PIN	V_R PIN	V_{CEX} PIN	V_{CC} PIN	V_{CCL} PIN	V_{CCH} PIN	V_{PD} PIN	V_{MAX} PIN	GROUNDED PIN
Output Voltage	$V_{OL(4)}$	4			2,3					10				5
	$V_{OL(9)}$	9			1					10				5
	$V_{OH(4)}$		4	2						10				5
	$V_{OH(4)}$		4	3						10				5
	$V_{OH(9)}$		9	1						10				5
Short-Circuit Current	$I_{SC(4)}$										10			2,4,5
	$I_{SC(9)}$										10			1,5,9
Reverse Current	$I_{R(1)}$						1				10			5
	$I_{R(2)}$						2				10			3,5
	$I_{R(3)}$						3				10			2,5
Output Leakage Current	$I_{CEX(4)}$							4,10						2,5
	$I_{CEX(9)}$							9,10						1,5
Forward Current	$I_{F(1)}$					1					10			5
	$I_{F(2)}$					2	3				10			5
	$I_{F(3)}$					3	2				10			5
Power Drain Current	$I_{POH(10)}$										10			5
	$I_{MAX(10)}$												10	1,2,5,7
Switching Time (Fig.2) (Pin 4 connected to Pin 7)		Pulse In	Pulse Out											
	t_{pd+}	2	7						10					5
	t_{pd-}	2	7						10					5

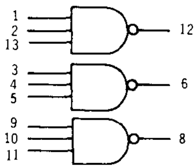
MC963F
MC863F, P



TO-86
CASE 83
SUFFIX F



UNIBLOCK
PLASTIC PACKAGE
CASE 93
SUFFIX P

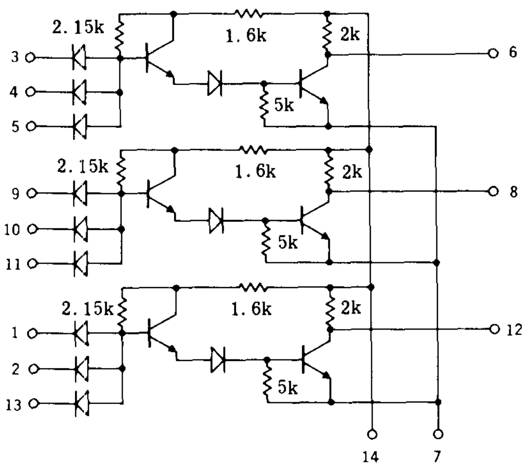


MDTL TRIPLE 3-INPUT "NAND/NOR" GATES (Additions to MC930/MC830 Series)

t_{pd} = 25 ns typ
P_D = 50 mW typ
Input Loading Factor = 1
Fan-Out = 7

Positive Logic:
$6 = \overline{3 \cdot 4 \cdot 5}$
$8 = \overline{9 \cdot 10 \cdot 11}$
$12 = \overline{13 \cdot 1 \cdot 2}$

FIGURE 1 — CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

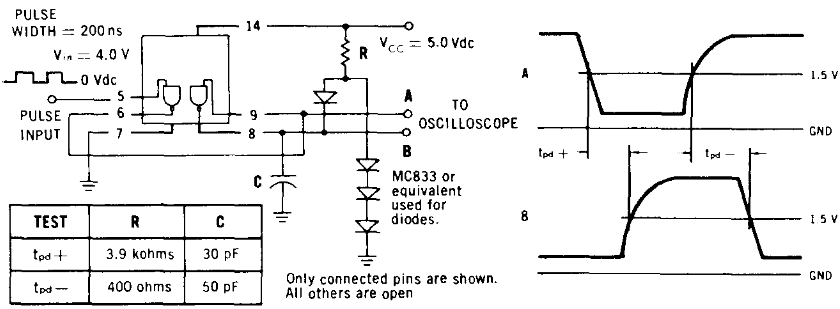
Test procedures are shown for one gate only. Other gates are tested in the same manner.

Characteristic	Symbol Pin No in ( )	MC963 Test Limits						Unit	MC863 Test Limits					
		−55°C		+25°C		+125°C			0°C		+25°C		+75°C	
		Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max
Output Voltage	V_{OL}(6)	—	0.40	—	0.40	—	0.45	Vdc	—	0.45	—	0.45	—	0.50
	V_{OH}(6)	2.50	—	2.60	—	2.50	—	Vdc	2.60	—	2.60	—	2.50	—
	V_{OH}(6)	2.50	—	2.60	—	2.50	—	Vdc	2.60	—	2.60	—	2.50	—
	V_{OH}(6)	2.50	—	2.60	—	2.50	—	Vdc	2.60	—	2.60	—	2.50	—
Short-Circuit Current	I_{SC}(6)	—	−4.0	—	−4.0	—	−3.9	mAdc	—	−3.9	—	−3.9	—	−3.75
Reverse Current	I_R(3)	—	2.0	—	2.0	—	5.0	μAdc	—	5.0	—	5.0	—	10
	I_R(4)	—	2.0	—	2.0	—	5.0	μAdc	—	5.0	—	5.0	—	10
	I_R(5)	—	2.0	—	2.0	—	5.0	μAdc	—	5.0	—	5.0	—	10
Output Leakage Current	I_{CEX}(6)	—	—	—	50	—	—	μAdc	—	—	—	100	—	—
Forward Current	I_F(3)	—	−1.60	—	−1.60	—	−1.50	mAdc	—	−1.40	—	−1.40	—	−1.33
	I_F(4)	—	−1.60	—	−1.60	—	−1.50	mAdc	—	−1.40	—	−1.40	—	−1.33
	I_F(5)	—	−1.60	—	−1.60	—	−1.50	mAdc	—	−1.40	—	−1.40	—	−1.33
Power Drain Current	I_{PDH}(14)	—	—	—	16.0	—	—	mAdc	—	—	—	19.6	—	—
	I_{max}(14)	—	—	—	8.25	—	—	mAdc	—	—	—	12.0	—	—
Switching Time (Pin 6 connected to Pin 9)	—	—	—	15	60	—	—	ns	—	—	15	60	—	—
	—	—	—	10	30	—	—	ns	—	—	10	30	—	—

Pins not listed are left open

MC963F/MC863F, P (continued)

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

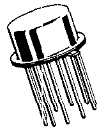


TEST	R	C
$t_{pd}+$	3.9 kohms	30 pF
$t_{pd}-$	400 ohms	50 pF

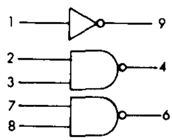
Characteristic	Symbol Pin No in ( )	I_{OL} Pin No	I_{OH} Pin No	V_{IL} Pin No	V_{IH} Pin No	V_F Pin No	V_R Pin No	V_{CEX} Pin No	V_{CC} Pin No	V_{CCL} Pin No	V_{CCH} Pin No	V_{PD} Pin No	V_{max} Pin No	Grounded Pin No
@ Test Temperature		Test Conditions: mA		Volts										
MC963	−55°C	10.4	−8.12	1.40	2.18	0	4.08	—	—	4.50	5.58	—	—	
MC963	+25°C	11.0	−8.12	1.18	2.80	0	4.80	4.50	5.00	4.50	5.58	5.00	8.00	
MC963	+125°C	9.8	−0.12	8.80	2.08	8	4.80	—	—	4.58	5.50	—	—	
MC863	0°C	11.0	−0.12	1.28	2.00	0.45	—	5.00	—	5.00	5.00	—	—	
MC863	+25°C	11.0	−0.12	1.18	1.90	0.45	5.00	5.88	5.00	5.80	5.08	5.00	8.80	
MC863	+75°C	10.4	−8.12	0.95	1.80	0.50	—	5.00	—	5.00	5.00	—	—	
Output Voltage	V_{OL}(6)	6	—	—	3, 4, 5	—	—	—	—	14	—	—	—	7
	V_{OH}(6)	—	6	3	—	—	—	—	—	14	—	—	—	7
	V_{OH}(6)	—	6	4	—	—	—	—	—	14	—	—	—	7
	V_{OH}(6)	—	6	5	—	—	—	—	—	14	—	—	—	7
Short-Circuit Current	I_{SC}(6)	—	—	—	—	—	—	—	—	—	14	—	—	3, 6, 7
Reverse Current	I_R(3)	—	—	—	—	—	3	—	—	—	14	—	—	4, 5, 7
	I_R(4)	—	—	—	—	—	4	—	—	—	14	—	—	3, 5, 7
	I_R(5)	—	—	—	—	—	5	—	—	—	14	—	—	3, 4, 7
Output Leakage Current	I_{CEX}(6)	—	—	—	—	—	—	6, 14	—	—	—	—	—	3, 7
Forward Current	I_F(3)	—	—	—	—	3	4, 5	—	—	—	14	—	—	7
	I_F(4)	—	—	—	—	4	3, 5	—	—	—	14	—	—	7
	I_F(5)	—	—	—	—	5	3, 4	—	—	—	14	—	—	7
Power Drain Current	I_{PDH}(14)	—	—	—	—	—	—	—	—	—	—	14	—	7
	I_{max}(14)	—	—	—	—	—	—	—	—	—	—	—	14	3, 7, 9, 13
Switching Time (Pin 6 connected to Pin 9)		Pulse In	Pulse Out											
	—	9	8	—	—	—	—	—	14	—	—	—	—	7
	—	9	8	—	—	—	—	—	14	—	—	—	—	7

Pins not listed are left open

MC963G
MC863G



CASE 96A
SUFFIX G



t_{pd} = 25 ns typ

P_D = 45 mW typ

Input Loading Factor = 1

Fan-Out = 7

Positive Logic:

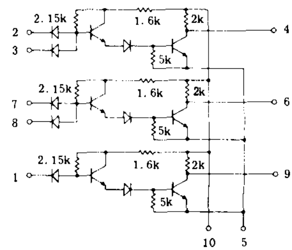
4 = $\overline{2 \cdot 3}$

6 = $\overline{7 \cdot 8}$

9 = $\overline{1}$

MDTL DUAL 2-INPUT "NAND/NOR" GATE PLUS INVERTER (Additions to MC930/MC830 Series)

FIGURE 1 — CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Test procedures are shown for the inverter and one gate only.

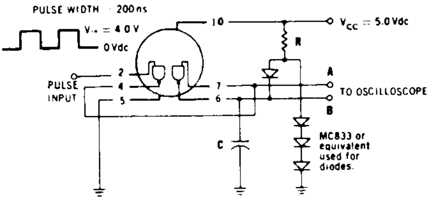
The other gate is tested in the same manner.

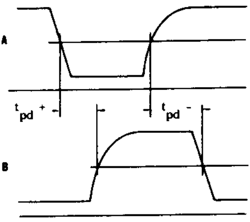
CHARACTERISTIC	SYMBOL PIN IN ( )	MC963G TEST LIMITS -55°C MIN	MAX	+25°C MIN	MAX	+125°C MIN	MAX	UNIT	MC863G TEST LIMITS 0°C MIN	MAX	+25°C MIN	MAX	+75°C MIN	MAX	UNIT
Output Voltage	$V_{OL(4)}$	—	0.40	—	0.40	—	0.45	Vdc	—	0.45	—	0.45	—	0.50	Vdc
	$V_{OL(9)}$	—	0.40	—	0.40	—	0.45	Vdc	—	0.45	—	0.45	—	0.50	Vdc
	$V_{OH(4)}$	2.50	—	2.60	—	2.50	—	Vdc	2.60	—	2.60	—	2.50	—	Vdc
	$V_{OH(4)}$	2.50	—	2.60	—	2.50	—	Vdc	2.60	—	2.60	—	2.50	—	Vdc
	$V_{OH(9)}$	2.50	—	2.60	—	2.50	—	Vdc	2.60	—	2.60	—	2.50	—	Vdc
Short-Circuit Current	$I_{SC(4)}$	—	-4.0	—	-4.0	—	-3.9	mAdc	—	-3.9	—	-3.9	—	-3.75	mAdc
	$I_{SC(9)}$	—	-4.0	—	-4.0	—	-3.9	mAdc	—	-3.9	—	-3.9	—	-3.75	mAdc
Reverse Current	$I_{R(1)}$	—	2.0	—	2.0	—	5.0	μAdc	—	5.0	—	5.0	—	10	μAdc
	$I_{R(2)}$	—	2.0	—	2.0	—	5.0	μAdc	—	5.0	—	5.0	—	10	μAdc
	$I_{R(3)}$	—	2.0	—	2.0	—	5.0	μAdc	—	5.0	—	5.0	—	10	μAdc
Output Leakage Current	$I_{CEX(4)}$	—	—	—	50	—	—	μAdc	—	—	—	100	—	—	μAdc
	$I_{CEX(9)}$	—	—	—	50	—	—	μAdc	—	—	—	100	—	—	μAdc
Forward Current	$I_{F(1)}$	—	-1.60	—	-1.60	—	-1.50	mAdc	—	-1.40	—	-1.40	—	-1.33	mAdc
	$I_{F(2)}$	—	-1.60	—	-1.60	—	-1.50	mAdc	—	-1.40	—	-1.40	—	-1.33	mAdc
	$I_{F(3)}$	—	-1.60	—	-1.60	—	-1.50	mAdc	—	-1.40	—	-1.40	—	-1.33	mAdc
Power Drain Current	$I_{POH(10)}$	—	—	—	16.0	—	—	mAdc	—	—	—	19.6	—	—	mAdc
	$I_{MAX(10)}$	—	—	—	8.25	—	—	mAdc	—	—	—	12.0	—	—	mAdc
Switching Time (Fig. 2) (Pin 4 connected to Pin 7)	t_{pd+}	—	—	15	60	—	—	ns	—	—	15	60	—	—	ns
	t_{pd-}	—	—	10	30	—	—	ns	—	—	10	30	—	—	ns

Pins not listed are left open.

MC963G/MC863G (continued)

FIGURE 2 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





TEST	R	C
t_{pd} +	3.9 kohms	30 pF
t_{pd} −	400 ohms	50 pF

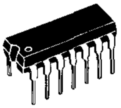
Only connected pins are shown
All others are open

CHARACTERISTIC	SYMBOL PIN IN ( )	I_{OL} PIN	I_{OH} PIN	V_{IL} PIN	V_{IH} PIN	V_F PIN	V_R PIN	V_{CEX} PIN	V_{CC} PIN	V_{CCL} PIN	V_{CCH} PIN	V_{PD} PIN	V_{MAX} PIN	GROUNDED PIN
@ Test Temperature		TEST CONDITIONS mA		VOLTS										
MC963G	-55°C	10.4	-0.12	1.40	2.10	0	4.00	---	---	4.50	5.50	---	---	
MC963G	+25°C	11.0	-0.12	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	5.00	8.00	
MC963G	+125°C	9.8	-0.12	0.80	2.00	0	4.00	---	---	4.50	5.00	---	---	
MC863G	0°C	11.0	-0.12	1.20	2.00	0.45	4.00	---	---	5.00	5.00	---	---	
MC863G	+25°C	11.0	-0.12	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	5.00	8.00	
MC863G	+75°C	10.4	-0.12	0.95	1.80	0.50	4.00	---	---	5.00	5.00	---	---	
Output Voltage	$V_{OL(4)}$	4			2,3					10				5
	$V_{OL(9)}$	9			1					10				5
	$V_{OH(4)}$		4	2						10				5
	$V_{OH(4)}$		4	3						10				5
	$V_{OH(9)}$		9	1						10				5
Short-Circuit Current	$I_{SC(4)}$										10			2,4,5
	$I_{SC(9)}$										10			1,5,9
Reverse Current	$I_{R(1)}$						1				10			5
	$I_{R(2)}$						2				10			3,5
	$I_{R(3)}$						3				10			2,5
Output Leakage Current	$I_{CEX(4)}$							4,10						2,5
	$I_{CEX(9)}$							9,10						1,5
Forward Current	$I_{F(1)}$					1					10			5
	$I_{F(2)}$					2	3				10			5
	$I_{F(3)}$					3	2				10			5
Power Drain Current	$I_{POH(10)}$											10		5
	$I_{MAX(10)}$												10	1,2,5,7
Switching Time (Fig. 2) (Pin 4 connected to Pin 7)		Pulse In	Pulse Out											
	t_{pd+}	2	7						10					5
	t_{pd-}	2	7						10					5

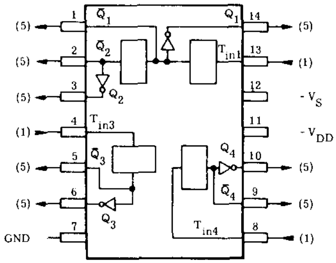
Pins not listed are left open.

MC1124P
MOS FREQUENCY DIVIDER

MOS integrated circuit frequency divider, a monolithic circuit consisting of four flip-flops with single rail inputs and Q and $\overline{Q}$ outputs.



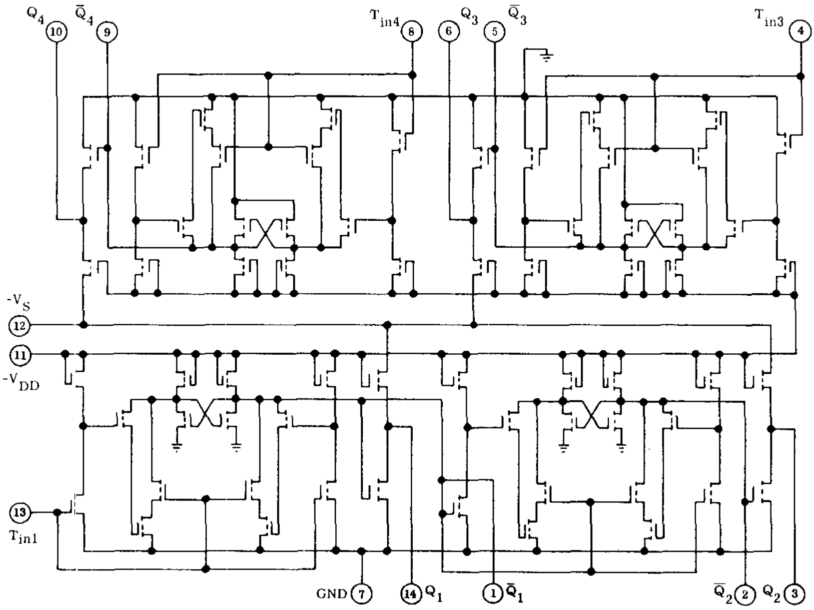
UNIBLOC
PLASTIC PACKAGE
CASE 93



Number in parenthesis = loading factor

NOTE: To cascade flip-flop stages, connect $\overline{Q}$ (trigger out) to T_{in} (trigger in) of the next stage.

CIRCUIT SCHEMATIC



MC1124P (continued)

MAXIMUM RATINGS

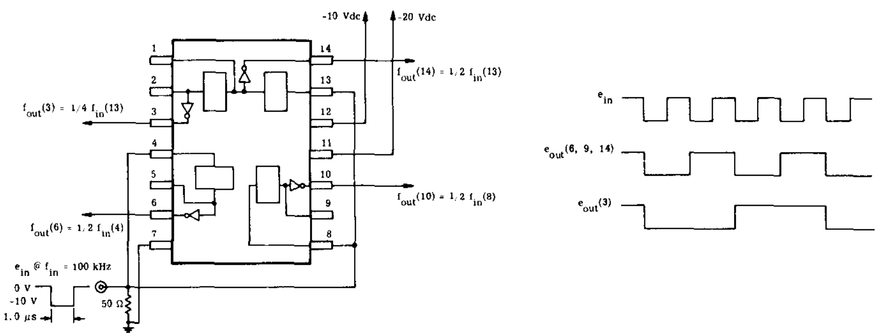
Rating	Symbol	Value	Unit
Drain Voltage	V_{DD}	-40 to +0.3	Vdc
Trigger Input Voltage	V_{in}	-30 to +0.3	Vdc
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Pin Under Test	Min	Max	Unit	Test Voltage @ T_A = 25°C			Ground
						VT_{in}	V_{DD}	V_S	
						*	-30 ± 1 Vdc	-10 ±0.5 Vdc	
						Applied to pins listed below:			
Drain Supply Drain Current	I_{DD}	11	-	2.5	mAdc	-	11	12	1,4,7,8,13
Source Supply Drain Current	I_{DS}	12	-	17	mAdc	-	1,2,5,9,11	12	4,7,8,13
Source Supply Leakage Current	I_{SS}	12	-	5.0	μAdc	-	-	12	1,2,3,4,5 6,7,8,9,10 11, 13, 14
"Q" Logical "0" Output Voltage	V_{OH}	3 6 10 14	-9.0 -9.0 -9.0 -9.0	- - - -	Vdc	1 4 8 13	11 11 11 11	12 12 12 12	7 7 7 7
"Q" Logical "1" Output Voltage	V_{OL}	3 6 10 14	- - - -	-2.5 -2.5 -2.5 -2.5	Vdc	1 4 8 13	11 11 11 11	12 12 12 12	7 7 7 7
"$\bar{Q}$" Logical "0" Output Voltage	V_{OH}	1 2 5 9	-10 -10 -10 -10	- - - -	Vdc	13 1 4 8	11 11 11 11	12 12 12 12	7 7 7 7
"$\bar{Q}$" Logical "1" Output Voltage	V_{OL}	1 2 5 9	- - - -	-2.5 -2.5 -2.5 -2.5	Vdc	13 1 4 8	11 11 11 11	12 12 12 12	7 7 7 7
Toggle Frequency	f_{Tog}		100	-	kHz		See Test Diagram		

*VT_{in} — Preset to desired output level by applying -20 Vdc to input then open.

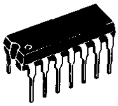
TOGGLE FREQUENCY TEST DIAGRAM AND WAVE FORMS



LINEAR INTEGRATED CIRCUITS

MC1302P
DUAL PREAMPLIFIER

Monolithic dual preamplifier designed for amplifying low level signals in audio applications.

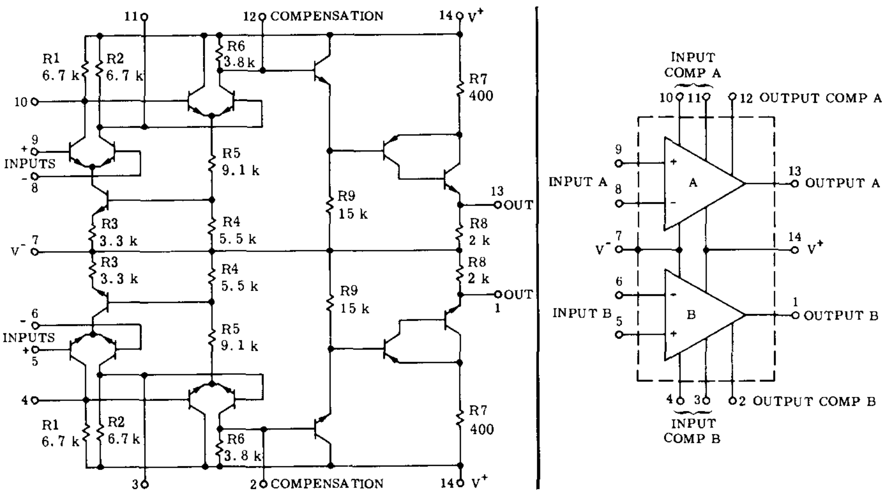


CASE 93

MAXIMUM RATINGS

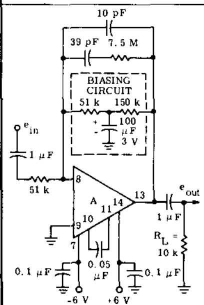
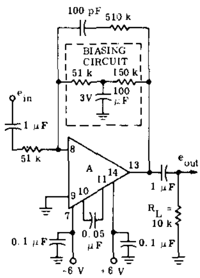
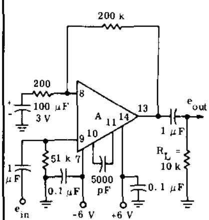
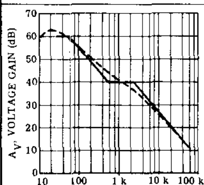
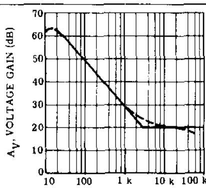
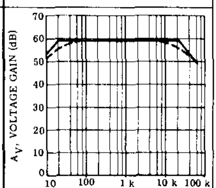
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+8 -8	Vdc Vdc
Differential Input Signal	V_{in}	±2.0	Volts
Output Short Circuit Duration	I_s	continuous	
Power Dissipation (Package Limitation) Derate above T_A = 25°C	P_D	400 3.3	mW mw/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

CIRCUIT SCHEMATIC



MC1302P (continued)

ELECTRICAL CHARACTERISTICS -FOR EACH AMPLIFIER
(V^+ = +6 Vdc, V^- = -6 Vdc, T_A = 25°C unless otherwise noted)

EQUALIZATION CHARACTERISTIC	RIAA	NAB	PREAMP
TEST DIAGRAM			
EQUALIZATION CURVE —— Theoretical Curve - - - Actual Curve			

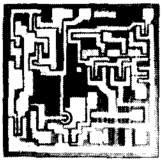
Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
Voltage Gain § f = 1.0 kHz	39	40	41	29	30	31	56	59	61	dB
Output Swing* f = 10 kHz	1.0	1.5	-	1.0	1.1	-	1.0	1.7	-	Vrms
Signal to Noise Ratio e_{out} = 1.0 Vrms	46	48	-	46	52	-	46	52	-	dB
Total Harmonic Distortion f = 1.0 kHz, e_{out} = 1.0 Vrms	-	0.6	0.8	-	0.25	0.3	-	0.6	0.8	%
Channel Separation f = 1.0 kHz	50	63	-	50	72	-	50	64	-	dB
f = 10 kHz	45	54	-	50	65	-	45	54	-	dB

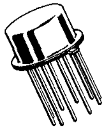
§ Voltage gain depends upon percent tolerance of feedback impedance ratio (components used were ± 5%).

* For linear operation the Output Voltage Swing should be less than 1.1 Vrms.

MC1433

OPERATIONAL AMPLIFIER

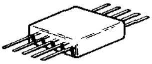




CASE 71
SUFFIX G

Pin 4 connected to case

Monolithic operational amplifier designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.



CASE 72
SUFFIX "F"
(TO-91)

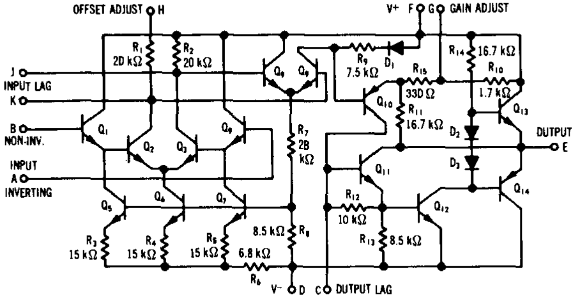
PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H	J	K
"G" Package	1	2	3	4	5	6	7	8	9	10
"F" Package	10	1	2	3	4	5	6	7	8	9

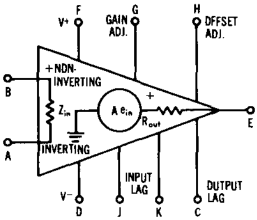
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V+ V-	+18 -18	Vdc Vdc
Differential Input Signal	V_{in}	±10	Volts
Common Mode Input Swing	CMV_{in}	±V+	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	I_S	1.0	s
Power Dissipation (Package Limitation) Metal Can Derate above T_A = 25°C Flat Package Derate above T_A = 25°C	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range*	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

*For full temperature range (-55°C to +125°C) and characteristic curves, see MC1533 data sheet.



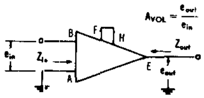
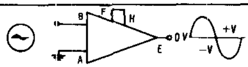
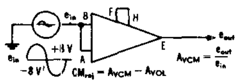
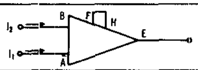
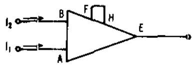
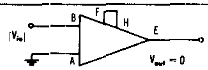
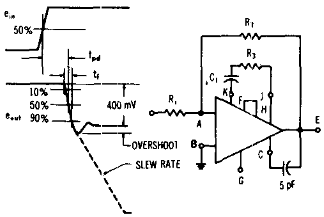
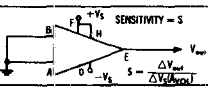
CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT

MC1433 (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = 25°C$ unless otherwise noted)

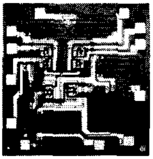
Characteristic Definitions [1]	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain (V @ Pin G = +15 Vdc) (Pin G open) (V @ Pin G = +15 Vdc, T_A = 0°C, +75°C) (Pin G open, T_A = 0°C, +75°C)	A_{VOL}	 30,000 10,000 20,000 5,000	 60,000 30,000 50,000 25,000	 - - - -	-
	Output Impedance (Pin G open, f = 20 Hz)	Z_{out}	-	100	150	Ω
	Input Impedance (Pin G open, f = 20 Hz)	Z_{in}	300	600	-	kΩ
	Output Voltage Swing (R_L = 10 kΩ) (R_L = 2 kΩ)	V_{out}	 ±12 ±10	 ±13 ±12	 - -	V_{peak}
	Input Common Mode Voltage Swing	CMV_{in}	±8	±9	-	V_{peak}
	Common Mode Rejection Ratio (V @ Pin G = +15 Vdc) (Pin G open)	CM_{rej}	 80 70	 100 94	 - -	dB
	Input Bias Current $\left(I_b = \frac{I_1 + I_2}{2}\right)$ (T_A = +25°C) (T_A = 0°C)	I_b	 - -	 0.5 -	 2.0 4.0	µA
	Input Offset Current ($I_{io} = I_1 - I_2$) ($I_{io} = I_1 - I_2$, T_A = 0°C) ($I_{io} = I_1 - I_2$, T_A = +75°C)	I_{io}	 - - -	 0.1 - -	 0.50 0.75 0.75	µA
	Input Offset Voltage [2] (T_A = 25°C) (T_A = 0°C, +75°C)	V_{io}	 - -	 1.0 -	 7.5 10.0	mV
	Step Response Gain = 100, 15% overshoot, R_1 = 1 kΩ, R_2 = 100 kΩ, R_3 = 100 Ω, C_1 = 0.02 µF	 t_f t_{pd} dV_{out}/dt [3]	 - - -	 0.15 0.06 11.0	 - - -	 µs µs V/µs
	Gain = 10, no overshoot, R_1 = 1 kΩ, R_2 = 10 kΩ, R_3 = 10 Ω, C_1 = 0.05 µF	t_f t_{pd} dV_{out}/dt [3]	- - -	0.3 0.1 1.5	- - -	µs µs V/µs
	Gain = 1, 20% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 5 Ω, C_1 = 0.1 µF	t_f t_{pd} dV_{out}/dt [3]	- - -	0.2 0.3 0.8	- - -	µs µs V/µs
	Average Temperature Coefficient of Input Offset Voltage (T_A = 0°C to +25°C) (T_A = +25°C to +75°C)	TC_{Vio}	 - -	 10 8	 - -	µV/°C
	Average Temperature Coefficient of Input Offset Current (T_A = 0°C to +25°C) (T_A = +25°C to +75°C)	TC_{Iio}	 - -	 0.1 0.05	 - -	nA/°C
	DC Power Dissipation (Power Supply = ±15 V, V_{out} = 0)	P_D	-	125	240	mW
	Positive Supply Sensitivity (V^- constant)	S^+	-	50	200	µV/V
	Negative Supply Sensitivity (V^+ constant)	S^-	-	50	200	µV/V

(1) All definitions imply linear operation

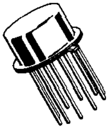
(2) Input offset voltage (V_{io}) may be adjusted to zero by varying the potential on pin H

(3) dV_{out}/dt = Slew Rate

MC1529G
MC1429G
DIFFERENTIAL AMPLIFIERS



NPN MONOLITHIC
ALL DIFFUSED



CASE 71

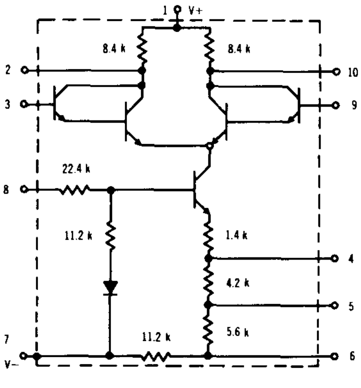
Darlington input differential amplifiers designed for high-gain applications. Features built-in temperature compensated current source for excellent temperature stability.

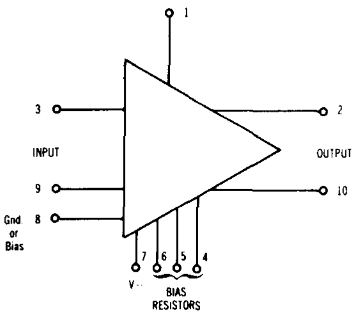
Pin 7 electrically connected to can

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V	+14	Vdc
Power Supply Voltage	V	-14	Vdc
Differential Input Signal	V_{in}	± 5	Vdc
Operating Temperature Range MC1529G MC1429G	T_A	 -55 to 125 0 to 75	°C
Storage Temperature Range	T_{stg}	-65 to 150	°C
Power Dissipation (Package Limitation) Derate above T_A = 25°C)	P_D	680 4.6	mW mW/°C

CIRCUIT SCHEMATICS



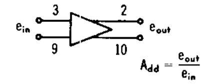
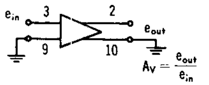
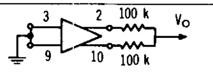
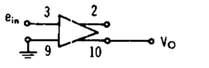
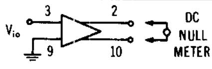
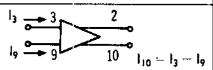
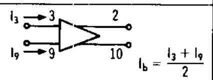
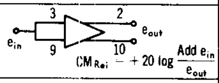
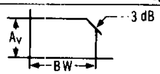
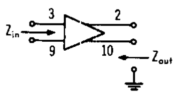


EQUIVALENT CIRCUIT

MC1529G/MC1429G (continued)

ELECTRICAL CHARACTERISTICS (V± = +12 Vdc; V− = −12 Vdc; V_s = 0 Vdc; T_A = 25°C unless otherwise noted)

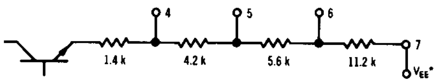
Connect pin 4 to pin 6 and pin 5 to pin 7 for all tests.

Characteristic Definitions*	Characteristic	Symbol	Min	Typ	Max	Unit
	Differential Voltage Gain	A_{dd}				
	MC1529G		50	75	110	V/V
			34	—	41	dB
	MC1429G		45	75	—	V/V
			33	—	—	dB
	Single Ended Voltage Gain	A_V				
	MC1529G		25	—	55	V/V
			28	—	35	dB
	MC1429G		22	—	—	V/V
			27	—	—	dB
	Output Voltage, Common Mode	$V_{o(CM)}$				Vdc
	MC1529G		6.5	7.0	8.5	
	MC1429G		5.5	7.0	8.5	
	Maximum Output Swing Both Types	V_o	5.8	—	—	$V_{(p-p)}$
	Input Offset Voltage	V_{io}				mVdc
	MC1529G		—	—	9.0	
	MC1429G		—	—	12.0	
	Input Offset Current	I_{io}				µAdc
	MC1529G		—	—	2.0	
	MC1429G		—	—	3.0	
	Input Bias Current	I_{in}				µAdc
	MC1529G		—	—	4.0	
	MC1429G		—	—	4.0	
	Common Mode Rejection Both Types	CM_{Rej}	70	—	—	dB
	Bandwidth	BW				kHz
	MC1529G		200	300	—	
	MC1429G		150	250	—	
	Differential Input Impedance	Z_{in}				kΩ
	MC1529G		40	—	—	
	MC1429G		30	—	—	
	Single Ended Output Impedance	Z_{out}				kΩ
	MC1529G		—	—	12	
	MC1429G		—	—	15	

*All definitions imply linear operation.

BIASING ARRANGEMENT

In the emitter of the current source transistor of each of the differential amplifiers, there are four resistors of different values which may be connected in seven ways. The resultant effective resistance in conjunction with a given V_{EE} makes provision for different current levels. For convenience, the seven methods together with their effective resistances are tabulated below.



* Pin 7 is connected to the substrate and must be connected to the V_{EE} supply for proper circuit operation.

METHOD	1	2	3	4	5	6	7
PIN CONNECTIONS	4-7	4-6, 5-7	4-5, 6-7	4-6	4-5	5-6	4,5,6 OPEN
EFFECTIVE RESISTANCE	1.4 k	3.37 k	7.0 k	12.6 k	18.2 k	16.8 k	22.4 k

MC1529G/MC1429G (continued)

EFFECT OF TEMPERATURE ON CHARACTERISTICS

FIGURE 1 — DIFFERENTIAL MODE GAIN

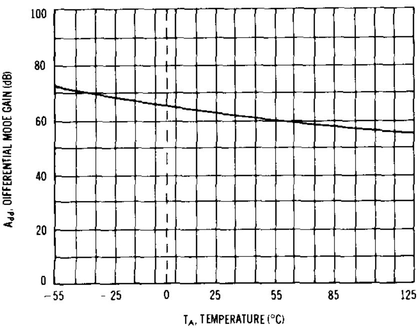


FIGURE 2 — OUTPUT VOLTAGE-COMMON MODE

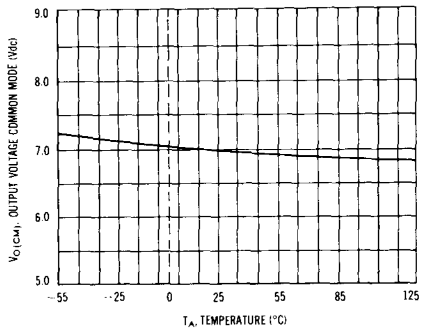


FIGURE 3 — INPUT OFFSET VOLTAGE

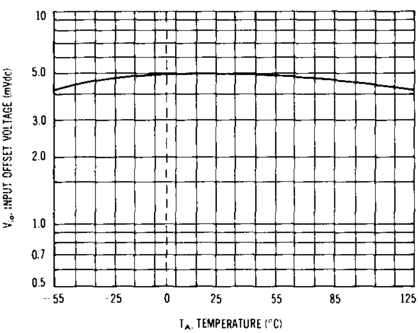


FIGURE 4 — INPUT OFFSET CURRENT

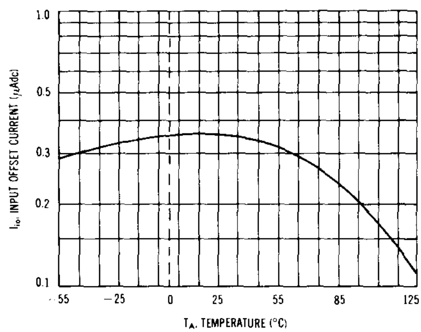


FIGURE 5 — COMMON MODE REJECTION

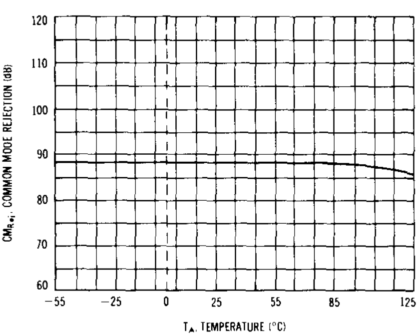
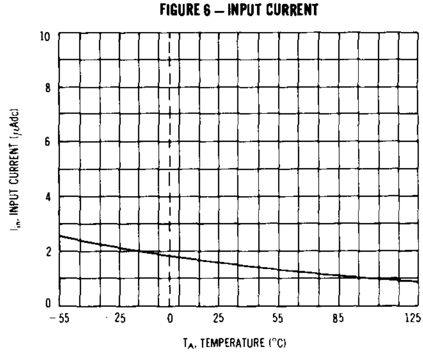
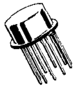


FIGURE 6 — INPUT CURRENT



MC1552G
MC1553G
VIDEO AMPLIFIER



CASE 71

Pin 6 connected to case

Monolithic video amplifier, a three-stage, direct-coupled, common-emitter cascade incorporating series-series feedback to achieve stable voltage gain, low distortion, and wide bandwidth. Employs a temperature-compensated dc feedback loop to stabilize the operating point and a current-biased emitter follower output. Intended for use as either a wide-band linear amplifier or as a fast rise pulse amplifier.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 9	V^+	9	Vdc
Input Voltage, Pin 1 to Pin 2 (R_S = 500 ohms)	V_{in}	1.0	V(RMS)
Power Dissipation (Package Limitation) Derate above 25°C	P_D	680 4.6	mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATICS

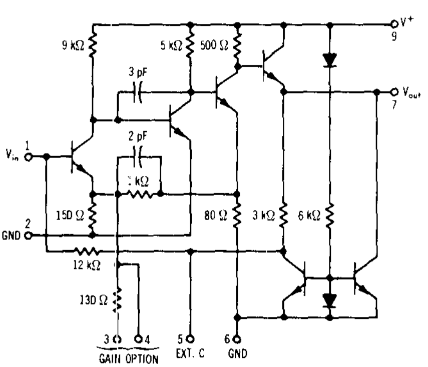


FIGURE 1 – MC1552 (LOW GAIN)

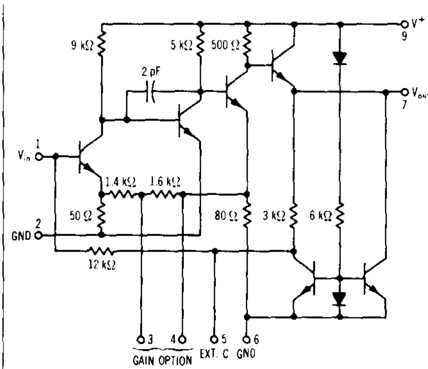


FIGURE 2 – MC1553 (HIGH GAIN)

MC1552G, MC1553G (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +6$ Vdc, $T_A = 25°C$ unless otherwise noted)

Characteristic		Fig. No.	Gain Option*	Symbol	Min	Typ	Max	Unit
Voltage Gain	MC1552	3	50 100	V_{out}/V_{in}	44 87	50 100	56 113	—
	MC1553		200 400		175 350	200 400	225 450	
Voltage Gain Variation (T_A = -55°C to +125°C)		3	All	—	—	±0.2	—	dB
Bandwidth	MC1552	3, 6	50 100	BW	21 17	40 35	— —	MHz
	MC1553		200 400		17 7.5	35 15	— —	
Input Impedance (f = 100 kHz, R_L = 1 kΩ)		—	All	$\|Z_{in}\|$	7	10	—	kΩ
Output Impedance (f = 100 kHz, R_S = 50 Ω)		—	All	$\|Z_{out}\|$	—	16	50	Ω
DC Output Voltage		3	All	V_{out} (dc)	2.5	2.8	3.2	Vdc
DC Output Voltage Variation (T_A = -55°C to +125°C)		3	All	ΔV_{out} (dc)	—	±0.05	—	Vdc
Output Voltage Swing ($Z_L \geq$ 1 kΩ, V_{in} = 100 mV rms)		3	All	V_{out}	3.6	4.2	—	Vp-p
Power Dissipation		—	All	P_D	—	75	120	mW
Delay Time	MC1552	3, 4	50 100	t_d	— —	6 9	— —	ns
	MC1553		200 400		— —	10 25	— —	
Rise Time	MC1552	3, 4	50 100	t_r	— —	9 12	16 20	ns
	MC1553		200 400		— —	11 30	20 45	
Overshoot		3, 4	All	$(V_{os}/V_p)100$	—	5	—	%
Noise Figure (R_S = 400 Ω, f_o = 30 MHz, BW = 3 MHz)		—	All	NF	—	5	—	dB
Total Harmonic Distortion (V_{out} = 2 Vp-p, f = 200 kHz, R_L = 1 kΩ)		—	All	—	—	0.2	—	%

*To obtain the voltage-gain characteristic desired, use the following pin connections:

Type	Voltage Gain	Pin Connections
MC1552	50	Pin 3 Open
	100	Ground Pin 3
MC1553	200	Connect Pin 3 to Pin 4
	400	Pins 3 and 4 Open

NOTES

1. Ground Pin 6 as close to can as possible to minimize overshoot. Best results by directly grounding can.

2. If large input and output coupling capacitors are used, place shield between them to avoid input-output coupling.

3. A high-frequency capacitor must always be used to bypass the power supply. This capacitor should be as close to the circuit as possible.

4. Voltage gain can be adjusted to any value between 50 and 3000 by connecting an external resistor from Pin 4 to ground on MC1552, or from Pin 3 to ground on MC1553, as shown in Figure 8. Under these conditions, the following equations must be used to determine C_1 and C_2 rather than the circuits shown in Figure 5.

Fig. 5b $C_1 = \frac{1}{2\pi f_c(1.7 \times 10^4)}$ Farads; $C_2 = 8\,C_1(V_{out}/V_{in})$ Farads

Fig. 5c $C_1 = \frac{V_{out}/V_{in}}{2\pi f_c(1.5 \times 10^4)}$ Farads

Fig. 5d $C_2 = \frac{V_{out}/V_{in}}{2\pi f_c(3 \times 10^3)}$ Farads

FIGURE 3 — TEST CIRCUIT

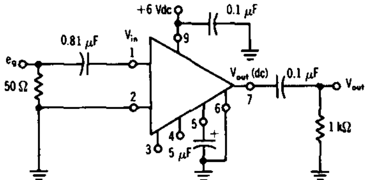
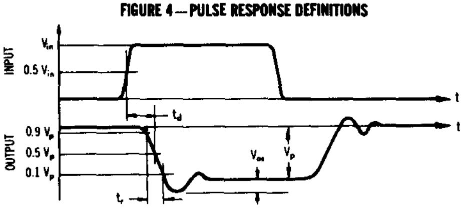


FIGURE 4 — PULSE RESPONSE DEFINITIONS



MC1552G, MC1553G (continued)

TYPICAL CHARACTERISTICS

$T_A = 25°C$

FIGURE 5a – FREQUENCY RESPONSE

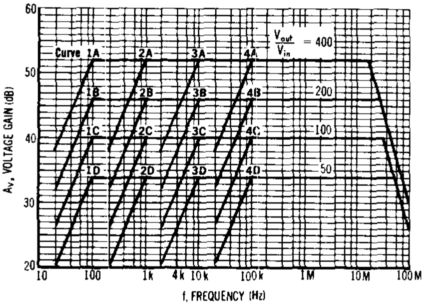
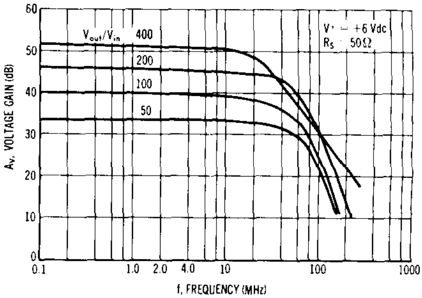
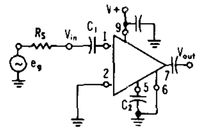


FIGURE 6 – VOLTAGE GAIN versus FREQUENCY



TEST CIRCUITS FOR FREQUENCY RESPONSE

FIGURE 5b – CAPACITIVE COUPLED INPUT (R_s < 5kΩ)



Curve No.	C_1 (μF)	C_2 (μF)
1A	0.1	250
1B	0.1	150
1C	0.1	70
1D	0.1	40

Curve No.	C_1 (μF)	C_2 (μF)
2A	0.01	30
2B	0.01	18
2C	0.01	8.0
2D	0.01	4.0
	(pF)	
3A	1000	3.0
3B	1000	1.8
3C	1000	0.8
3D	1000	0.4
4A	100	0.3
4B	100	0.18
4C	100	0.08
4D	100	0.04

FIGURE 7 – MAXIMUM NEGATIVE SWING SLEW RATE versus LOAD CAPACITANCE

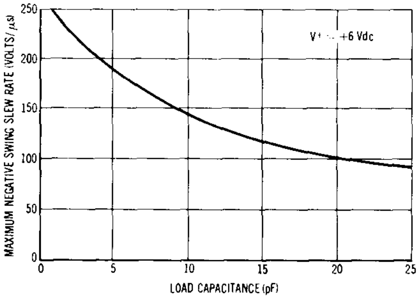
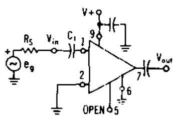


FIGURE 5c – CAPACITIVE COUPLED INPUT (R_s < 500Ω)



Curve No.	C_1 (μF)	Curve No.	C_1 (μF)
1A	20	3A	0.4
1B	10	3B	0.2
1C	7.0	3C	0.1
1D	3.0	3D	0.06
2A	3.0	4A	0.04
2B	1.0	4B	0.02
2C	0.8	4C	0.01
2D	0.5	4D	0.007

FIGURE 8 – VOLTAGE GAIN ADJUSTMENT BY USE OF EXTERNAL RESISTOR

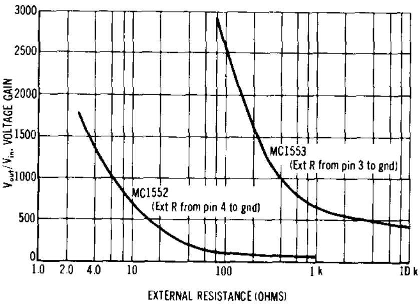
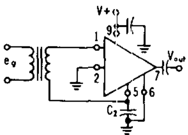


FIGURE 5d – TRANSFORMER COUPLED INPUT



Curve No.	C_2 (μF)	Curve No.	C_2 (μF)
1A	200	3A	2.0
1B	100	3B	1.0
1C	70	3C	0.7
1D	30	3D	0.3
2A	20	4A	0.2
2B	10	4B	0.1
2C	7.0	4C	0.07
2D	3.0	4D	0.03

MC1552G, MC1553G (continued)

INPUT ADMITTANCE

$V^+ = 6$ Vdc, $R_L = 1$ kΩ, $T_A = 25°C$

FIGURE 9 — GAIN = 50

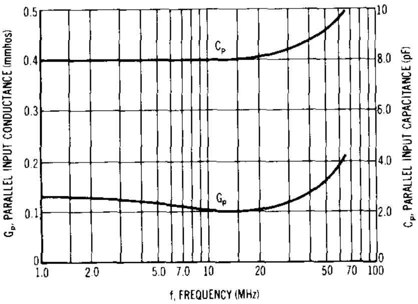


FIGURE 10 — GAIN = 100

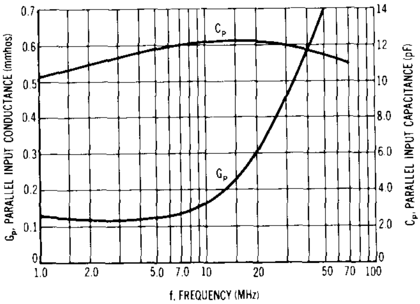


FIGURE 11 — GAIN = 200

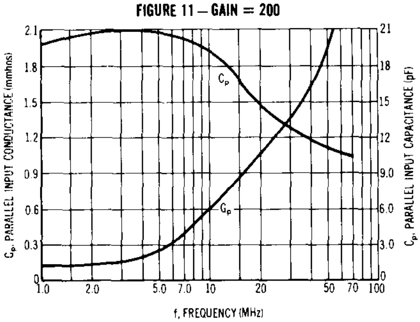


FIGURE 12 — GAIN = 400

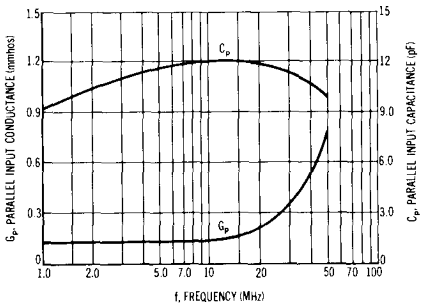


FIGURE 13 — OUTPUT IMPEDANCE versus FREQUENCY

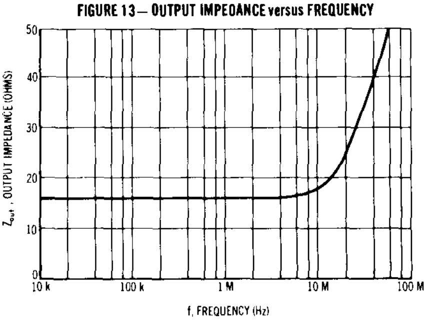
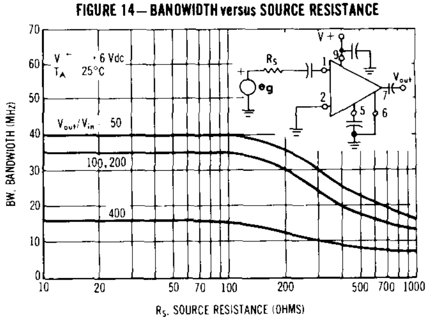
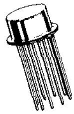


FIGURE 14 — BANDWIDTH versus SOURCE RESISTANCE



MC1554G

1-WATT POWER AMPLIFIER



CASE 71

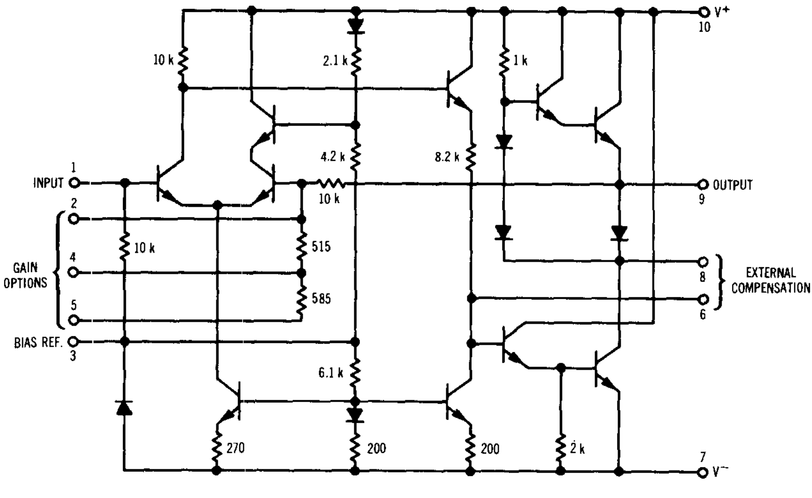
Pin 7 Electrically Connected to Can

Monolithic 1-watt power amplifier designed to amplify signals to 300 kHz with one watt delivered to a direct or capacitively coupled load.

MAXIMUM RATINGS (Tc = 25°C unless otherwise noted)

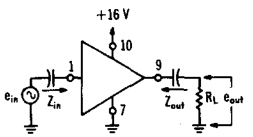
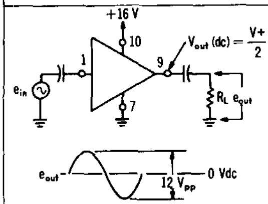
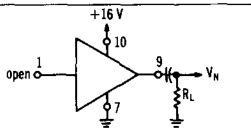
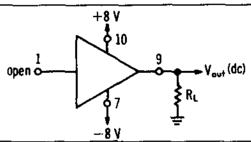
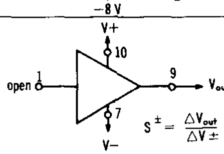
Rating	Symbol	Value	Unit
Total Power Supply Voltage	$\lvert V^+ \rvert + \lvert V^- \rvert$	18	Vdc
Peak Load Current	I_{out}	0.5	Amp
Audio Output Power	P_{out}	1.8	Watt
Power Dissipation (package limitation)	P_D		
$T_A = 25°C$		600	mW
Derate above 25°C		4.8	mW/°C
$T_C = 25°C$		1.8	Watts
Derate above 25°C		14.4	mW/°C
Operating Temperature Range	T_C	-55 to +125	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

CIRCUIT SCHEMATIC



MC1554G (continued)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)
Frequency compensation shown in Figures 2 and 3.

Characteristic Definitions	Characteristic	R_1 (ohms)	Gain Option*	Symbol	Min	Typ	Max	Unit
	Output Power	16	-	P_{out}	1.0	1.1	-	Watt
	Power Dissipation (@ P_{out} = 1.0 W)	16	-	P_D	-	0.9	1.2	Watt
	Voltage Gain	16	10	A_V	6.0	10	12	V/V
		16	18		-	16	-	
		16	38		-	36	-	
	Input Impedance	-	10	Z_{in}	7.0	10	-	kΩ
	Output Impedance	-	10	Z_{out}	-	0.2	-	Ω
	Power Bandwidth (for e_{out} < 5% THD)	16	10		-	270	-	kHz
		16	16		-	250	-	
		16	36		-	210	-	
	Total Harmonic Distortion (for e_{tn} < 0.05% THD, f = 20 Hz to 20 kHz)			THD				%
	P_{out} = 1.0 Watt (sinewave)	16	10		-	0.4	-	
	P_{out} = 0.1 Watt (sinewave)	16	10		-	0.5	-	
	Zero Signal Current Drain	∞	-	I_D	-	11	15	mAdc
	Output Noise Voltage	16	10	V_N	-	0.3	-	mV RMS
	Output Quiescent Voltage (Split Supply Operation)	16	-	V_{out}(dc)	-	±3.0	±10.0	mVdc
	Positive Supply Sensitivity (V^- constant)	∞	-	S^+	-	-40	-	mV/V
	Negative Supply Sensitivity (V^+ constant)	∞	-	S^-	-	-40	-	mV/V

* To obtain the voltage gain characteristic desired, use the following pin connections:

Voltage Gain	Pin Connection
10	Pins 2 and 4 open, Pin 5 to ac ground
18	Pins 2 and 5 open, Pin 4 to ac ground
36	Pin 2 connected to Pin 5, Pin 4 to ac ground

TYPICAL CONNECTIONS

FIGURE 2 — SPLIT SUPPLY OPERATION
VOLTAGE GAIN (A_V) = 10, $f_{LOW} \approx$ 25 Hz

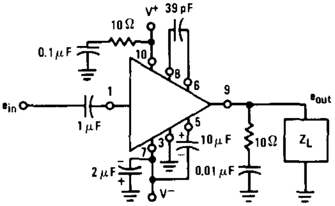
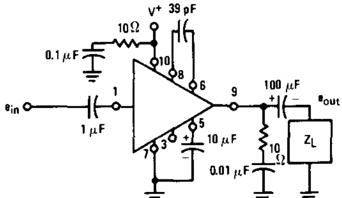


FIGURE 3 — SINGLE SUPPLY OPERATION
VOLTAGE GAIN (A_V) = 10, $f_{LOW} \approx$ 100 Hz



MC1554G (continued)

RECOMMENDED OPERATING CONDITIONS

In order to avoid local VHF instability, the following set of rules must be adhered to:

1. An R-C stabilizing network (0.1 μF in series with 10 ohms) should be placed directly from pin 9 to ground, as shown in Figures 2 and 3, using short leads, to eliminate local VHF instability caused by lead inductance to the load.
2. Excessive lead inductance from the V+ supply to pin 10 can cause high frequency instability. To prevent this, the V+ by-pass capacitor should be connected with short leads from the V+ pin to ground. If this capacitor is remotely located a series R-C network (0.1 μF and 10 ohms) should be used directly from pin 10 to ground as shown in Figures 2 and 3.
3. Lead lengths from the external components to pins 7, 9, and 10 of the package should be as short as possible to insure good VHF grounding for these points.

Due to the large bandwidth of the amplifier, coupling must be avoided between the output and input leads. This can be assured by either (a) use of short leads which are well isolated, (b) narrow-banding the overall amplifier by placing a capacitor from pin 1 to ground to form a low-pass filter in combination with the source impedance, or (c) use of a shielded input cable. In applications which require upper band-edge control the input low-pass filter is recommended.

TYPICAL CHARACTERISTICS

FIGURE 4 — MAXIMUM AVAILABLE OUTPUT POWER (SINE WAVE)

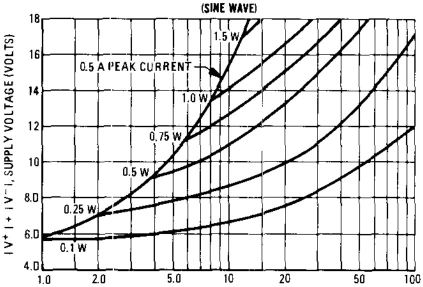


FIGURE 5 — MAXIMUM DEVICE DISSIPATION (SINE WAVE)

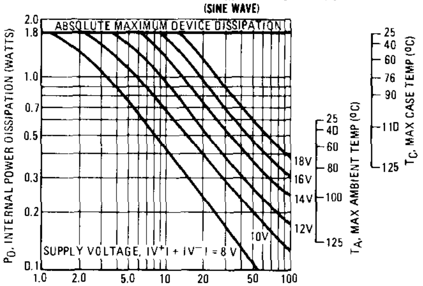


FIGURE 6 — TOTAL HARMONIC DISTORTION versus LOAD RESISTANCE

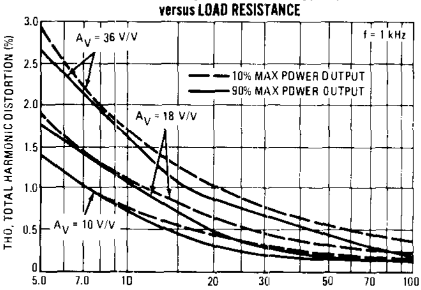
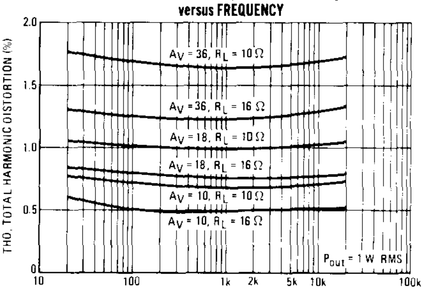


FIGURE 7 — TOTAL HARMONIC DISTORTION versus FREQUENCY



MC1554G (continued)

TYPICAL CHARACTERISTICS

FIGURE 8 — VOLTAGE GAIN versus TEMPERATURE

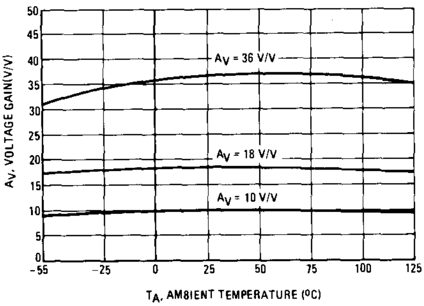


FIGURE 9 — OUTPUT VOLTAGE CHANGE

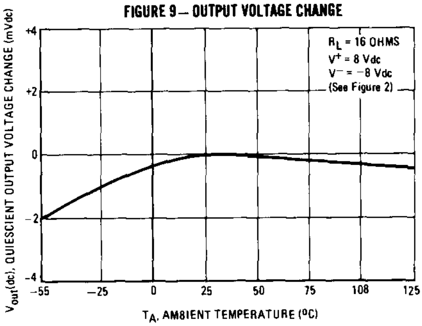


FIGURE 10 — VOLTAGE GAIN versus FREQUENCY (R_L = 16 OHMS)

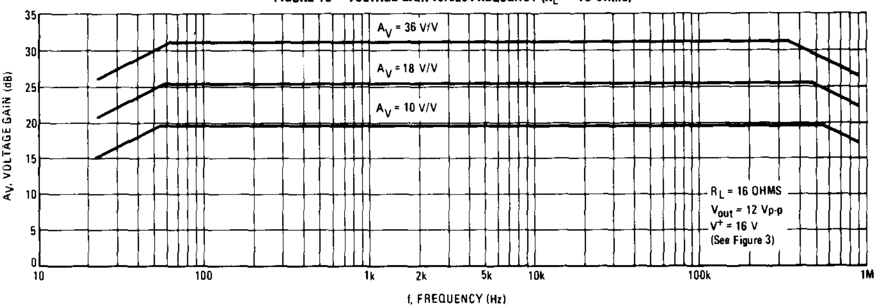
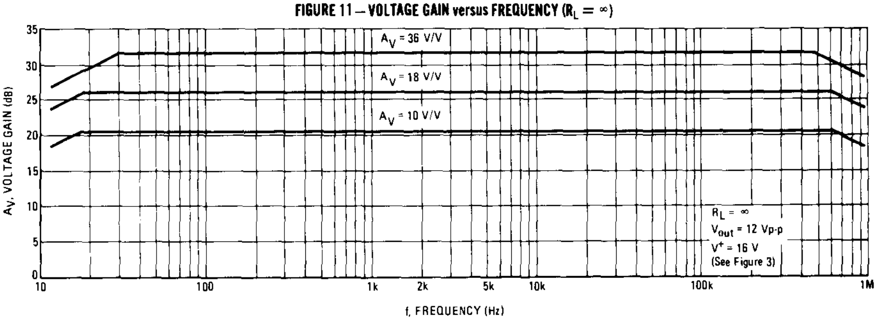
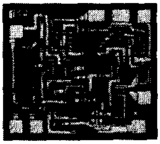
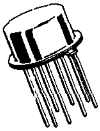


FIGURE 11 — VOLTAGE GAIN versus FREQUENCY ($R_L = \infty$)



MC1709
OPERATIONAL AMPLIFIER

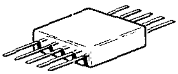




CASE 96
SUFFIX G
TO-99

Lead 4 connected to case

Monolithic operational amplifier designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.



CASE 72
SUFFIX F
(TO-91)

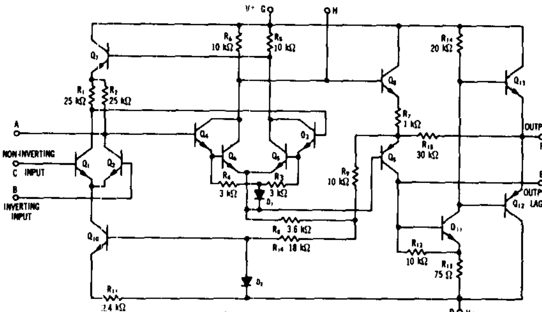
PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H
"G" Package	1	2	3	4	5	6	7	8
"F" Package	2	3	4	5	6	7	8	9

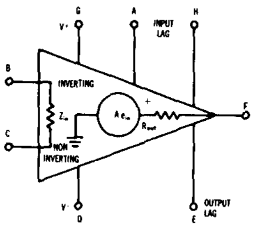
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation) Metal Can Derate above T_A = 25°C Flat Package Derate above T_A = 25°C	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-85 to +150	°C

CIRCUIT SCHEMATICS



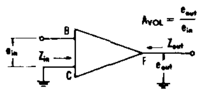
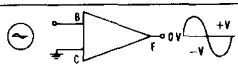
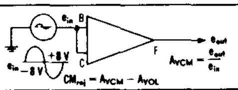
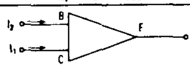
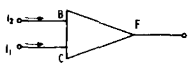
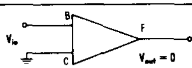
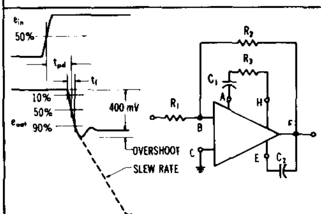
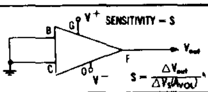
CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT

MC1709 (continued)

ELECTRICAL CHARACTERISTICS (V+ = +15 Vdc, V− = −15 Vdc, T_A = 25°C unless otherwise noted)

Characteristic Definitions ①	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain (V_{out} = ± 10 V, T_A = -55°C to +125°C)	A_{VOL}	25,000	45,000	70,000	-
	Output Impedance (f = 20 Hz)	Z_{out}	-	150	-	Ω
	Input Impedance (f = 20 Hz)	Z_{in}	150	400	-	kΩ
	Output Voltage Swing (R_L = 10 kΩ) (R_L = 2 kΩ)	V_{out}	±12 ±10	±14 ±13	- -	V_{peak}
	Input Common Mode Voltage Swing	CMV_{in}	±8	±10	-	V_{peak}
	Common Mode Rejection Ratio	CM_{rej}	70	90	-	dB
	Input Bias Current $\left(I_b = \frac{I_1 + I_2}{2}\right)$ (T_A = +25°C) (T_A = -55°C)	I_b	- -	0.2 0.5	0.5 1.5	µA
	Input Offset Current ($I_{io} = I_1 - I_2$) ($I_{io} = I_1 - I_2$, T_A = -55°C) ($I_{io} = I_1 - I_2$, T_A = +125°C)	I_{io}	- - -	0.05 - -	0.2 0.5 0.2	µA
	Input Offset Voltage (T_A = 25°C) (T_A = -55°C + 125°C)	V_{io}	- -	1.0 -	5.0 6.0	mV
	Step Response {Gain = 100, 5% overshoot, R_1 = 1 kΩ, R_2 = 100 kΩ, R_3 = 1.5 kΩ, C_1 = 100 pF, C_2 = 3 pF}	t_f t_{pd} dV_{out}/dt ②	- - -	0.8 0.38 12.0	- - -	µs µs V/µs
	{Gain = 10, 10% overshoot, R_1 = 1 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 500 pF, C_2 = 20 pF}	t_f t_{pd} dV_{out}/dt ②	- - -	0.8 0.34 1.7	- - -	µs µs V/µs
	{Gain = 1, 5% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 5000 pF, C_2 = 200 pF}	t_f t_{pd} dV_{out}/dt ②	- - -	2.2 1.3 0.25	- - -	µs µs V/µs
	Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = -55°C to +125°C) (R_S ≤ 10 kΩ, T_A = -55°C to +125°C)	TC_{Vio}	- -	3.0 6.0	- -	µV/°C
	DC Power Dissipation (Power Supply = ±15 V, V_{out} = 0)	P_D	-	80	165	mW
	Positive Supply Sensitivity (V^- constant)	S^+	-	25	150	µV/V
	Negative Supply Sensitivity (V^+ constant)	S^-	-	25	150	µV/V

① All definitions imply linear operation

② dV_{out}/dt = Slew Rate

MC1709 (continued)

TYPICAL OUTPUT CHARACTERISTICS

FIGURE 1 – TEST CIRCUIT
$V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = 25°C$

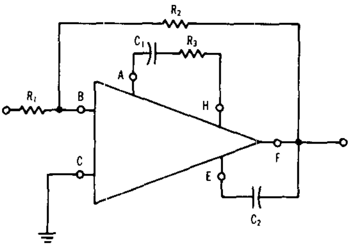


Fig. No.	Curve No.	Test Conditions				
		R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	C_1 (pF)	C_2 (pF)
2	1	10 k	10 k	1.5 k	5 k	200
	2	10 k	100 k	1.5 k	500	20
	3	10 k	1M	1.5 k	100	3
	4	1 k	1M	0	10	3
3	1	1 k	1M	0	10	3
	2	10 k	1M	1.5 k	100	3
	3	10 k	100 k	1.5 k	500	20
	4	10 k	10 k	1.5 k	5 k	200
4	1	0	∞	1.5 k	5 k	200
	2	0	∞	1.5 k	500	20
	3	0	∞	1.5 k	100	3
	4	0	∞	0	10	3

FIGURE 2 – LARGE SIGNAL SWING versus FREQUENCY

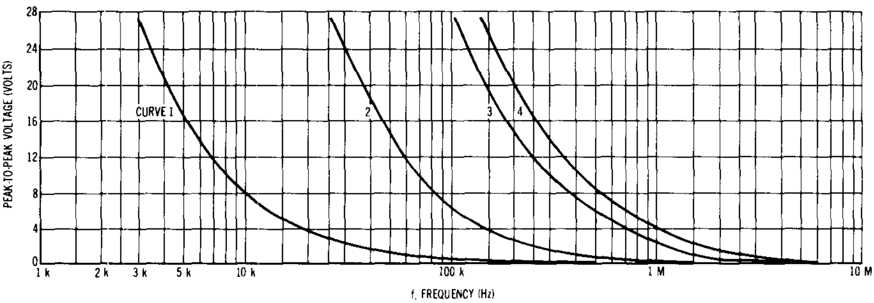


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

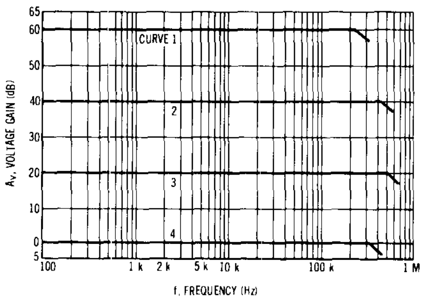
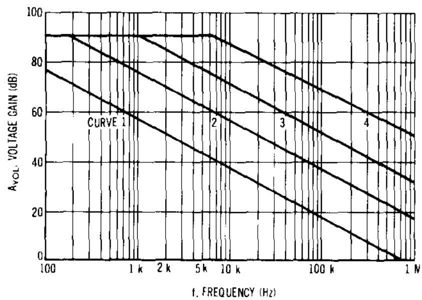


FIGURE 4 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY



MC1709 (continued)

FIGURE 5 — POWER DISSIPATION versus POWER SUPPLY VOLTAGE

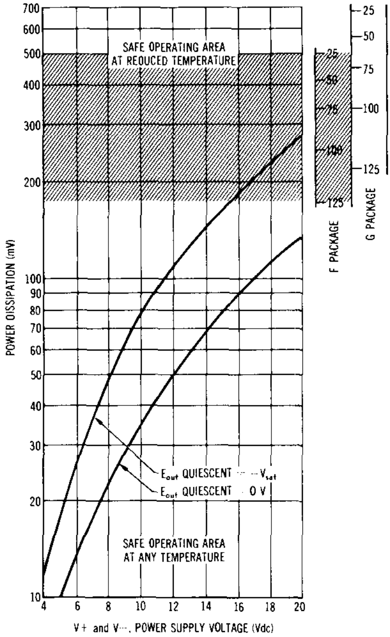


FIGURE 6 — VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

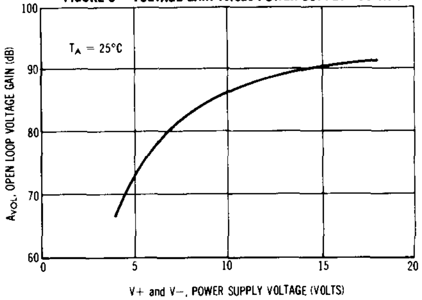


FIGURE 7 — COMMON SWING versus POWER SUPPLY VOLTAGE

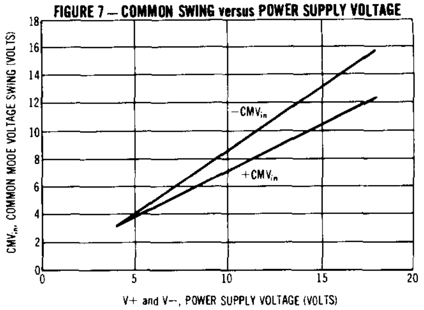


FIGURE 8 — INPUT OFFSET VOLTAGE versus TEMPERATURE

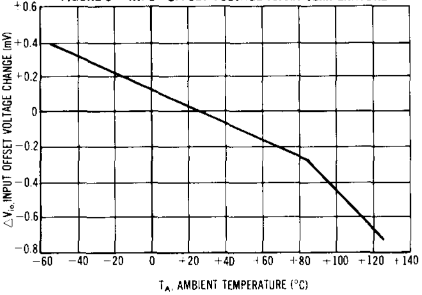
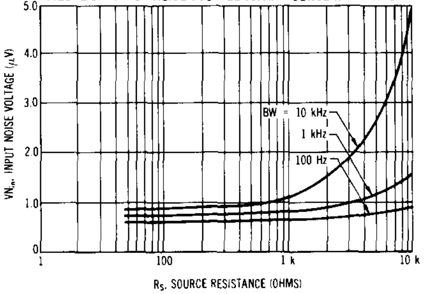
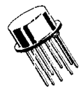


FIGURE 9 — INPUT NOISE VOLTAGE versus SOURCE RESISTANCE

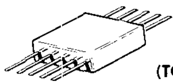


MC1709C



(TO-99)
CASE 71
SUFFIX "G"

Lead 4 connected to case



(TO-91)
CASE 72
SUFFIX "F"

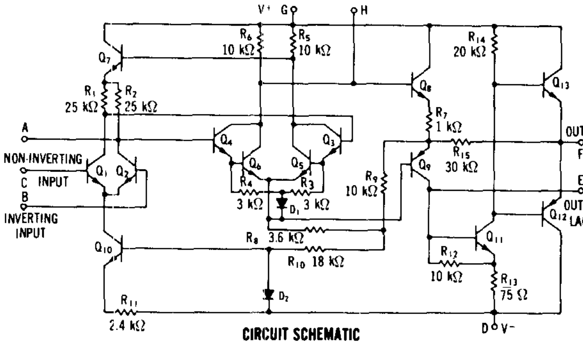
Monolithic operational amplifier designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

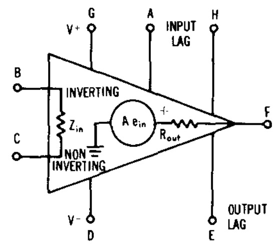
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	I_S	5.0	s
Power Dissipation (Package Limitation) Metal Can Derate above T_A = 25°C Flat Package Derate above T_A = 25°C	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range*	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

*For full temperature range (-55°C to +125°C) and characteristic curves, see MC1709 data sheet.

CIRCUIT SCHEMATICS



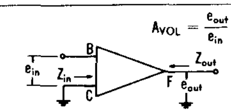
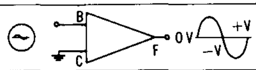
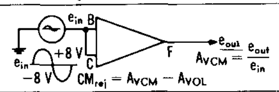
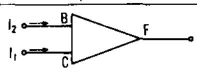
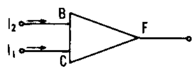
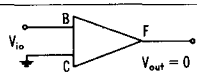
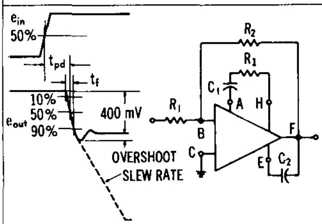
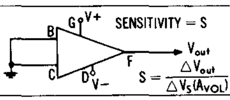
CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT

MC1709C (continued)

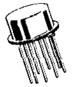
ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = 25°C$ unless otherwise noted)

Characteristic Definitions (linear operation)	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain (R_L=2 kΩ, V_{out} = ± 10 V, T_A = 0°C to +75°C)	A_{VOL}	15,000	45,000	-	-
	Output Impedance (f = 20 Hz)	Z_{out}	-	150	-	Ω
	Input Impedance (f = 20 Hz)	Z_{in}	50	250	-	kΩ
	Output Voltage Swing (R_L = 10 kΩ) (R_L = 2 kΩ)	V_{out}	 ±12 ±10	 ±14 ±13	 - -	V_{peak}
	Input Common Mode Voltage Swing	CMV_{in}	±8.0	±10	-	V_{peak}
	Common Mode Rejection Ratio	CM_{rej}	65	90	-	dB
	Input Bias Current $\left(I_b = \frac{I_1 + I_2}{2}\right)$, ($T_A$ = +25°C) (T_A = 0°C)	I_b	 - -	 0.3 -	 1.5 2.0	µA
	Input Offset Current ($I_{io} = I_1 - I_2$) ($I_{io} = I_1 - I_2$, T_A = 0°C) ($I_{io} = I_1 - I_2$, T_A = +75°C)	I_{io}	 - - -	 0.1 - -	 0.5 0.75 0.75	µA
	Input Offset Voltage (T_A = 25°C) (T_A = 0°C, +75°C)	V_{io}	 - -	 2.0 -	 7.5 10	mV
	Step Response Gain = 100, 5% overshoot, R_1 = 1 kΩ, R_2 = 100 kΩ, R_3 = 1.5 kΩ, C_1 = 100 pF, C_2 = 3 pF	 t_f t_{pd} dV_{out}/dt (1)	 - - -	 0.8 0.38 12	 - - -	 µs µs V/µs
	Gain = 10, 10% overshoot, R_1 = 1 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 500 pF, C_2 = 20 pF	t_f t_{pd} dV_{out}/dt (1)	- - -	0.6 0.34 1.7	- - -	µs µs V/µs
	Gain = 1, 5% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 5000 pF, C_2 = 200 pF	t_f t_{pd} dV_{out}/dt (1)	- - -	2.2 1.3 0.25	- - -	µs µs V/µs
	Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = 0°C to +75°C) ($R_S \le$ 10 kΩ, T_A = 0°C to +75°C)	TC_{Vio}	 - -	 3.0 6.0	 - -	µV/°C
	DC Power Dissipation (Power Supply = ±15 V, V_{out} = 0)	P_D	-	80	200	mW
	Positive Supply Sensitivity (V^- constant)	S^+	-	25	200	µV/V
	Negative Supply Sensitivity (V^+ constant)	S^-	-	25	200	µV/V

(1) dV_{out}/dt = Slew Rate

MC1710

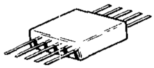
DIFFERENTIAL VOLTAGE COMPARATOR



CASE 96
(TO-99)
SUFFIX G

Lead 4 connected to case

Monolithic differential voltage comparator designed for use in level detection, low-level sensing, and memory applications.



CASE 72
(TO-91)
SUFFIX F

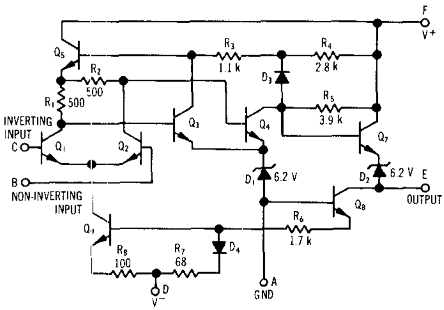
PIN CONNECTIONS

Schematic	A	B	C	D	E	F
"G" Package	1	2	3	4	7	8
"F" Package	1	2	3	5	6	8

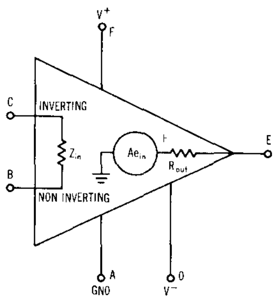
MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+ 14 - 7.0	Vdc Vdc
Differential Input Signal	V_{in}	± 5.0	Volts
Common Mode Input Swing	CMV_{in}	± 7.0	Volts
Peak Load Current	I_L	10	mA
Power Dissipation (package limitation) Metal Can Derate above $T_A = 25°C$ Flat Package Derate above $T_A = 25°C$	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATICS



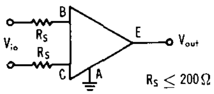
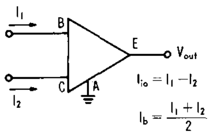
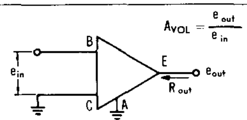
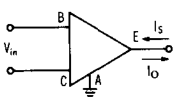
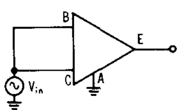
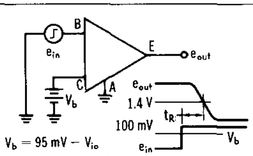
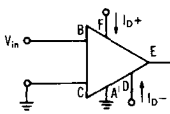
CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT

MC1710 (continued)

ELECTRICAL CHARACTERISTICS ($V^+ = +12$ Vdc, $V^- = -6$ Vdc, $T_A = 25°C$ unless otherwise noted)

Characteristic Definitions	Characteristic	Symbol	Min	Typ	Max	Unit
	Input Offset Voltage	V_{io}				mVdc
	$V_{out} = 1.4$ Vdc, $T_A = 25°C$		-	2.0	5.0	
	$V_{out} = 1.8$ Vdc, $T_A = -55°C$		-	-	6.0	
	$V_{out} = 1.0$ Vdc, $T_A = +125°C$		-	-	6.0	
	Temperature Coefficient of Input Offset Voltage	TC_{Vio}	-	5.0	-	µV/°C
	Input Offset Current	I_{io}				µAdc
	$V_{out} = 1.4$ Vdc, $T_A = 25°C$		-	1.0	10	
	$V_{out} = 1.8$ Vdc, $T_A = -55°C$		-	-	20	
	$V_{out} = 1.0$ Vdc, $T_A = +125°C$		-	-	20	
	Input Bias Current	I_b				µAdc
	$V_{out} = 1.4$ Vdc, $T_A = 25°C$		-	12	75	
	$V_{out} = 1.6$ Vdc, $T_A = -55°C$		-	-	150	
	$V_{out} = 1.0$ Vdc, $T_A = +125°C$		-	-	150	
	Voltage Gain	A_{VOL}				V/V
	$T_A = 25°C$		750	1700	-	
	$T_A = -55$ to $+125°C$		500	-	-	
	Output Resistance	R_{out}	-	200	-	ohms
	Differential Voltage Range	V_{in}	±5.0	-	-	Vdc
	Positive Output Voltage $V_{in} \geq 15$ mVdc, $0 \leq I_o \leq 0.5$ mA	V_{OH}	2.5	3.2	4.0	Vdc
	Negative Output Voltage $V_{in} \geq -15$ mVdc	V_{OL}	-1.0	-0.5	0	Vdc
	Output Sink Current $V_{in} \geq -15$ mV, $V_{out} \geq 0$	I_s	1.6	2.5	-	mAdc
	Input Common Mode Range $V^- = -7$ Vdc	CMV_{in}	±5.0	-	-	Volts
	Response Time For Positive and Negative Going Input Pulse	t_R	-	40	-	ns
	Power Supply Current $V_{out} \leq 0$ Vdc	I_D+	-	6.4	-	mAdc
		I_D-	-	5.5	-	
	Power Consumption					mW
	TO-99 Metal Can		-	115	175	
	TO-91 Flat Package		-	115	150	

MC1710 (continued)

TYPICAL CHARACTERISTICS

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

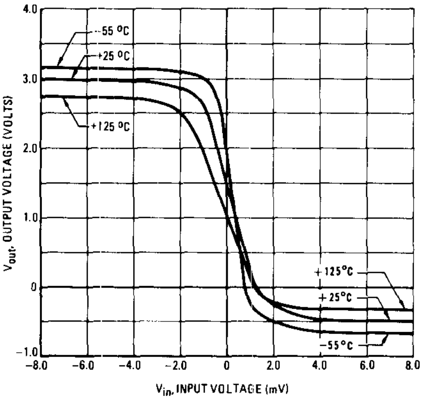


FIGURE 2 – INPUT OFFSET VOLTAGE versus TEMPERATURE

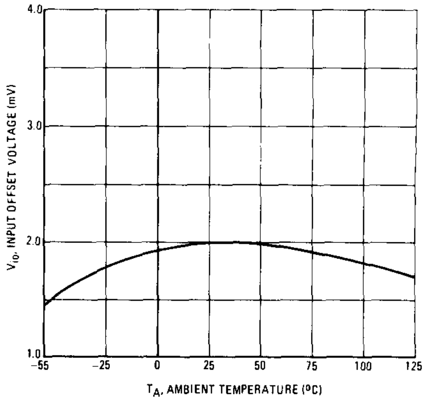


FIGURE 3 – INPUT OFFSET CURRENT versus TEMPERATURE

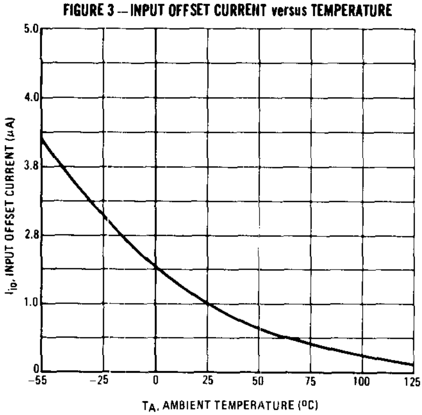
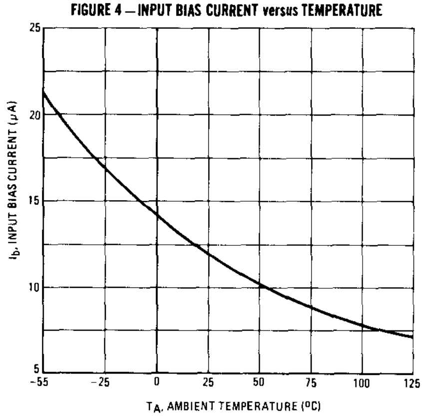


FIGURE 4 – INPUT BIAS CURRENT versus TEMPERATURE



MC1710 (continued)

TYPICAL CHARACTERISTICS

FIGURE 5 — GAIN VARIATION WITH POWER SUPPLY VOLTAGE

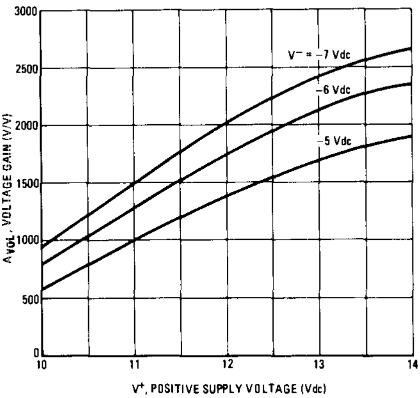


FIGURE 6 — VOLTAGE GAIN versus TEMPERATURE

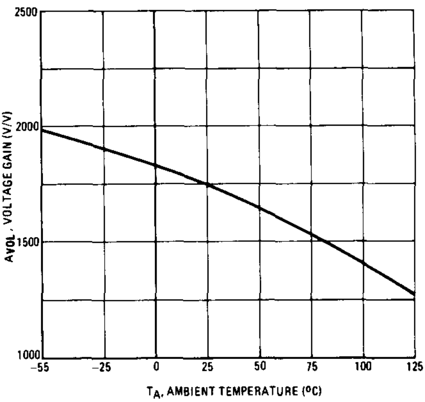


FIGURE 7 — RESPONSE TIME

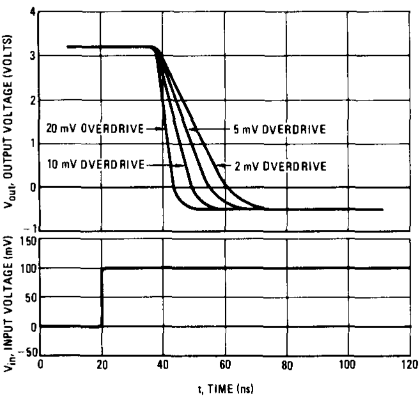
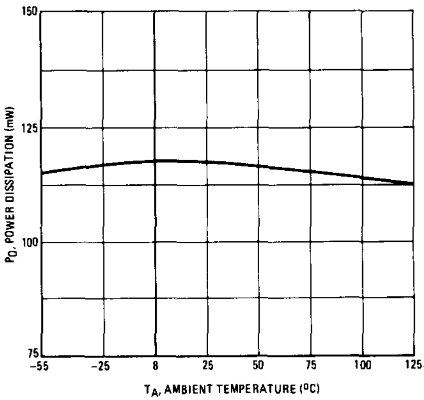


FIGURE 8 — POWER DISSIPATION versus TEMPERATURE



[redacted]

HARDWARE

MK30
MK35

MK-30
MK-35

POWER TRANSISTOR MOUNTING KITS

Mounting kits, types MK-30 and MK-35, provide the necessary hardware to properly mount the TO-36 case (standard industry-type power transistors) to the chassis. With these kits, power transistors can be electrically insulated from the heat sink chassis, while maintaining complete heat transfer characteristics

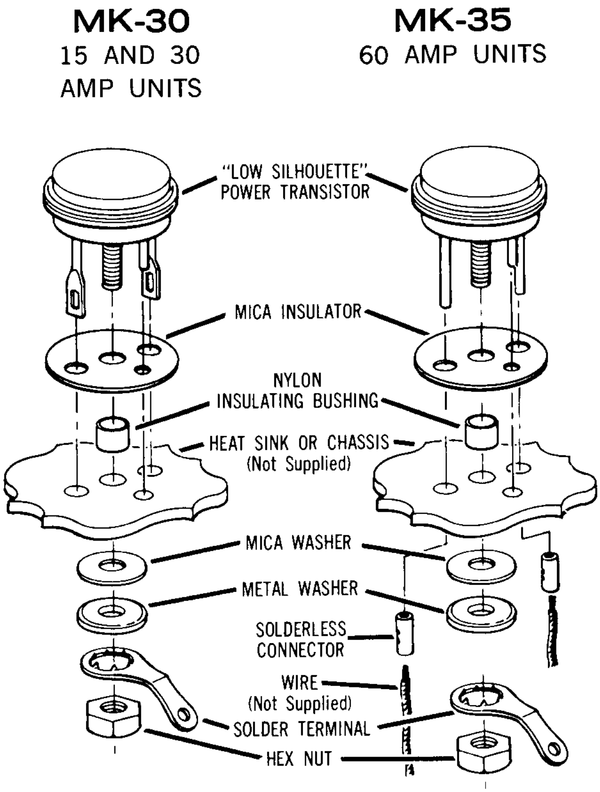
MK-30 Designed for use in applications requiring 30 Amps or less with solder connection to the transistor leads.

MK-35 Designed for use in applications requiring greater than 30 Amps with solderless connection to the transistor leads.

To obtain maximum contact area between case and heat sink for better heat transfer, it is recommended that the transistor first be mounted on the heat sink or chassis. Then, for maximum wire-to transistor lead strength and high-current capacity, the solderless connectors provided are crimped to the transistor leads and heavy wire. The wires may be soldered directly to the leads if strength and high currents (approximately 50 Amps) are not the primary considerations. (Solderless connector tools are available from the Thomas and Betts Co., Elizabeth, N. J. Possible wire types: AWG #12 regular strand (65 x 30) or #10 solid-tinned copper wire.)

These new mounting kits are individually packaged in a convenient polyethylene container.

MK-30, MK-35 (continued)



NOTE: The surface to which the transistor is mounted must be smooth, flat and free of burrs or irregularities which may damage insulation or prevent intimate contact with the transistor mounting base.

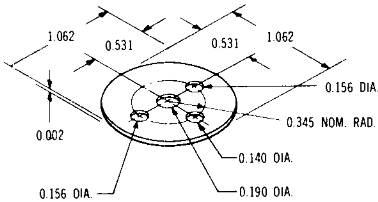
Typical thermal characteristics for mica insulators are given in the table below. (Figures may vary with mounting torque applied. Do not over stress.)

KIT TYPE	INSULATING WASHER	MAXIMUM THERMAL RESISTANCE (°C/Watt)	
		Dry	With DC4*
—	No Insulator	.20	.10
MK-30	Mica	.80	.40
MK-35	Mica	.80	.40

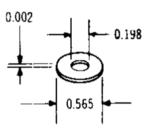
*DC4 is Dow Corning No. 4 Silicone Lubricant.

OUTLINE DIMENSIONS

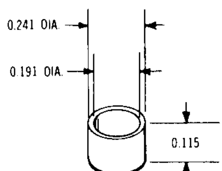
MK-30 / MK-35



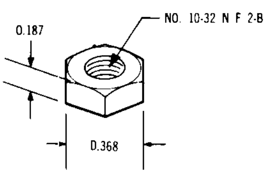
MICA INSULATOR
14B52600F06



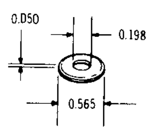
MICA WASHER
14B52600F01



NYLON INSULATING BUSHING
43B51547F01



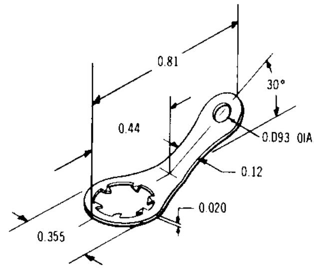
HEX NUT
(Cadmium Plated)
02B51568F13



METAL WASHER
(Cadmium Plated)
04B51567F17

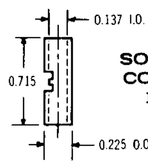
NOTE: All Dimensions Nominal

MK-30 ONLY

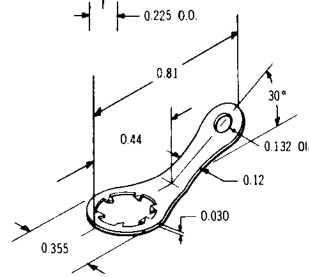


SOLDER TERMINAL
(Tin Dipped)
29B52595F13

MK-35 ONLY



SOLDERLESS CONNECTOR
10M52014A



SOLDER TERMINAL
(Cadmium Plated)
29B52595F09